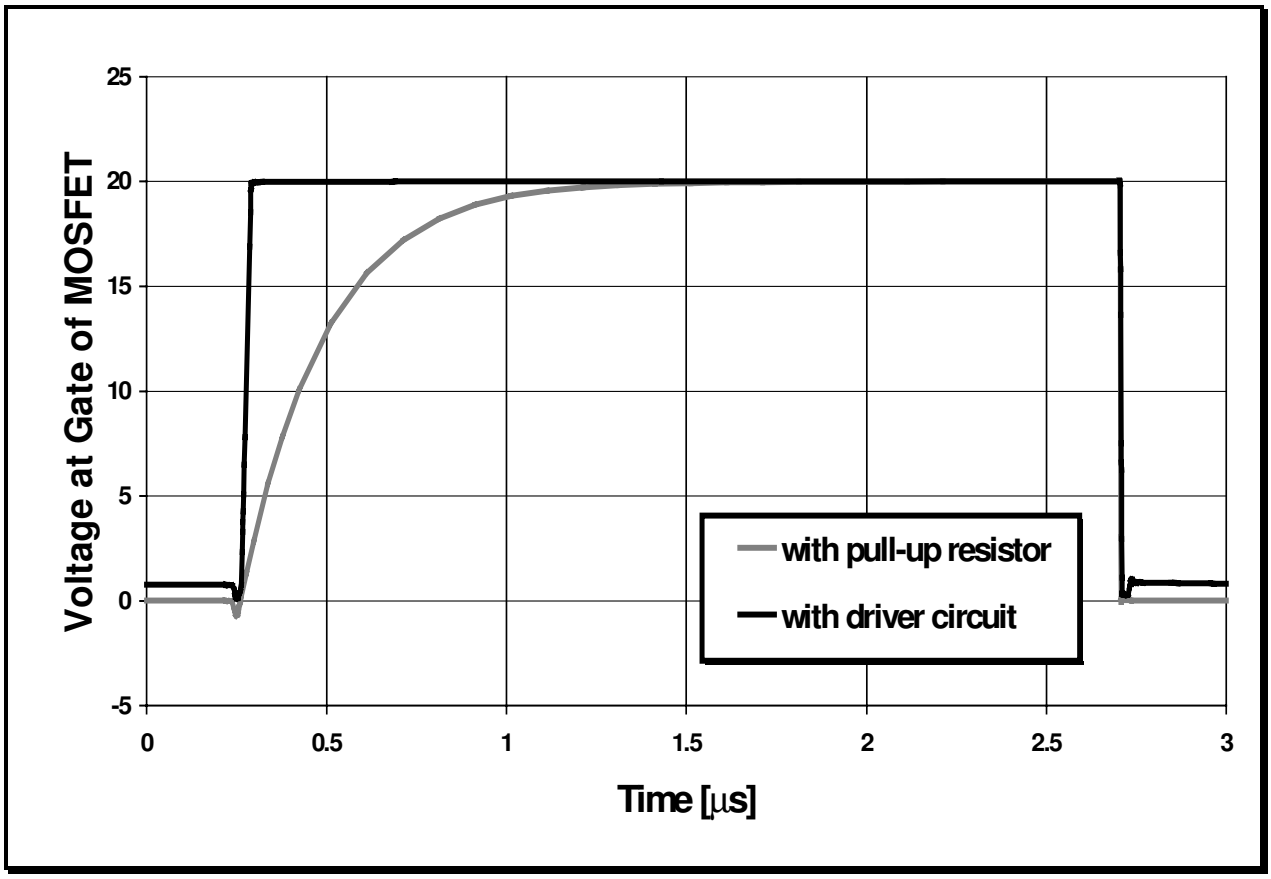

Figure 3.2: Rise of gate voltage using pull-up resistor or driver circuit

The difference is particularly apparent in the rising edge. In the circuit with the pull-up resistor, the rise time depends on the resistor R_1 and the input capacitance of the switching transistor C_{Gate}: $\tau = R_{Pull-up} \cdot C_{Gate}$. When using a driver circuit, the rise time does not depend on the pull-up resistor, but instead on the switching time of the transistors Q_1 and Q_2. The voltage V_{Gate} at the gate of the switching transistor therefore rises very quickly, and the input capacitance of the MOSFET C_{Gate} is very quickly charged and discharged.

4. Drain-Source Voltage Limiting

With MOS transistors the maximum Gate-Source voltage is usually 20 V. With circuits such as that shown in figure 3.1, the Gate-Source voltage of the switching transistor in the conducting state is about the same as the input voltage V_{CC}. When using an input voltage $V_{CC} > 20$ V an additional circuit must therefore be used to limit the Gate-Source voltage to the maximum permissible value.

The circuit shown in figure 4.1 limits the Gate-Source voltage of the MOSFET to a value which is below the maximum permissible voltage.

The Zener diode Z_1 determines the maximum Gate-Source voltage at the MOSFET. The Zener voltage V_Z of the diode Z_1 is chosen to be high enough to ensure that the MOSFET is driven sufficiently hard to attain the desired on-resistance R_{DSon} . The transistor J_1 operates as a current source. If the transistor Q_{out} is switched on, and the transistor J_1 thus conducting, then the voltage $V_{CC} - V_{Z1} - V_{D4} + V_{BE(Q2)}$ will appear at node 1. If the transistor is non-conducting, then the voltage at node 1 will again rise to that of the supply voltage V_{CC}.

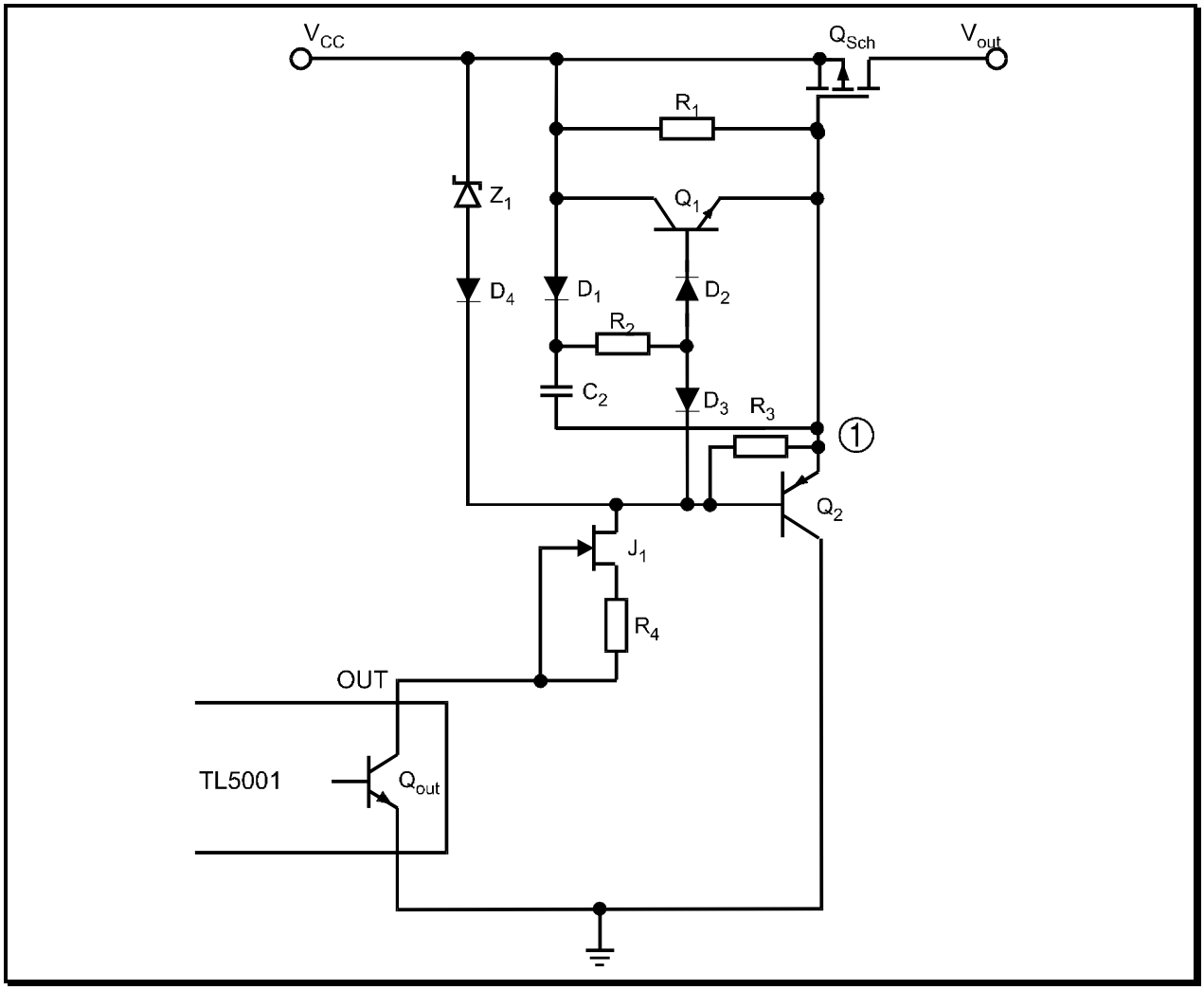

Figure 4.1: Limiting the Gate-Source voltage