TIDEP-01002

REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	07/17/2018	JAC
A1	PROTOTYPE UPDATE	10/05/2018	JAC
B	BETA UPDATE	10/09/2018	JAC

REV A TO A1 CHANGE SUMMARY:

Sheet 01: Bump schematic version to Rev A1.
Sheet 02: Add note for LP8860 EEPROM defaults.
Sheet 10: Add DS9xx note to terminate unused lvds with 100 ohm.
Sheet 14: Change R608 from 3.32K to 1K for lower default level.
Sheet 16: Change LP87xx nRST to VSYS_3V3 so PMIC will power up.
Sheet 16: Change C608 to no-pop to speed up the VIO_3V3 ramp.
Sheet 17: Add pull-ups to SD card interface that got inadvertently dropped from LCARD.

REV A1 TO B CHANGE SUMMARY:

Sheet 01: Bump schematic version to Rev B.
Sheet 10: Terminate unused lvds with 100 ohm.
Sheet 10: Fix inversion of OXA_2:0 -/+
Sheet 17: Update SD card connector, non-EOL part

REVISION STATUS OF SHEETS

REV												
SH												
REV												
SH												
REV	A	A	A	A1	A	A1	A1					
SH	11	12	13	14	15	16	17					
REV	B	A1	A	A	A	A	A	A	A	B	NEXT ASSY	USED ON
SH	1	2	3	4	5	6	7	8	9	10	APPLICATION	

DWN	J.A.C.	DATE 07/17/2018
CHK	T.W.K.	DATE 07/17/2018
ENGR	J.A.C.	DATE 07/17/2018
ENGR-MGR	J.A.C.	DATE 07/17/2018
QA	C.M.D.	DATE 07/17/2018
MFG	J.A.C.	DATE 07/17/2018
RLSE	J.A.C.	DATE 07/17/2018

TEXAS INSTRUMENTS INCORPORATED

Preliminary Information - Subject to change

Title: DRA71x DCARD CPU Board		
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INDEX	BALL	SIGNAL	GPIO	RAIL	IPU/IPD	SCHEMATIC NET	XPU/XPD	
1	L3	GPMC_A11	GPIO2_1	VDDSHV10	PD	H_DS90C189_RSTn	PD-10K	1.8V GPIO
2	A18	MCASP1_AXR8	GPIO5_10	VDDSHV3	PD	H_DCAN1_STB	PD-10K	
3	B17	MCASP1_AXR9	GPIO5_11	VDDSHV3	PD	H_DCAN1_EN	PD-10K	
4	B16	MCASP1_AXR10	GPIO5_12	VDDSHV3	PD	H_DCAN1_nFAULT	PU-10K	
5	A15	MCASP1_AXR4	GPIO5_6	VDDSHV3	PD	ENET_EN	PU-3.32K	*
6	A14	MCASP1_AXR5	GPIO5_7	VDDSHV3	PD	ENET_WAKE	PU-3.32K	*
7	A17	MCASP1_AXR6	GPIO5_8	VDDSHV3	PD	ENET_INH	PU-3.32K	*
8	A16	MCASP1_AXR7	GPIO5_9	VDDSHV3	PD	ENET_INTSn	PU-3.32K	*
9	AA1	MMC3_DAT5	GPIO1_23	VDDSHV7	PU	HDMI_HPD	IPU-10K	
10	AB1	MMC3_DAT7	GPIO1_25	VDDSHV7	PU	HDMI_CEC_A	IPU-10K	
11	Y2	MMC3_CLK	GPIO6_29	VDDSHV7	PU	MMC_PWR_ON	PU-10K	
12	Y1	MMC3_CMD	GPIO6_30	VDDSHV7	PU	EN_SDIO_3V3	PU-10K	
13	Y4	MMC3_DAT0	GPIO6_31	VDDSHV7	PU	H_DISPLAY_RSTn	PD-3.32K	*
14	F24	SPI2_CS0	GPIO7_17	VDDSHV3	PU	H_TAS2505_RSTn	PD-3.32K	*
15	W2	MMC3_DAT3	GPIO7_2	VDDSHV7	PU	GPIO_7_2	PD-3.32K	*
16	Y3	MMC3_DAT4	GPIO1_22	VDDSHV7	PU	GPIO1_22/EHRPWM3A	PU-10K	
17	Y5	GPIO6_10	GPIO6_10	VDDSHV7	PU	GP6_10/EHRPWM2A	PU-10K	
18	Y6	GPIO6_11	GPIO6_11	VDDSHV7	PU	GP6_11/EHRPWM2B	PU-10K	

Device	I2C1	I2C2
CPU ID EEPROM	0x50	
CPU TAS2505IR	0x18	
CPU LP87523-Q1	0x60	
CPU LP8860-Q1	0x2D	
CPU HDMI EEDID		0x50

POWER RAILS	VOLTAGE
VDDSHV1	3.3V
VDDSHV3	3.3V
VDDSHV4	3.3V
VDDSHV7	3.3V
VDDSHV8	3.3V/1.8V
VDDSHV9	3.3V
VDDSHV10	1.8V
VDDSHV11	1.8V

```
uint8_t lp8860_eeprom[] = {
0xED,  //60
0xDC,  //61
0xDC,  //62
0xF8,  //63
0xDD,  //64
0xE5,  //65
0xFA,  //66 F8 PWM, FA BRT_REG
0x77,  //67
0x77,  //68
0x71,  //69
0x3F,  //6A
0xB7,  //6B
0x17,  //6C
0xEF,  //6D
0xB0,  //6E
0x8B,  //6F
0xCE,  //70
0xCA,  //71
0xE5,  //72
0xE4,  //73
0x35,  //74
0x06,  //75
0xDA,  //76
0xFF,  //77
0x3E};  //78
```

HS1

APF19-19-10CB/A01

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DRA71x / DRA79x / TDA2E-17 / AM570x

Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

U27A

HDMI
VDDA_HDMI

hdmi1_data2x / hdmi1_data2y — AE14 / AD15 — H_HDMI_DX2 13 / H_HDMI_DY2 13
hdmi1_data1x / hdmi1_data1y — AE12 / AD13 — H_HDMI_DX1 13 / H_HDMI_DY1 13
hdmi1_data0x / hdmi1_data0y — AE11 / AD12 — H_HDMI_DX0 13 / H_HDMI_DY0 13
hdmi1_clockx / hdmi1_clocky — AE9 / AD10 — H_HDMI_CLKX 13 / H_HDMI_CLKY 13

GPMC/GPIO
VDDSHV10

M1 gpmc_a0/vin1a_d16/vout3_d16/vin1b_d0/i2c4_scl/uart5_rxd/gpio7_3/gpmc_a26/gpmc_a16
M2 gpmc_a1/vin1a_d17/vout3_d17/vin1b_d1/i2c4_sda/uart5_txd/gpio7_4
L2 gpmc_a2/vin1a_d18/vout3_d18/vin1b_d2/uart7_rxd/uart5_ctsn/gpio7_5
L1 gpmc_a3/qspi1_cs2/vin1a_d19/vout3_d19/vin1b_d3/uart7_txd/uart5_rtsn/gpio7_6
K3 gpmc_a4/qspi1_cs3/vin1a_d20/vout3_d20/vin1b_d4/i2c5_scl/uart6_rxd/gpio1_26
K2 gpmc_a5/vin1a_d21/vout3_d21/vin1b_d5/i2c5_sda/uart6_txd/gpio1_27
J1 gpmc_a6/vin1a_d22/vout3_d22/vin1b_d6/uart8_rxd/uart6_ctsn/gpio1_28
K1 gpmc_a7/vin1a_d23/vout3_d23/vin1b_d7/uart8_txd/uart6_rtsn/gpio1_29
K4 gpmc_a8/vin1a_hsync0/vout3_hsync/vin1b_hsync1/timer12/spi4_sclk/gpio1_30
H1 gpmc_a9/vin1a_vsync0/vout3_vsync/vin1b_vsync1/timer1 1/spi4_d1/gpio1_31
J2 gpmc_a10/vin1a_de0/vout3_de/vin1b_clk1/timer10/spi4_d0/gpio2_0
L3 gpmc_a11/vin1a_fld0/vout3_fld/vin1b_de1/timer9/spi4_cs0/gpio2_1
G1 gpmc_a12/gpmc_a0/vin1b_fld1/timer8/spi4_cs1/dma_evt1/gpio2_2
H3 gpmc_a13/qspi1_rtclk/timer7/spi4_cs2/dma_evt2/gpio2_3
H4 gpmc_a14/qspi1_d3(I)/timer6/spi4_cs3/gpio2_4
K6 gpmc_a15/qspi1_d2(I)/timer5/gpio2_5
K5 gpmc_a16/qspi1_d0(I/O)/gpio2_6
G2 gpmc_a17/qspi1_d1(I)/gpio2_7
F2 gpmc_a18/qspi1_sclk/gpio2_8

GPIO
VDDSHV3

gpio6_14/mcasp1_axr8/dcan2_tx/uart10_rxd/i2c3_sda/timer1/gpio6_14 — H21
gpio6_15/mcasp1_axr9/dcan2_rx/uart10_txd/i2c3_scl/timer2/gpio6_15 — K22
gpio6_16/mcasp1_axr10/clkout1/timer3/gpio6_16 — K23

SYSTEM

GPMC/MMC2
VDDSHV11

A4 gpmc_a19/mmc2_dat4/gpmc_a13/vin2b_d0/vin1b_d0/gpio2_9
E7 gpmc_a20/mmc2_dat5/gpmc_a14/vin1b_d1/vin1b_d1/gpio2_10
D6 gpmc_a21/mmc2_dat6/gpmc_a15/vin1b_d2/vin1b_d2/gpio2_11
C5 gpmc_a22/mmc2_dat7/gpmc_a16/vin2b_d3/vin1b_d3/gpio2_12
B5 gpmc_a23/mmc2_clk/gpmc_a17/vin2b_d4/vin1b_d4/gpio2_13
D7 gpmc_a24/mmc2_dat0/gpmc_a18/vin2b_d5/vin1b_d5/gpio2_14
C6 gpmc_a25/mmc2_dat1/gpmc_a19/vin2b_d6/vin1b_d6/gpio2_15
A5 gpmc_a26/mmc2_dat2/gpmc_a20/vin2b_d7/vin1b_d7/gpio2_16
B6 gpmc_a27/mmc2_dat3/gpmc_a21/vin2b_hsync1/vin1b_hsync1/gpio2_17
A6 gpmc_cs1/mmc2_cmd/gpmc_a22/vin2b_vsync1/vin1b_vsync1/gpio2_18

GPMC/GPIO
VDDSHV10

F1 gpmc_ad0/vin1a_d0/vout3_d0/gpio1_6/sysboot0
E2 gpmc_ad1/vin1a_d1/vout3_d1/gpio1_7/sysboot1
E1 gpmc_ad2/vin1a_d2/vout3_d2/gpio1_8/sysboot2
C1 gpmc_ad3/vin1a_d3/vout3_d3/gpio1_9/sysboot3
D1 gpmc_ad4/vin1a_d4/vout3_d4/gpio1_10/sysboot4
D2 gpmc_ad5/vin1a_d5/vout3_d5/gpio1_11/sysboot5
B1 gpmc_ad6/vin1a_d6/vout3_d6/gpio1_12/sysboot6
B2 gpmc_ad7/vin1a_d7/vout3_d7/gpio1_13/sysboot7
C2 gpmc_ad8/vin1a_d8/vout3_d8/gpio7_18/sysboot8
D3 gpmc_ad9/vin1a_d9/vout3_d9/gpio7_19/sysboot9
A2 gpmc_ad10/vin1a_d10/vout3_d10/gpio7_28/sysboot10
B3 gpmc_ad11/vin1a_d11/vout3_d11/gpio7_29/sysboot11
C3 gpmc_ad12/vin1a_d12/vout3_d12/gpio1_18/sysboot12
C4 gpmc_ad13/vin1a_d13/vout3_d13/gpio1_19/sysboot13
A3 gpmc_ad14/vin1a_d14/vout3_d14/gpio1_20/sysboot14
B4 gpmc_ad15/vin1a_d15/vout3_d15/gpio1_21/sysboot15

MEMORY-Nonvolatile

CLOCKING
VDDA_OSC

xi_osc0 — Y12 — 10pF C292 — 19.2MHz/10pF Y3 — C276 10pF — xo_osc0 AB12 — vssa_osc0 AA12
xi_osc1 — AC11
xo_osc1 — AA11
vssa_osc1 — AB11

H5 gpmc_advn_ale/gpmc_cs6/clkout2/gpmc_wait1/gpmc_a2/gpmc_a23/timer3/i2c3_sda/dma_evt2/gpio2_23/gpmc_a19
H2 gpmc_ben0/gpmc_cs4/vin2b_de1/vin1b_de1/timer2/dma_evt3/gpio2_26/gmpc_a21
H6 gpmc_ben1/gpmc_cs5/vin2b_clk1/vin1b_clk1/gpmc_a3/vin2b_fld1/vin1b_fld1/timer1/dma_evt4/gpio2_27/gpmc_a22
G5 gpmc_oen_ren/gpio2_24
G6 gpmc_wen/gpio2_25
F6 gpmc_wait0/gpio2_28/gpmc_a25/gpmc_a15
F3 gpmc_cs0/gpio2_19
G4 gpmc_cs2/qspi1_cs0/gpio2_20/gpmc_a23/gpmc_a13
G3 gpmc_cs3/qspi1_cs1/vin1a_clk0/vout3_clk/gpmc_a1/gpio2_21/gpmc_a24/gpmc_a14
L4 gpmc_clk/gpmc_cs7/clkout1/gpmc_wait1/vin2b_clk1/vin1b_clk1/timer4/i2c3_scl/dma_evt1/gpio2_22/gpmc_a20

VDDSHV3

MMC1
VDDSHV8

mmc1_clk/gpio6_21 — U3
mmc1_cmd/gpio6_22 — V4
mmc1_d0/gpio6_23 — V3
mmc1_d1/gpio6_24 — V2
mmc1_d2/gpio6_25 — W1
mmc1_d3/gpio6_26 — V1
mmc1_sdcd/uart6_rxd/i2c4_sda/gpio6_27 — U5
mmc1_sdwp/uart6_txd/i2c4_scl/gpio6_28 — V5

xref_clk0/mcasp2_axr8/mcasp1_axr4/mcasp1_ahclkx/mcasp5_ahclkx/atl_clk0/vin1a_d0/hdq0/clkout2/timer13/pr2_mii1_col/xx/gpio6_17 — J25
xref_clk1/mcasp2_axr9/mcasp1_axr5/mcasp2_ahclkx/mcasp6_ahclkx/atl_clk1/vin1a_clk0/timer14/pr2_mii1_crs/xx/gpio6_18 — J24
xref_clk2/mcasp2_axr10/mcasp1_axr6/mcasp3_ahclkx/mcasp7_ahclkx/alt_clk2/timer15/gpio6_19 — H24
xref_clk3/mcasp2_axr11/mcasp1_axr7/mcasp4_ahclkx/mcasp8_ahclkx/alt_clk3/hdq0/clkout3/timer16/gpio6_20 — H25 R75 0 H_XREF_CLK3 11

MMC3/GPIO
VDDSHV7

mmc3_clk/usb3_ulpi_d5/vin2b_d7/vin1a_d7/ehrpwm2_tripzone_input/pr2_mii1_txd3/xx/gpio6_29 — Y2
mmc3_cmd/spi3_sclk/usb3_ulpi_d4/vin2b_d6/vin1a_d6/eCAP2_in_PWM2_out/pr2_mii1_txd2/xx/gpio6_30 — Y1
mmc3_dat0/spi3_d1/uart5_rxd/usb3_ulpi_d3/vin2b_d5/vin1a_d5/eQEP3A_in/pr2_mii1_txd1/xx/gpio6_31 — Y4
mmc3_dat1/spi3_d0/uart5_txd/usb3_ulpi_d2/vin2b_d4/vin1a_d4/eQEP3B_in/pr2_mii1_txd0/xx/gpio7_0 — AA2
mmc3_dat2/spi3_cs0/uart5_ctsn/usb3_ulpi_d1/vin2b_d3/vin1a_d3/eQEP3_index/pr2_mii_mrt_clk/xx/gpio7_1 — AA3
mmc3_dat3/spi3_cs1/uart5_rtsn/usb3_ulpi_d0/vin2b_d2/vin1a_d2/eQEP3_strobe/pr2_mii1_rxdv/xx/gpio7_2 — W2
mmc3_dat4/spi4_sclk/uart10_rxd/usb3_ulpi_nxt/vin2b_d1/vin1a_d1/ehrpwm3A/pr2_mii1_rxd3/xx/gpio1_22 — Y3
mmc3_dat5/spi4_d1/uart10_txd/usb3_ulpi_dir/vin2b_d0/vin1a_d0/ehrpwm3B/pr2_mii1_rxd2/xx/gpio1_23 — AA1
mmc3_dat6/spi4_d0/uart10_ctsn/usb3_ulpi_stp/vin2b_de1/vin1a_hsync0/ehrpwm3_tripzone_input/pr2_mii1_rxd1/xx/gpio1_24 — AA4
mmc3_dat7/spi4_cs0/uart10_rtsn/usb3_ulpi_clk/vin2b_clk1/vin1a_vsync0/eCAP3_in_PWM3_out/pr2_mii1_rxd0/xx/gpio1_25 — AB1
gpio6_10/mdio_mclk/i2c3_sda/usb3_ulpi_d7/vin2b_hsync1/vin1a_clk/ehrpwm2a/pr2_mii_mt1_clk/xx/gpio6_10 — V5
gpio6_11/mdio_d/i2c3_scl/us3_ulpi_d6/vin2b_vsync1/vin1a_de0/ehrpwm2b/pr2_mii1_txen/xx/gpio6_11 — Y6

CONTROL
VDDSHV3

nmin_dsp — L24 H_NMIN_DSP
porz — F19
resetn — K24
rstoutn — E20
VDDA33V_USB
Wakeup0/dcan1_rx/gpio1_0/sys_nirq2 — AC10
Wakeup3/sys_nirq1/gpio1_3/dcan2_rx — AB10

Video Inputs

vin2a_d23/vin2b_d0/rgmii1_rxd0/vout2_d0/mii1_txen/pr1_mii1_crs/xx/gpio4_31 — D13
vin2a_d22/vin2b_d1/rgmii1_rxd1/vout2_d1/mii1_crs/pr1_mii1_col/xx/gpio4_30 — C13
vin2a_d21/vin2b_d2/rgmii1_rxd2/vout2_d2/mii1_col/pr1_mii1_rxlink/xx/gpio4_29 — E13
vin2a_d20/vin2b_d3/rgmii1_rxd3/vout2_d3/mii1_rxer/eCAP3_in_PWM3_out/pr1_mii1_rxer/xx/gpio4_28 — B13
vin2a_d19/vin2b_d4/rgmii1_rxctl/vout2_d4/mii1_txer/ehrpwm3_tripzone_input/pr1_mii1_rxd0/xx/gpio4_27 — F11
vin2a_d18/vin2b_d5/rgmii1_rxc/vout2_d5/mii1_txd3/ehrpwm3B/pr1_mii1_rxd1/xx/gpio4_26 — E11
vin2a_d17/vin2b_d6/rgmii1_txd0/vout2_d6/mii1_txd2/ehrpwm3A/pr1_mii1_rxd2/xx/gpio4_25 — A13
vin2a_d16/vin2b_d7/rgmii1_txd1/vout2_d7/mii1_txd1/eQEP3_strobe/pr1_mii1_rxd3/xx/gpio4_24 — A12
vin2a_d15/rgmii1_txd2/vout2_d8/mii1_txd0/eQEP3_index/pr1_mii1_rxdv/xx/gpio4_16 — B12
vin2a_d14/rgmii1_txd3/vout2_d9/mii1_txclk/eQEP3B_in/pr1_mii_mr1_clk/xx/gpio4_15 — C11
vin2a_d13/rgmii1_txctl/vout2_d10/mii1_rxdv/kbd_row8/eQEP3A_in/pr1_mii1_txd0/xx/gpio4_14 — D11
vin2a_d12/rgmii1_txc/vout2_d11/mii1_rxclk/kbd_col8/eCAP2_in_PWM2_out/pr1_mii1_txd1/xx/gpio4_13 — D10
vin2a_d11/mdio_d/vout2_d12/kbd_row7/ehrpwm2_tripzone_input/pr1_mdio_data/xx/gpio4_12/gpmc_a23 — C10
vin2a_d10/mdio_mclk/vout2_d13/kbd_col7/ehrpwm2B/pr1_mdio_mdclk/xx/gpio4_11/gpmc_a24 — E10
vin2a_d9/vout2_d14/emu19/mii1_rxd0/kbd_col6/ehrpwm2A/pr1_mii1_txd2/xx/gpio4_10/gpmc_a25 — B10
vin2a_d8/vout2_d15/emu18/mii1_rxd3/kbd_col5/eQEP2_strobe/pr1_mii1_txd3/xx/gpio4_9/gpmc_a26 — A10
vin2a_d7/vout2_d16/emu17/mii1_rxd2/kbd_col4/eQEP2_index/pr1_mii1_txen/xx/gpio4_8 — F10
vin2a_d6/vout2_d17/emu16/mii1_rxd1/kbd_col3/eQEP2B_in/pr1_mii_mt1_clk/xx/gpio4_7 — A11
vin2a_d5/vout2_d18/emu15/uart10_rtsn/kbd_col2/eQEP2A_in/pr1_edio_sof/xx/gpio4_6 — A8
vin2a_d4/vout2_d19/emu14/uart10_ctsn/kbd_col1/ehrpwm1_synco/pr1_edc_sync0_out/xx/gpio4_5 — A9
vin2a_d3/vout2_d20/emu13/uart10_txd/kbd_col0/ehrpwm1_synci/pr1_edc_latch0_in/xx/gpio4_4 — A7
vin2a_d2/vout2_d21/emu12/uart10_rxd/kbd_row6/eCAP1_in_PWM1_out/pr1_ecap0_ecap_capin_apwm_o/xx/gpio4_3 — B9
vin2a_d1/vout2_d22/emu11/uart9_rtsn/spi4_cs0/kbd_row5/ehrpwm1_tripzone_input/pr1_uart0_txd/xx/gpio4_2 — C8
vin2a_d0/vout2_d23/emu10/uart9_ctsn/spi4_d0/kbd_row4/ehrpwm1B/pr1_uart0_rxd/xx/gpio4_1

vin2a_clk0/vout2_fld/emu5/kbd_row0/eQEP1A_in/xx/gpio3_28/gpmc_a27/gpmc_a17 — D8
vin2a_vsync0/vin2b_vsync1/vout2_vsync/emu9/uart9_txd/spi4_d1/kbd_row3/ehrpwm1A/pr1_uart0_rts_n/xx/gpio4_0 — B8
vin2a_hsync0/vin2b_hsync1/vout2_hsync/emu8/uart9_rxd/spi4_sclk/kbd_row2/eQEP1_strobe/pr1_uart0_cts_n/xx/gpio3_31/gpmc_a27 — E8
vin2a_fld0/vin2b_clk1/vout2_clk/emu7/eQEP1_index/xx/gpio3_30/gpmc_a27/gpmc_a18 — C7
vin2a_de0/vin2a_fld0/vin2b_fld1/vin2b_de1/vout2_de/emu6/kbd_row1/eQEP1B_in/xx/gpio3_29 — B7

I2C
VDDSHV3

i2c1_scl — G22 — H_I2C1_SCL 9,10,11,14,16
i2c1_sda — G23 — H_I2C1_SDA 9,10,11,14,16
i2c2_scl/hdmi1_ddc_sda — G21 R266 0 — HDMI_DSDA 13
i2c2_sda/hdmi1_ddc_scl — F23 R265 0 — HDMI_DSCL 13
PULLUPS AT HDMI

VIN2
VDDSHV1

Debug
VDDSHV3

emu0/gpio8_30 — C21 — H_EMU0 12
emu1/gpio8_31 — C22 — H_EMU1 12
emu2 — E14 R292 22 — H_EMU2 12
emu3 — F14 — H_EMU3 12
emu4 — F13 — H_EMU4 12
EMU2 IS DEFAULT TRACE CLOCK.

rtck/gpio8_29 — K25 R70 22 — H_JTAG_RTCK 12
tclk — K21 — H_JTAG_TCK 12
tdi/gpio8_27 — L23 — H_JTAG_TDI 12
tdo/gpio8_28 — J20 R264 22 — H_JTAG_TDO 12
tms — L21 — H_JTAG_TMS 12
trstn — L22 — H_JTAG_TRSTn 12

CSI
VDDA_CSI

csi2_0_dx0 / csi2_0_dy0 — AC1 / AB2
csi2_0_dx1 / csi2_0_dy1 — AD1 / AC2
csi2_0_dx2 / csi2_0_dy2 — AE2 / AD2

Si Test

rsv_iforce — K20
rsv_vsense — G20
rsv_atestv — L19
rsv_vpp — F20 — TP32

X777AJGCBD

VIO_3V3
R447 NP
R236 NP
R71 2.2K
R262 10K
REV-B
R263 100 — EMU_RSTn 12
C375 1000pF
H_PORz 11,16
TP36
R104 2.2K
H_RSTOUTn 9,16
H_PMIC_INTn 16
R234 3.32K
R233 3.32K

VOUT3B 1.8VIO: VOUT3B_D16..D23, VOUT3B_D22, VOUT3B_HSYNC, VOUT3B_VSYNC, VOUT3B_DE, H_DS90C189_RSTn
eMMC 1.8VIO: MMC2_DAT4..DAT7, MMC2_CLK R99 0, MMC2_DAT0..DAT3, MMC2_CMD
VOUT3B 1.8VIO: VOUT3B_D0..D15
VOUT3B_CLK R445 0
H_MMC1_CLK R66 100, H_MMC1_CMD, H_MMC1_D0..D3, H_MMC1_SDCD
MMC_PWR_ON, EN_SDIO_3V3, H_DISPLAY_RSTn
GPIO7_2, GPIO1_22/EHRPWM3A, HDMI_HPD
HDMI_CEC_A, GP6_10/EHRPWM2A, GP6_11/EHRPWM2B
EMAC[1]_RXD0..RXD3, EMAC[1]_RXCTL, EMAC[1]_RXC, EMAC[1]_TXD0..TXD3, EMAC[1]_TXCTL, EMAC[1]_TXC, MDIO_MDIO, MDIO_MDCLK
H_EMU19, H_EMU18, H_EMU17..H_EMU10
H_EMU5, H_EMU9..H_EMU6
H_CSI2_DX0/DY0, H_CSI2_DX1/DY1, H_CSI2_DX2/DY2

DRA71x

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U27E

DRA71x / DRA79x / TDA2E-17 / AM570x

Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

CONNECTIVITY

PCIe

VDDA_PCIE

AD7 pcie_rxp0
AE6 pcie_rxn0
AD9 pcie_txp0
AE8 pcie_txn0
AC8 ljcb_clkp
AB9 ljcb_clkn

USB

VDDA33V_USB

AC6 usb1_dp
AB7 usb1_dn
AD3 usb1_drvvbus/timer16/gpio6_12
AB6 usb2_dp
AC5 usb2_dn
AA6 usb2_drvvbus/timer15/gpio6_13

VDDA_USB

AD6 usb_rxp0/pcie_rxp1
AE5 usb_rxn0/pcie_rxn1
AD4 usb_txp0/pcie_txp1
AE3 usb_txn0/pcie_txn1

ETHERNET

VDDSHV9

T4 rgmii0_txc/uart3_ctsn/rmii1_rxd1/mii0_rxd3/vin2a_d3/vin1b_d3/usb3_ulpi_clk/spi3_d0/spi4_cs2/pr1_mii0_rxd3/xx/gpio5_20
T5 rgmii0_txctl/uart3_rtsn/rmii1_rxd0/mii0_rxd2/vin2a_d4/vin1b_d4/usb3_ulpi_stp/spi3_cs0/spi4_cs3/pr1_mii0_rxd2/xx/gpio5_21
R1 rgmii0_txd0/rmii0_rxd0/mii0_rxd0/vin2a_d10/usb3_ulpi_d1/spi4_cs0/uart4_rtsn/pr1_mii0_rxd0/xx/gpio5_25
R2 rgmii0_txd1/rmii0_rxd1/mii0_rxd1/vin2a_vsync0/vin1b_vsync1/usb3_ulpi_d0/spi4_d0/uart4_ctsn/pr1_mii0_rxd1/xx/gpio5_24
P3 rgmii0_txd2/rmii0_rxer/mii0_rxer/vin2a_hsync0/vin1b_hsync1/usb3_ulpi_nxt/spi4_d1/uart4_txd/pr1_mii0_rxer/xx/gpio5_23
P4 rgmii0_txd3/rmii0_crs/mii0_crs/vin2a_de0/vin1b_de1/usb3_ulpi_dir/spi4_sclk/uart4_rxd/pr1_mii0_crs/xx/gpio5_22
N2 rgmii0_rxc/rmii1_txen/mii0_txclk/vin2a_d5/vin1b_d5/usb3_ulpi_d2/pr1_mii_mt0_clk/xx/gpio5_26
P2 rgmii0_rxctl/rmii1_txd1/mii0_txd3/vin2a_d6/vin1b_d6/usb3_ulpi_d3/pr1_mii0_txd3/xx/gpio5_27
N4 rgmii0_rxd0/rmii0_txd0/mii0_txd0/vin2a_fld0/vin1b_fld1/usb3_ulpi_d7/pr1_mii0_txd0/xx/gpio5_31
N3 rgmii0_rxd1/rmii0_txd1/mii0_txd1/vin2a_d9/usb3_ulpi_d6/pr1_mii0_txd1/xx/gpio5_30
P1 rgmii0_rxd2/rmii0_txen/mii0_txen/vin2a_d8/usb3_ulpi_d5/pr1_mii0_txen/xx/gpio5_29
N1 rgmii0_rxd3/rmii1_txd0/mii0_txd2/vin2a_d7/vin1b_d7/usb3_ulpi_d4/pr1_mii0_txd2/xx/gpio5_28
P5 RMII_MHZ_50_CLK/vin2a_d11/xx/gpio5_17
L6 mdio_d/uart3_ctsn/mii0_txer/vin2a_d0/vin1b_d0/pr1_mii0_rxlink/xx/gpio5_16
L5 mdio_mclk/uart3_rtsn/mii0_col/vin2a_clk0/vin1b_clk1/pr1_mii0_col/xx/gpio5_15

MLBP

VDDS_MLB

U2 mlbp_clk_p
U1 mlbp_clk_n
T2 mlbp_d_p
T1 mlbp_d_n
T3 mlbp_sig_p
U4 mlbp_sig_n

UART

VDDSHV4

M25 uart1_txd/mmc4_sdwp/gpio7_23
L25 uart1_rxd/mmc4_sdcd/gpio7_22
M24 uart1_rtsn/uart9_txd/mmc4_cmd/gpio7_25
L20 uart1_ctsn/uart9_rxd/mmc4_clk/gpio7_24

12 H_UART3_TXD_BOOT
12 H_UART3_RXD_BOOT

N25 uart2_txd/uart3_rtsn/uart3_sd/mmc4_dat1/uart2_txd/uart1_dsrn/gpio7_27
N23 uart2_rxd/uart3_ctsn/uart3_rctx/mmc4_dat0/uart2_rxd/uart1_dcdn/gpio7_26
N24 uart2_rtsn/uart3_txd/uart3_irtx/mmc4_dat3/uart10_txd/uart1_rin/gpio1_17
N22 uart2_ctsn/uart3_irrx/mmc4_dat2/uart10_rxd/uart1_dtrn/gpio1_16

VDDSHV9

N6 uart3_txd/rmii1_rxer/mii0_rxclk/vin2a_d2/vin1b_d2/spi3_d1/spi4_cs1/pr1_mii_mr0_clk/xx/gpio5_19
N5 uart3_rxd/rmii1_crs/mii0_rxdv/vin2a_d1/vin1b_d1/spi3_sclk/pr1_mii0_rxdv/xx/gpio5_18

DRA71x

MCASP

VDDSHV3

mcasp1_aclkr/mcasp7_axr2/i2c4_sda/gpio5_0 D16
mcasp1_aclkx/vin1a_fld0/i2c3_sda/pr2_mdio_mdclk/xx/gpio7_31 C16
mcasp1_fsx/vin1a_de0/i2c3_scl/pr2_mdio_data/gpio7_30 C17
mcasp1_fsr/mcasp7_axr3/i2c4_scl/gpio5_1 D17
mcasp1_axr0/uart6_rxd/vin1a_vsync0/i2c5_sda/pr2_mii0_rxer/xx/gpio5_2 D14
mcasp1_axr1/uart6_txd/vin1a_hsync0/i2c5_scl/pr2_mii_mt0_clk/xx/gpio5_3 B14
mcasp1_axr2/mcasp6_axr2/uart6_ctsn/gpio5_4 C14
mcasp1_axr3/mcasp6_axr3/uart6_rtsn/gpio5_5 B15
mcasp1_axr4/mcasp4_axr2/gpio5_6 A15 ENET_EN 11
mcasp1_axr5/mcasp4_axr3/gpio5_7 A14 ENET_WAKE 11
mcasp1_axr6/mcasp5_axr2/gpio5_8 A17 ENET_INH 11
mcasp1_axr7/mcasp5_axr3/timer4/gpio5_9 A16 ENET_INTSn 11
mcasp1_axr8/mcasp6_axr0/spi3_sclk/vin1a_d15/timer5/pr2_mii0_txen/xx/gpio5_10 A18 H_DCAN1_STB 11
mcasp1_axr9/mcasp6_axr1/spi3_d1/vin1a_d14/timer6/pr2_mii0_txd3/xx/gpio5_11 B17 H_DCAN1_EN 11
mcasp1_axr10/mcasp6_aclkx/mcasp6_aclkr/spi3_d0/vin1a_d13/timer7/pr2_mii0_txd2/xx/gpio5_12 B16 H_DCAN1_nFAULT 11
mcasp1_axr11/mcasp6_fsx/mcasp6_fsr/spi3_cs0/vin1a_d12/timer8/pr2_mii0_txd1/xx/gpio4_17 B18
mcasp1_axr12/mcasp7_axr0/spi3_cs1/vin1a_d11/timer9/pr2_mii0_txd0/xx/gpio4_18 A19
mcasp1_axr13/mcasp7_axr1/vin1a_d10/timer10/pr2_mii_mr0_clk/xx/gpio6_4 E17
mcasp1_axr14/mcasp7_aclkx/mcasp7_aclkr/vin1a_d9/timer11/pr2_mii0_rxdv/xx/gpio6_5 E16
mcasp1_axr15/mcasp7_fsx/mcasp7_fsr/vin1a_d8/timer12/pr2_mii0_rxd3/xx/gpio6_6 F16

VDDSHV3

mcasp2_aclkx/vin1a_d7/pr2_mii0_rxd2/xx E19
mcasp2_fsx/vin1a_d6/pr2_mii0_rxd1/xx D19
mcasp2_axr0 A20
mcasp2_axr1 B19
mcasp2_axr2/mcasp3_axr2/vin1a_d5/pr2_mii0_rxd0/xx/gpio6_8 A21
mcasp2_axr3/mcasp3_axr3/vin1a_d4/pr2_mii0_rxlink/xx/gpio6_9 B21
mcasp2_axr4/mcasp8_axr0/gpio1_4 B20
mcasp2_axr5/mcasp8_axr1/gpio6_7 C19
mcasp2_axr6/mcasp8_aclkx/mcasp8_aclkr/gpio2_29 D20
mcasp2_axr7/mcasp8_fsx/mcasp8_fsr/gpio1_5 C20

VDDSHV3

mcasp3_aclkx/mcasp3_aclkr/mcasp2_axr12/uart7_rxd/vin1a_d3/pr2_mii0_crs/xx/gpio5_13 A22
mcasp3_fsx/mcasp3_fsr/mcasp2_axr13/uart7_txd/vin1a_d2/pr2_mii0_col/xx/gpio5_14 A23
mcasp3_axr0/mcasp2_axr14/uart7_ctsn/uart5_rxd/vin1a_d1/pr2_mii1_rxer/xx B22
mcasp3_axr1/mcasp2_axr15/uart7_rtsn/uart5_txd/vin1a_d0/vin5a_fld0/pr2_mii1_rxlink/xx B23

VDDSHV3

mcasp4_aclkx/mcasp4_aclkr/spi3_sclk/uart8_rxd/i2c4_sda C23 R97 0 H_MCASP4_ACLKX 11
mcasp4_fsx/mcasp4_fsr/spi3_d1/uart8_txd/i2c4_scl B25 H_MCASP4_FSX 11 CLASS D AMP
mcasp4_axr0/spi3_d0/uart8_ctsn/uart4_rxd/i2c6_scl A24 H_MCASP4_AXR0 11
mcasp4_axr1/spi3_cs0/uart8_rtsn/uart4_txd/xx/i2c6_sda D23 H_MCASP4_AXR1 11

VDDSHV7

mcasp5_aclkx/mcasp5_aclkr/spi4_sclk/uart9_rxd/i2c5_sda/mlb_clk/xx AC3
mcasp5_fsx/mcasp5_fsr/spi4_d1/uart9_txd/i2c5_scl/xx U6
mcasp5_axr0/spi4_d0/uart9_ctsn/uart3_rxd/mlb_sig/pr2_mdio_mdclk/xx AA5
mcasp5_axr1/spi4_cs0/uart9_rtsn/uart3_txd/mlb_dat/pr2_mdio_data/xx AC4

SPI

VDDSHV3

spi1_cs0/gpio7_10 B24
spi1_cs1/spi2_cs1/gpio7_11 C25
spi1_cs2/uart4_rxd/mmc3_sdcd/spi2_cs2/dcan2_tx/mdio_mclk/hdmi1_hpd/gpio7_12 E24
spi1_cs3/uart4_txd/mmc3_sdwp/spi2_cs3/dcan2_rx/mdio_d/hdmi1_cec/gpio7_13 E25
spi1_d0/gpio7_9 D25
spi1_d1/gpio7_8 D24
spi1_sclk/gpio7_7 C24

spi2_cs0/uart3_rtsn/uart5_txd/gpio7_17 F24 H_TAS2505_RSTn 11
spi2_d0/uart3_ctsn/uart5_rxd/gpio7_16 G24
spi2_d1/uart3_txd/gpio7_15 F25
spi2_sclk/uart3_rxd/gpio7_14 G25

DCAN

VDDSHV3

dcan1_tx/uart8_rxd/mmc2_sdcd/hdmi1_hpd/gpio1_14 H22 H_DCAN1_TX 11
dcan1_rx/uart8_txd/mmc2_sdwp/hdmi1_cec/gpio1_15 H23 H_DCAN1_RX 11

X777AJGCBD

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U27B

8	H_DDR1_A0	AC18	ddr1_a0
8	H_DDR1_A1	AE19	ddr1_a1
8	H_DDR1_A2	AD19	ddr1_a2
8	H_DDR1_A3	AB19	ddr1_a3
8	H_DDR1_A4	AD20	ddr1_a4
8	H_DDR1_A5	AE20	ddr1_a5
8	H_DDR1_A6	AA18	ddr1_a6
8	H_DDR1_A7	AA20	ddr1_a7
8	H_DDR1_A8	Y21	ddr1_a8
8	H_DDR1_A9	AC20	ddr1_a9
8	H_DDR1_A10	AA21	ddr1_a10
8	H_DDR1_A11	AC21	ddr1_a11
8	H_DDR1_A12	AC22	ddr1_a12
8	H_DDR1_A13	AC15	ddr1_a13
8	H_DDR1_A14	AB15	ddr1_a14
8	H_DDR1_A15	AC16	ddr1_a15
8	H_DDR1_BA0	AE16	ddr1_ba0
8	H_DDR1_BA1	AA16	ddr1_ba1
8	H_DDR1_BA2	AB16	ddr1_ba2
8	H_DDR1_ODT0	AD18	ddr1_odt0
8	H_DDR1_CASN	AD16	ddr1_casn
8	H_DDR1_RASN	AD17	ddr1_rasn
8	H_DDR1_CKE	AB18	ddr1_cke
8	H_DDR1_CLK_P	AD21	ddr1_ckp
8	H_DDR1_CLK_N	AE21	ddr1_ckn
8	H_DDR1_CSN0	AC19	ddr1_csn0
8	H_DDR1_RST	AE17	ddr1_rst
8	H_DDR1_WEN	AE18	ddr1_wen
8	H_DDR1_DQM0	AE23	ddr1_dqm0
8	H_DDR1_DQS0_P	AD22	ddr1_dqs0
8	H_DDR1_DQS0_N	AE22	ddr1_dqsn0
8	H_DDR1_D0	AA23	ddr1_d0
8	H_DDR1_D1	AC24	ddr1_d1
8	H_DDR1_D2	AB24	ddr1_d2
8	H_DDR1_D3	AD24	ddr1_d3
8	H_DDR1_D4	AB23	ddr1_d4
8	H_DDR1_D5	AC23	ddr1_d5
8	H_DDR1_D6	AD23	ddr1_d6
8	H_DDR1_D7	AE24	ddr1_d7
8	H_DDR1_DQM1	W22	ddr1_dqm1
8	H_DDR1_DQS1_P	Y24	ddr1_dqs1
8	H_DDR1_DQS1_N	Y25	ddr1_dqsn1
8	H_DDR1_D8	AA24	ddr1_d8
8	H_DDR1_D9	W25	ddr1_d9
8	H_DDR1_D10	Y23	ddr1_d10
8	H_DDR1_D11	AD25	ddr1_d11
8	H_DDR1_D12	AC25	ddr1_d12
8	H_DDR1_D13	AB25	ddr1_d13
8	H_DDR1_D14	AA25	ddr1_d14
8	H_DDR1_D15	W24	ddr1_d15
8	H_DDR1_DQM2	U21	ddr1_dqm2
8	H_DDR1_DQS2_P	V24	ddr1_dqs2
8	H_DDR1_DQS2_N	V25	ddr1_dqsn2
8	H_DDR1_D16	W23	ddr1_d16
8	H_DDR1_D17	U25	ddr1_d17
8	H_DDR1_D18	U24	ddr1_d18
8	H_DDR1_D19	W21	ddr1_d19
8	H_DDR1_D20	T22	ddr1_d20
8	H_DDR1_D21	U22	ddr1_d21
8	H_DDR1_D22	U23	ddr1_d22
8	H_DDR1_D23	T21	ddr1_d23
8	H_DDR1_DQM3	P25	ddr1_dqm3
8	H_DDR1_DQS3_P	R24	ddr1_dqs3
8	H_DDR1_DQS3_N	R25	ddr1_dqsn3
8	H_DDR1_D24	T23	ddr1_d24
8	H_DDR1_D25	T25	ddr1_d25
8	H_DDR1_D26	T24	ddr1_d26
8	H_DDR1_D27	P21	ddr1_d27
8	H_DDR1_D28	N21	ddr1_d28
8	H_DDR1_D29	P22	ddr1_d29
8	H_DDR1_D30	P23	ddr1_d30
8	H_DDR1_D31	P24	ddr1_d31
	VDDR_VREFSTL	Y20	vref_ddr1

DRA71x

X777AJGCBD

DRA71x / DRA79x / TDA2E-17 / AM570x

Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

MEMORY-Volatile, DDR3

EMIF1

VDDS_DDR1

TEXAS INSTRUMENTS INCORPORATED

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DRA71x / DRA79x / TDA2E-17 / AM570x

Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

POWER

ANALOG SUPPLIES

INTERNAL LDOs

VDA_PLL_1V8

C406 1uF 10V X7S 0402
C331 0.1uF 16V 0402

E5 80dB @ 27MHz 0805 2A
C372 1uF 10V X7S 0402
C359 0.1uF 16V 0402
VDA_COREGMACVID_FIL1V8

E4 80dB @ 27MHz 0805 2A
C343 1uF 10V X7S 0402
C340 0.1uF 16V 0402
VDA_DDRDBGGPUPER_FIL1V8

E7 80dB @ 27MHz 0805 2A
C407 1uF 10V X7S 0402
C349 0.1uF 16V 0402
VDA_MPU_ABE_FIL1V8

E1 80dB @ 27MHz 0805 2A
C286 1uF 10V X7S 0402
C309 0.1uF 16V 0402
VDA_OSC_FIL1V8

E6 80dB @ 27MHz 0805 2A
C408 1uF 10V X7S 0402
C364 0.47uF 10V X7S 0402
VDA_VIDEO_FIL1V8

VDA_PHY_1V8

E3 80dB @ 27MHz 0805 2A
C324 1uF 10V X7S 0402
C333 0.1uF 16V 0402
VDA_CSI_FIL1V8

E2 80dB @ 27MHz 0805 2A
C301 1uF 10V X7S 0402
C310 0.1uF 16V 0402
VDA_HDMI_FIL1V8

C302 1uF 10V X7S 0402
C306 0.1uF 16V 0402

C308 0.1uF 16V 0402

DRA71x

R20	vdda_ddr
L9	vdda_core_gmac
K10	vdda_dsp_iva_1
L10	vdda_dsp_iva_2
N10	vdda_debug
N9	vdda_gpu
M10	vdda_per
K16	vdda_mpu_abe_1
L16	vdda_mpu_abe_2
W13	vdda_osc_1
Y13	vdda_osc_2
K14	vdda_video_1
L14	vdda_video_2
T6	vdda_csi
W15	vdda_hdmi_1
Y15	vdda_hdmi_2
W11	vdda_pcie_1
Y11	vdda_pcie_2
W8	vdda_usb_1
Y8	vdda_usb_2
Y9	vdda_usb_3
AA10	vdda33v_usb_1
Y10	vdda33v_usb_2

VIO_3V3

C285 0.1uF 0402 16V
C284 1uF 10V X7S 0402
C281 10uF 10V X7R 0805

U27C

X777AJGCBD

cap_vbbldo_dsp	F8	VCAP_VBBLDO_DSP
cap_vbbldo_gpu	T7	VCAP_VBBLDO_GPU
		VCAP_VBBLDO_IVA
		VCAP_VBBLDO_MPU
cap_vbbldo_iva	G14	
cap_vbbldo_mpu	F17	
cap_vddram_core1	U20	VCAP_VDDRAM_CORE1
		VCAP_VDDRAM_CORE3
		VCAP_VDDRAM_CORE4
cap_vddram_core3	K7	
cap_vddram_core4	G19	
cap_vddram_dsp	L7	VCAP_VDDRAM_DSP
cap_vddram_gpu	V7	VCAP_VDDRAM_GPU
		VCAP_VDDRAM_IVA
		VCAP_VDDRAM_MPU
cap_vddram_iva	G12	
cap_vddram_mpu	G18	

C394 1uF 10V X7S 0402
C395 1uF 10V X7S 0402
C329 1uF 10V X7S 0402
C388 1uF 10V X7S 0402

C412 1uF 10V X7S 0402
C358 1uF 10V X7S 0402
C322 1uF 10V X7S 0402

C374 1uF 10V X7S 0402
C426 1uF 10V X7S 0402
C320 1uF 10V X7S 0402
C334 1uF 10V X7S 0402

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DRA71x / DRA79x / TDA2E-17 / AM570x

Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

POWER

DIGITAL SUPPLIES & GNDS

VDD_CORE_AVS
C551 10uF X7R 0805 10V
C303 1uF 4V X7S 0508
C373 1uF 4V X7S 0508
C344 1uF 4V X7S 0508
C323 1uF 4V X7S 0508
C321 0.47uF 10V X7S 0402
C332 0.47uF 10V X7S 0402
C348 0.47uF 10V X7S 0402
C347 0.47uF 10V X7S 0402
C341 0.47uF 10V X7S 0402

VDD_DSP_AVS
C537 10uF X7R 0805 10V
C536 10uF X7R 0805 10V
C401 1uF 4V X7S 0508
C385 1uF 4V X7S 0508
C402 1uF 4V X7S 0508
C393 1uF 4V X7S 0508
C403 1uF 4V X7S 0508
C357 0.47uF 10V X7S 0402
C368 0.47uF 10V X7S 0402
C370 0.47uF 10V X7S 0402
C367 0.47uF 10V X7S 0402
C362 0.1uF 16V X7S 0402
C361 0.1uF 16V X7S 0402

VDDS_1V8
C108 10uF 10V X7R 0805
C380 1uF X7S 4V 0508
C434 1uF 10V X7S 0402
C428 0.47uF 10V X7S 0402
C335 0.1uF 0402 16V
C430 0.1uF 0402 16V
C431 0.1uF 0402 16V
C342 0.1uF 0402 16V
C298 0.1uF 0402 16V
C369 0.1uF 0402 16V
C318 0.1uF 0402 16V

VDD_DDR_1V35
C307 10uF 10V 0805 X7R
C289 1uF 4V 0508 X7S
C311 0.47uF 10V 0402 X7S
C352 0.47uF 10V 0402 X7S
C294 0.47uF 10V 0402 X7S
C351 0.47uF 10V 0402 X7S
C354 0.47uF 10V 0402 X7S
C312 0.47uF 10V 0402 X7S
C293 0.47uF 10V 0402 X7S
C295 0.47uF 10V 0402 X7S
C315 0.47uF 10V 0402 X7S
C319 0.47uF 10V 0402 X7S
C297 0.47uF 10V 0402 X7S
C325 0.47uF 10V 0402 X7S

VIO_3V3
C120 10uF 10V 0805 X7R
C119 4.7uF 0805 16V
C118 1uF 10V 0402 X7S
C114 0.47uF 10V 0402 X7S
C356 0.1uF 0402 16V
C296 0.1uF 0402 16V
C277 0.1uF 0402 16V
C282 0.1uF 0402 16V
C432 0.1uF 0402 16V
C345 0.1uF 0402 16V
C287 0.1uF 0402 16V
C283 0.1uF 0402 16V
C288 0.1uF 0402 16V
C379 0.1uF 0402 16V
C390 0.1uF 0402 16V

VDDSHV_134
VDDSHV_7
VDDSHV_8
VDDSHV_9
VDDSHV_10
VDDSHV_11
VDA_SDIO_DV

U27D

J15	vdd_1	H9	vdd_dsp_1
J16	vdd_2	H11	vdd_dsp_2
J18	vdd_3	H13	vdd_dsp_3
K12	vdd_4	J9	vdd_dsp_4
K18	vdd_5	J11	vdd_dsp_5
L12	vdd_6	J13	vdd_dsp_6
L17	vdd_7	G11	vdds18v_1
M11	vdd_8	H20	vdds18v_2
M13	vdd_9	W7	vdds18v_3
M15	vdd_10	Y18	vdds18v_4
M17	vdd_11	P7	vdds_mlb_1
N11	vdd_12	R7	vdds_mlb_2
N13	vdd_13	P20	vdds18v_ddr1_1
N15	vdd_14	Y19	vdds18v_ddr1_2
N18	vdd_15	AA19	vdds18v_ddr1_3
P10	vdd_16	T19	vdds_ddr1_1
P12	vdd_17	T20	vdds_ddr1_2
P14	vdd_18	W17	vdds_ddr1_3
P16	vdd_19	W18	vdds_ddr1_4
P18	vdd_20	W20	vdds_ddr1_5
R10	vdd_21		vdds_ddr1_6
R12	vdd_22	G9	vddshv1_1
R14	vdd_23	G10	vddshv1_2
R16	vdd_24	G15	vddshv3_1
R17	vdd_25	G17	vddshv3_2
T9	vdd_26	H15	vddshv3_3
T11	vdd_27	H17	vddshv3_4
T13	vdd_28	J19	vddshv3_5
T15	vdd_29	K19	vddshv3_6
T17	vdd_30	M19	vddshv4_1
U9	vdd_31	N19	vddshv4_2
U11	vdd_32	U7	vddshv7_1
U13	vdd_33	U8	vddshv7_2
U15	vdd_34	N8	vddshv8_1
U18	vdd_35	P8	vddshv8_2
V10	vdd_36	M7	vddshv9_1
V12	vdd_37	N7	vddshv9_2
V14	vdd_38	J7	vddshv10_1
V16	vdd_39	J8	vddshv10_2
V18	vdd_40	K8	vddshv10_3
W10	vdd_41	F7	vddshv11_1
W12	vdd_42	G7	vddshv11_2
W14	vdd_43	H7	vddshv11_3
W16	vdd_44		

DRA71x

X777AJGCBD

	A1	vss_44	P19	vss_87	AA8
vss_1	A25	vss_45	R8	vss_88	AA9
vss_2	G8	vss_46	R9	vss_89	AB8
vss_3	G13	vss_47	R11	vss_90	AC13
vss_4	G16	vss_48	R13	vss_91	AE1
vss_5	H8	vss_49	R15	vss_92	AE15
vss_6	H10	vss_50	R18	vss_93	AE25
vss_7	H12	vss_51	R19	vss_94	AA15
vss_8	H14	vss_52	T8	vss_95	
vss_9	H16	vss_53	T10		
vss_10	H18	vss_54	T12		
vss_11	H19	vss_55	T14		
vss_12	J10	vss_56	T16		
vss_13	J12	vss_57	T18		
vss_14	J14	vss_58	U10		
vss_15	J17	vss_59	U12		
vss_16	K9	vss_60	U14		
vss_17	K11	vss_61	U16		
vss_18	K13	vss_62	U17		
vss_19	K15	vss_63	U19		
vss_20	K17	vss_64	V8		
vss_21	L8	vss_65	V9		
vss_22	L11	vss_66	V11		
vss_23	L13	vss_67	V13		
vss_24	L15	vss_68	V15		
vss_25	L18	vss_69	V17		
vss_26	AA13	vss_70	V19		
vss_27	M8	vss_71	W9		
vss_28	M9	vss_72	W19		
vss_29	M12	vss_73	Y7		
vss_30	M14	vss_74	Y14		
vss_31	M16	vss_75	Y16		
vss_32	M18	vss_76	Y17		
vss_33	M20	vss_77	AA7		
vss_34	N12	vss_78	AA8		
vss_35	N14	vss_79	AA9		
vss_36	N16	vss_80	AB8		
vss_37	N17	vss_81	AC13		
vss_38	N20	vss_82	AE1		
vss_39	P9	vss_83	AE15		
vss_40	P11	vss_84	AE25		
vss_41	P13	vss_85	AA15		
vss_42	P15	vss_86			
vss_43	P17				

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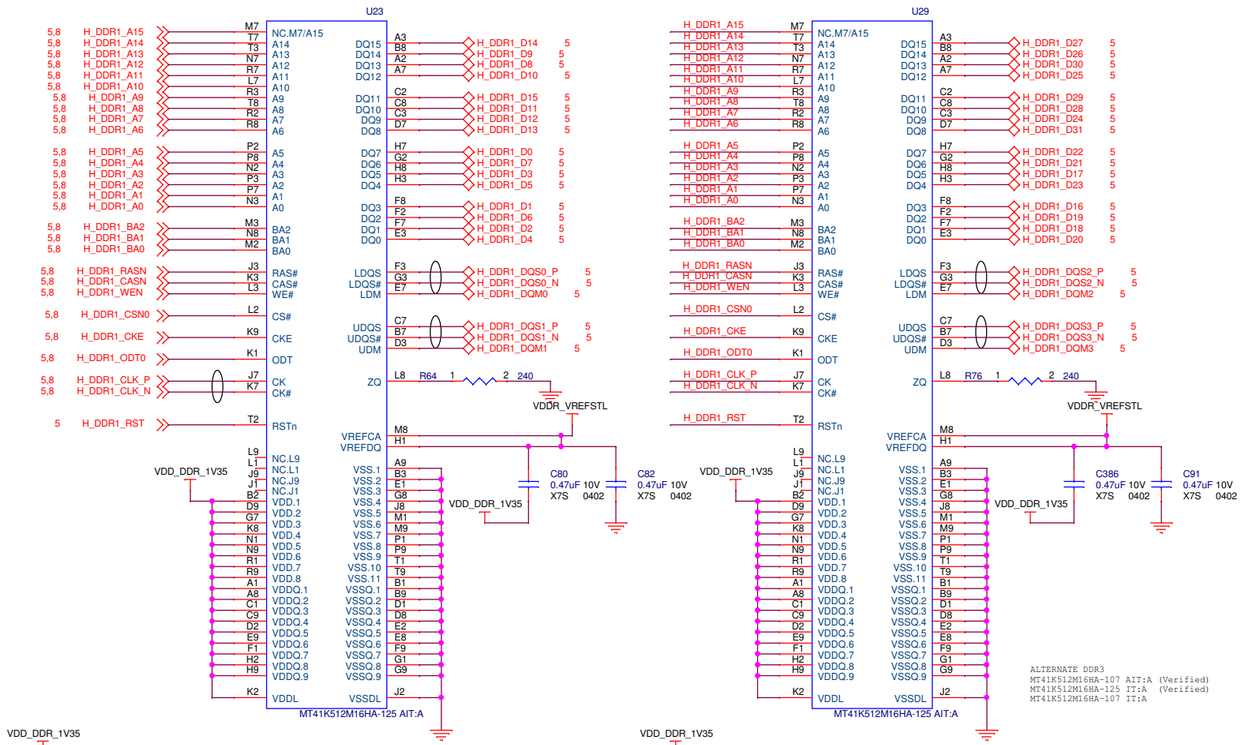

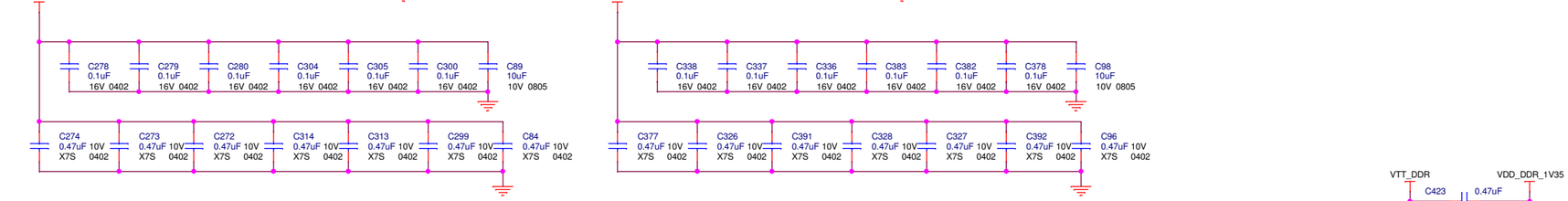

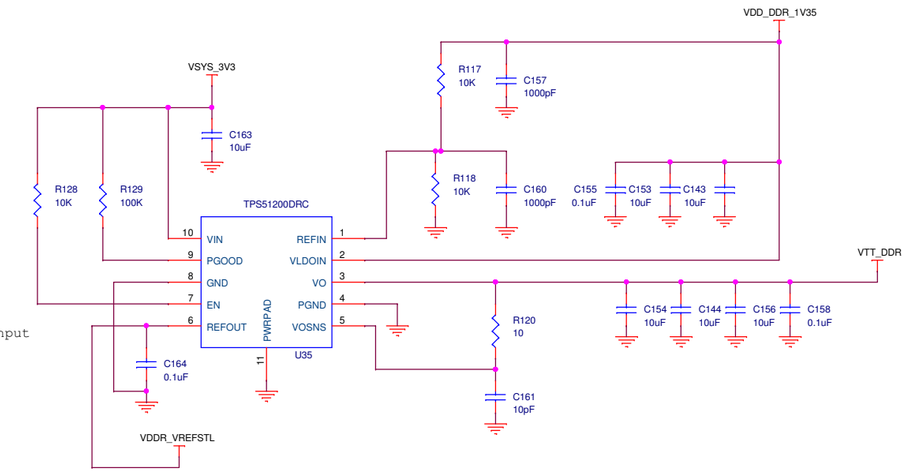

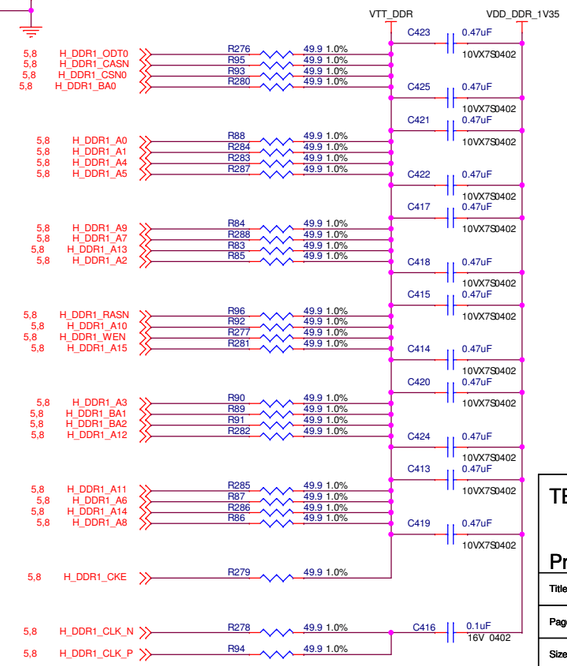

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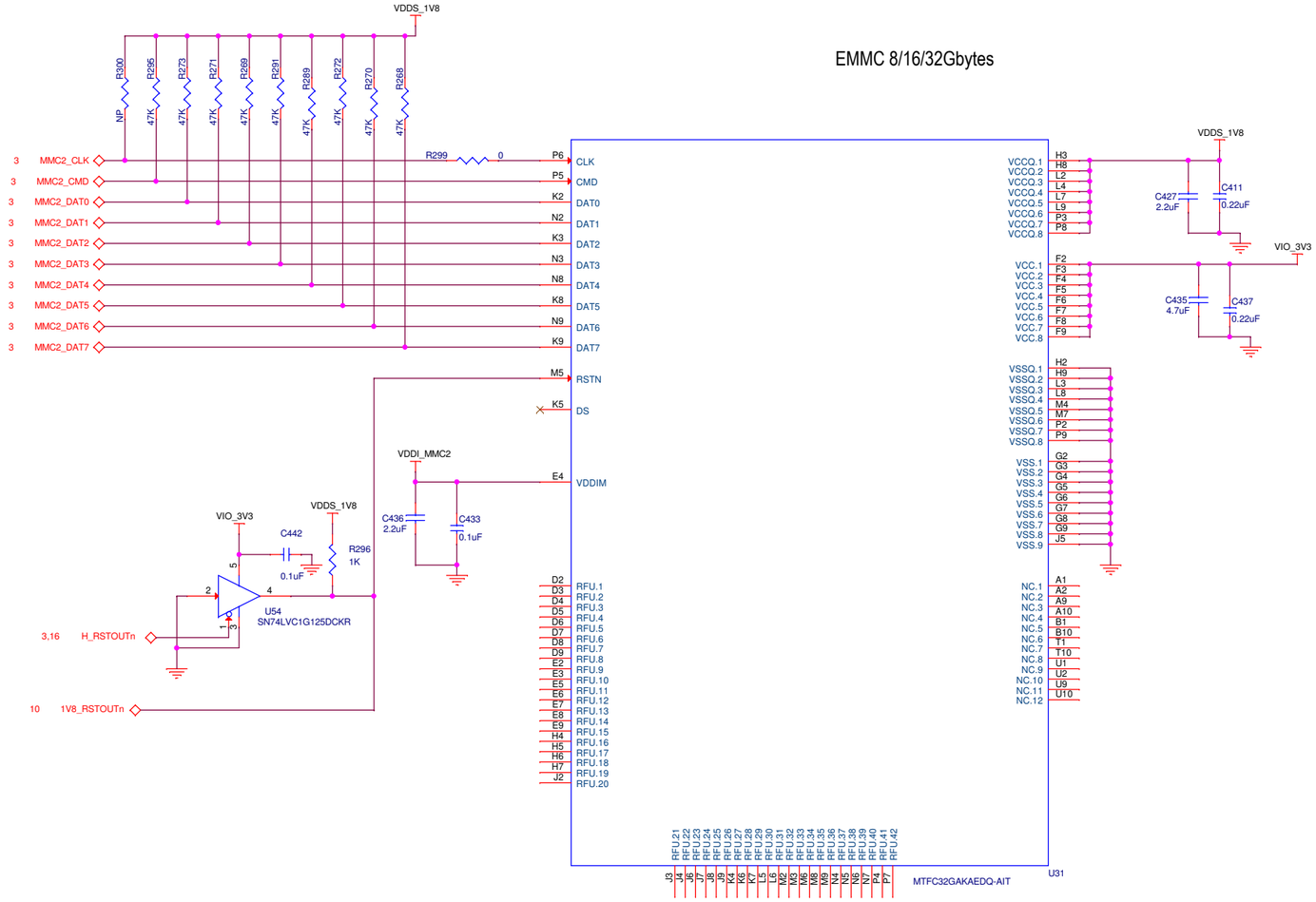
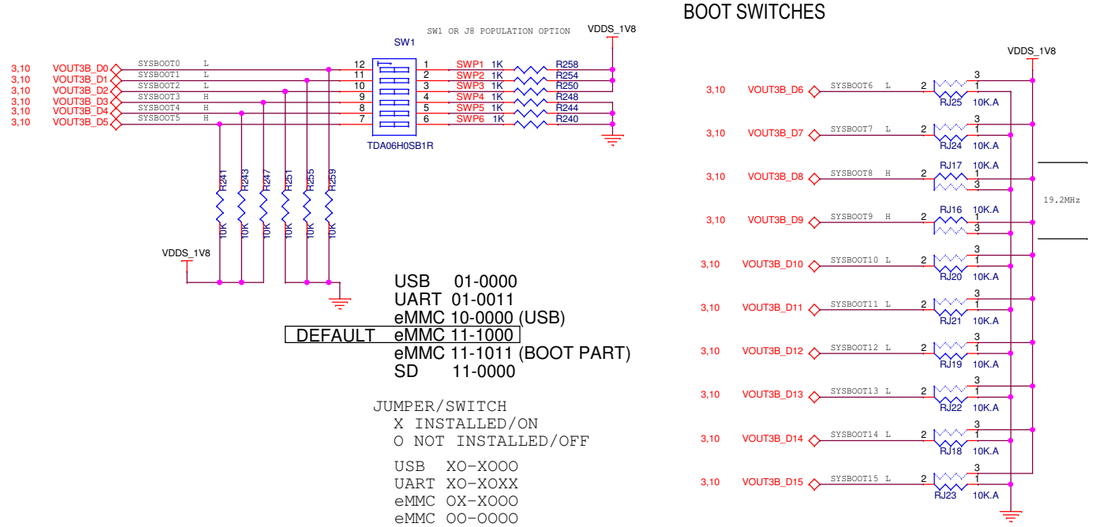
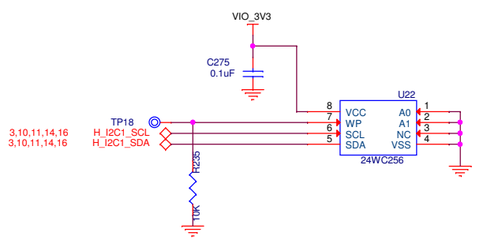
EMMC 8/16/32Gbytes



BOOT SWITCHES



ID EEPROM



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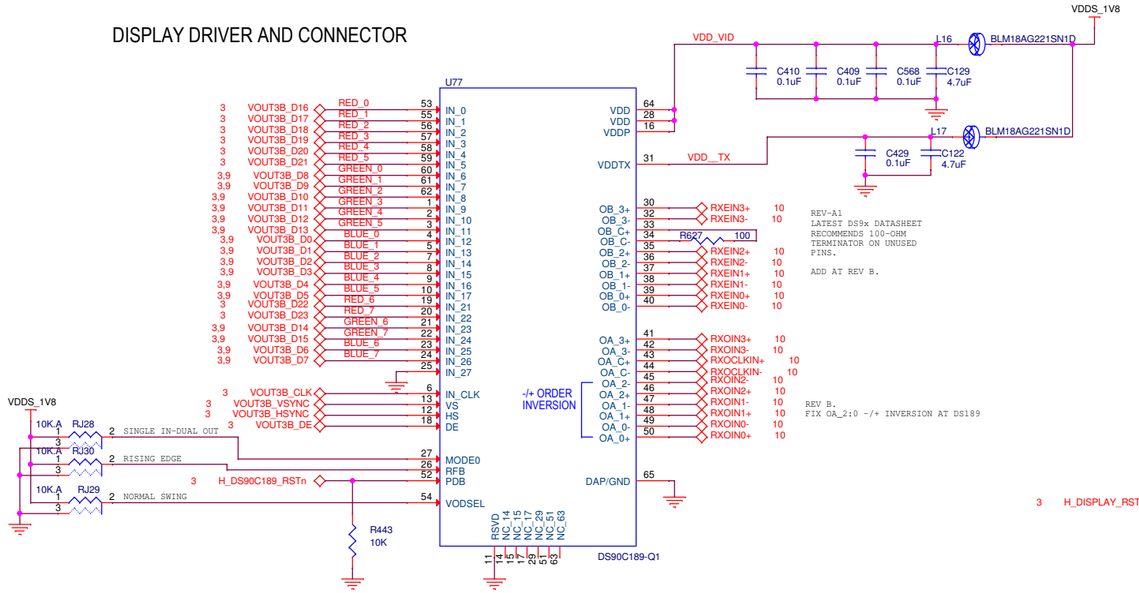
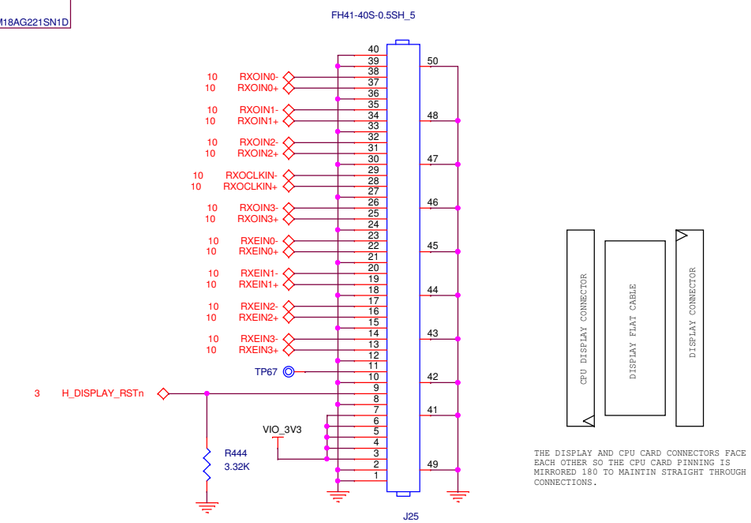
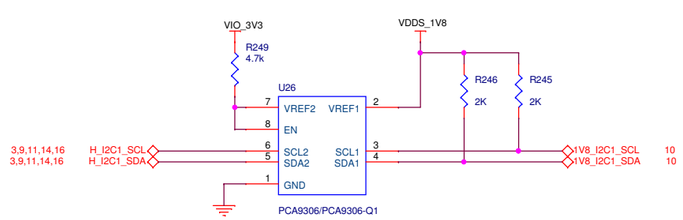
DISPLAY DRIVER AND CONNECTOR



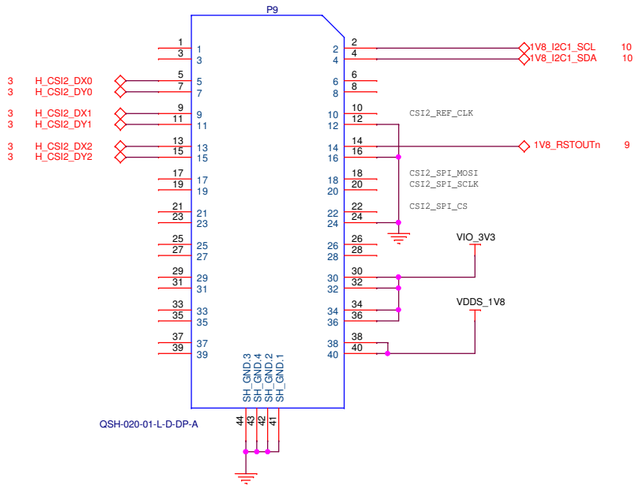


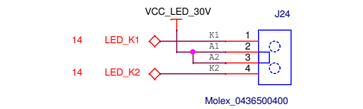
THE DISPLAY AND CPU CARD CONNECTORS FACE EACH OTHER SO THE CPU CARD PINNING IS MIRRORED 180 TO MAINTIN STRAIGHT THROUGH CONNECTIONS.

CSI2 EXPANSION

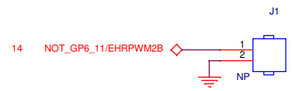


CSI2 TO MATCH J6 ENTRY EVM AT 1.8V IO





DISPLAY LED SUPPLY IS 32v@580mA MAX



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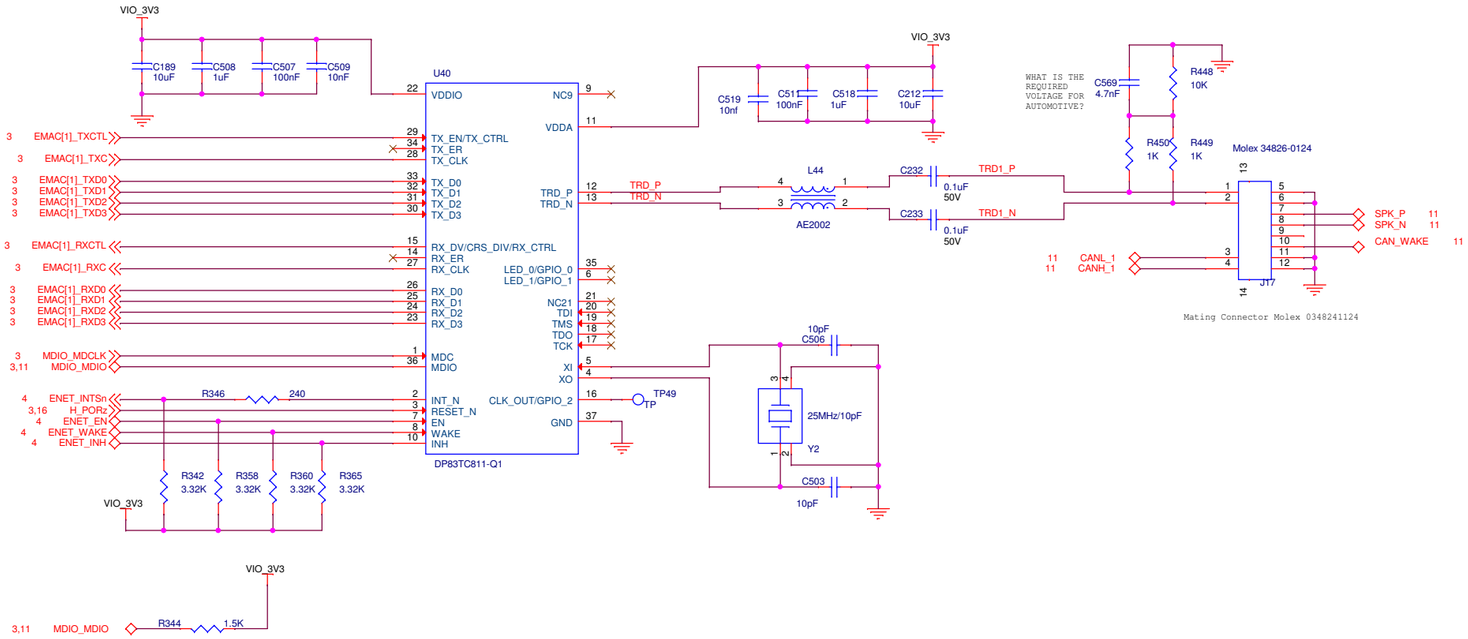
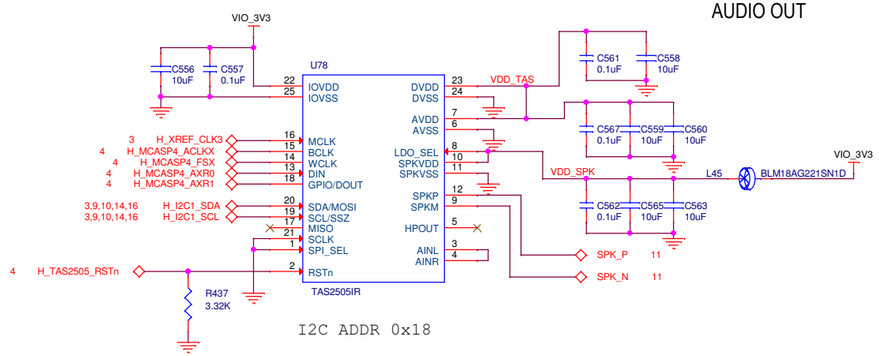
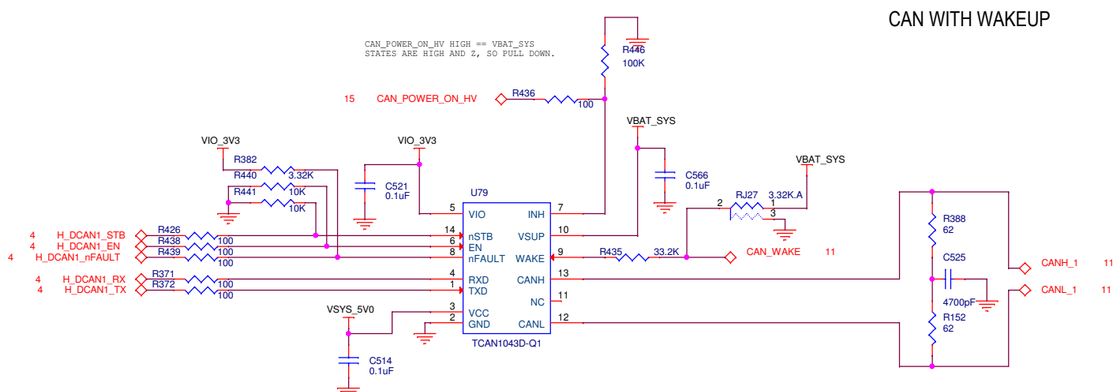
ENET



AUDIO OUT



CAN WITH WAKEUP



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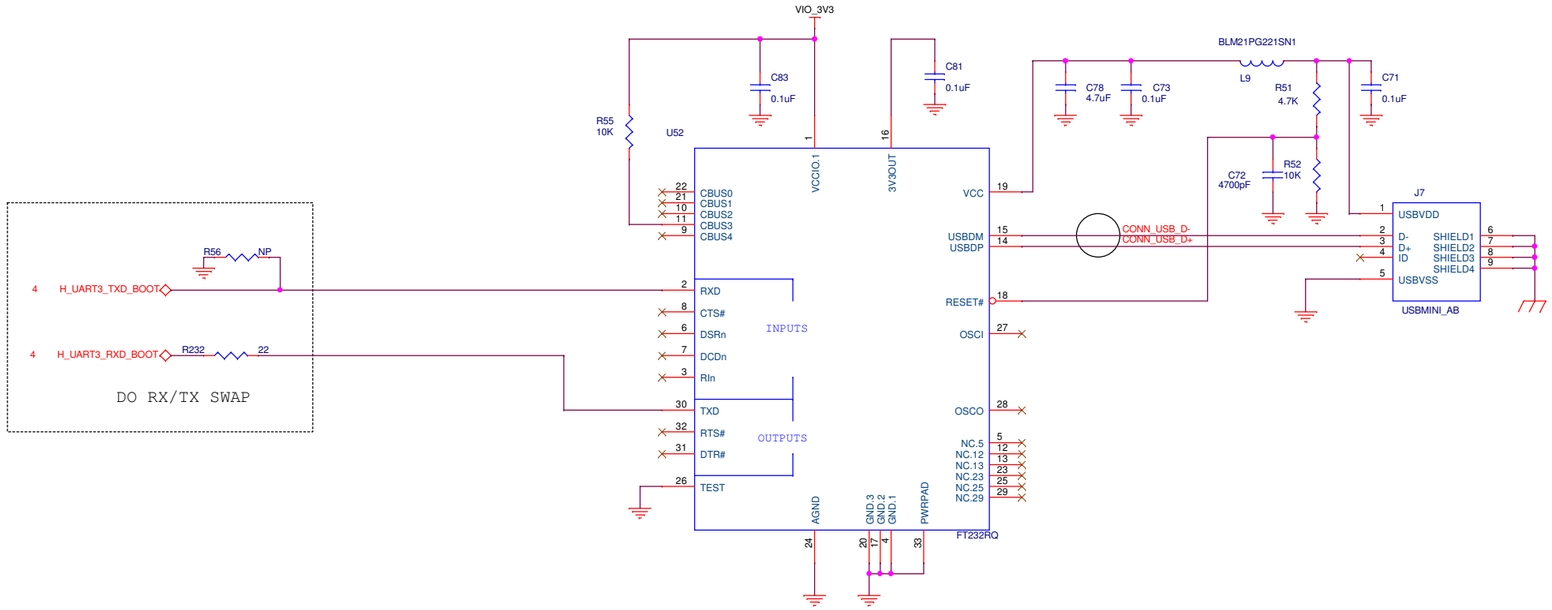
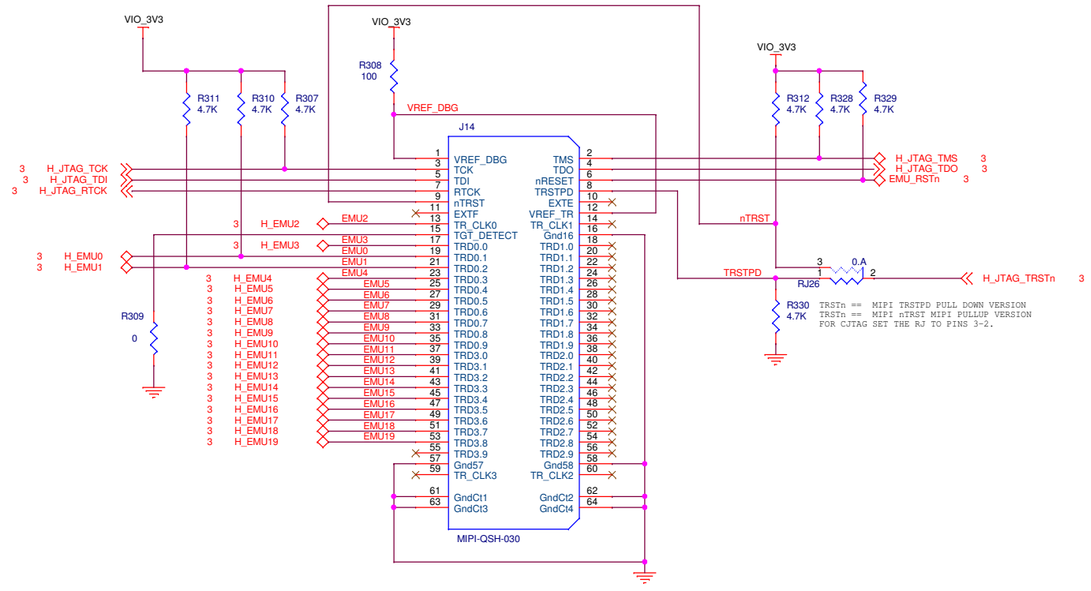
TERMINAL/UART-BOOT



JTAG/DEBUG



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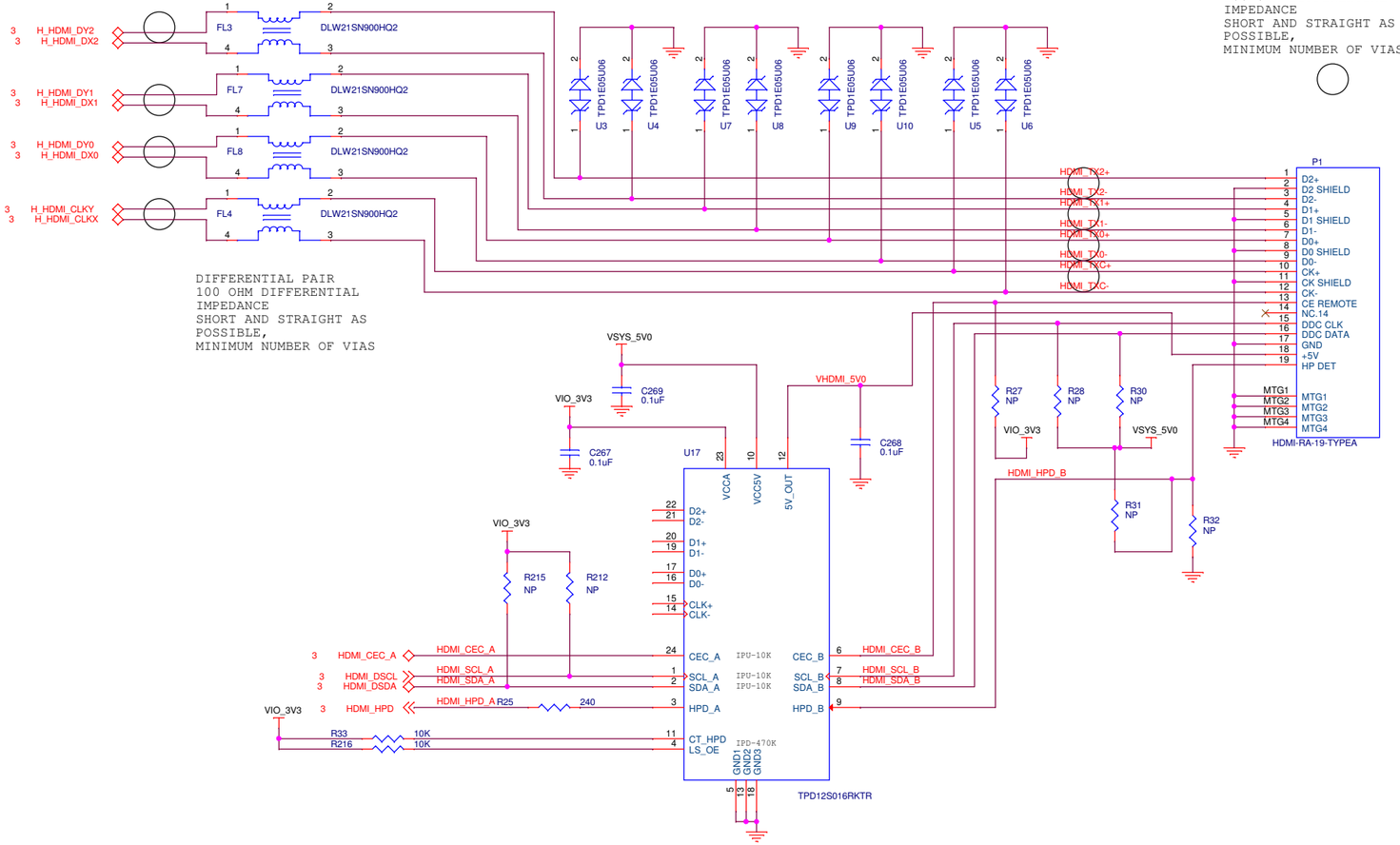
DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS



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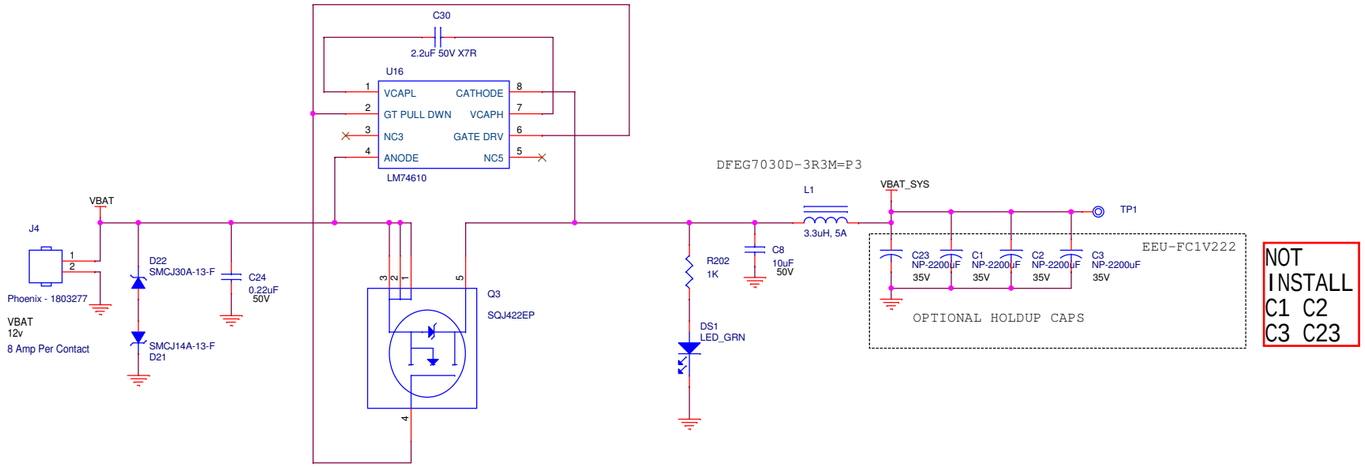
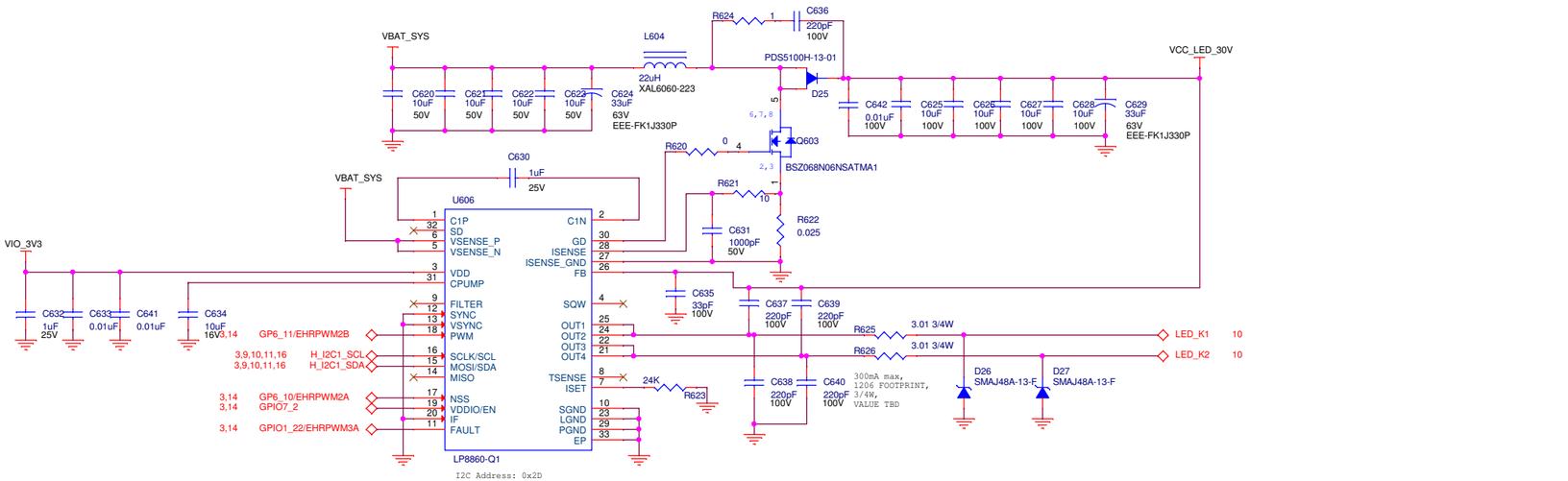
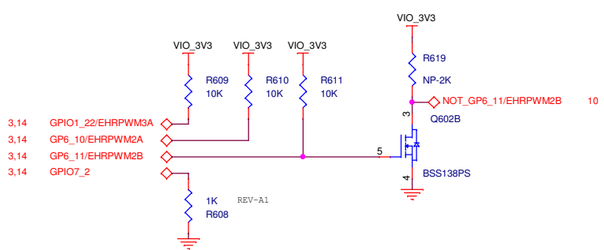
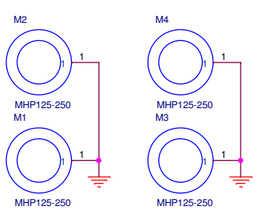


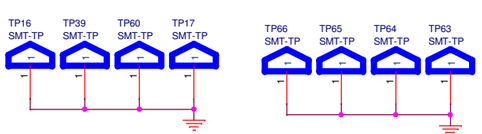
POWER INPUT AND PROTECTION

30V DISPLAY LED POWER









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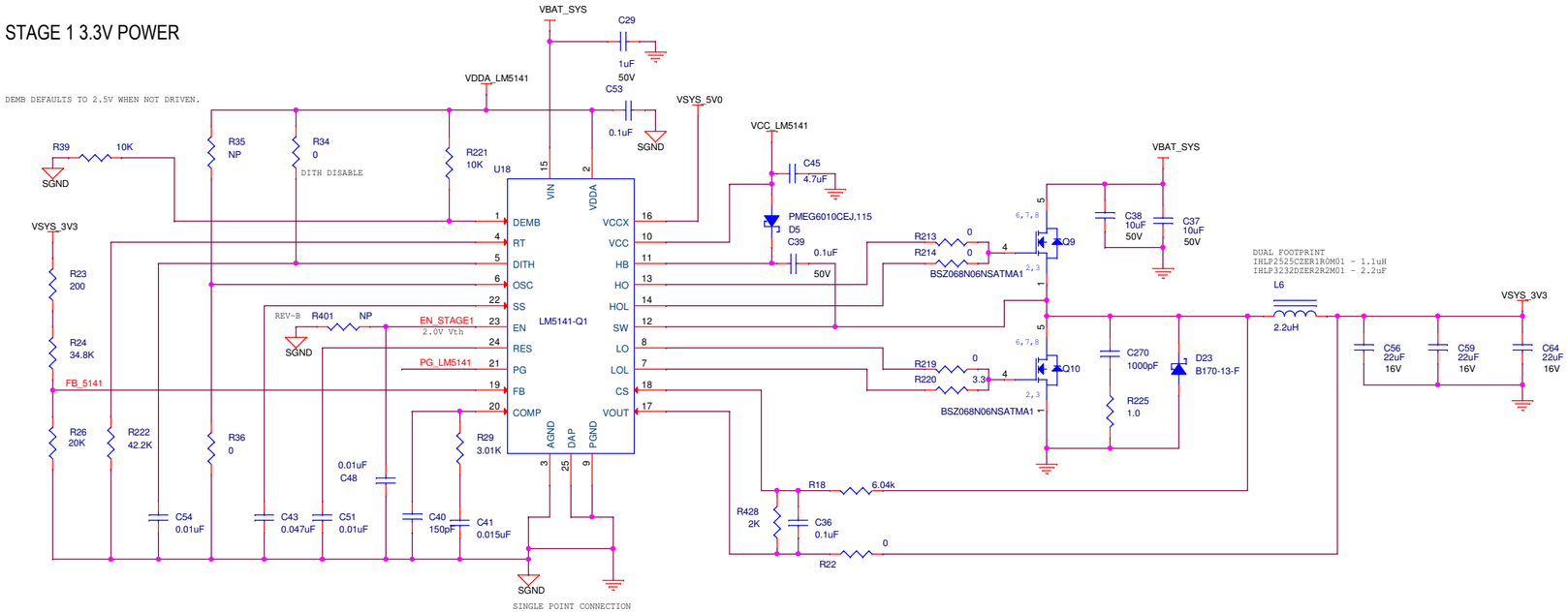
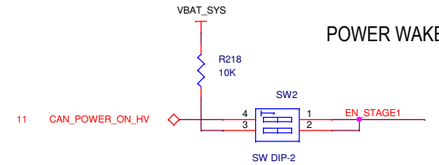
STAGE 1 3.3V POWER



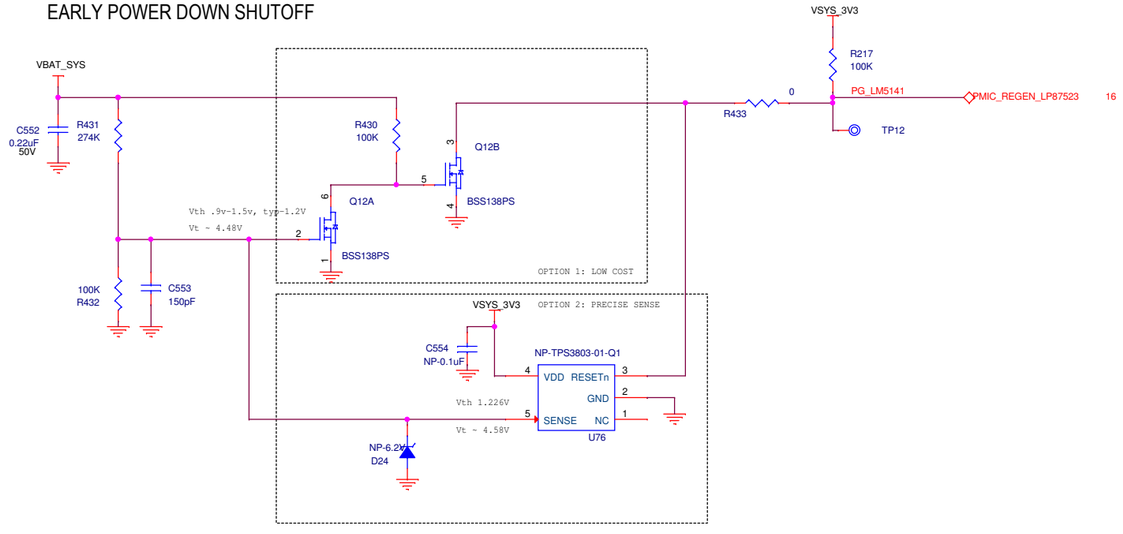
POWER WAKEUP BYPASS



CAN_POWER_ON_HV HIGH == VBAT_SYS.
CAN_POWER_ON_HV HAS 100K PULLDOWN AT CAN XCVR.

CAN_POWER_ON_HV HAS 2 STATES - HIGH, Z, CANNOT PULL LOW.

EARLY POWER DOWN SHUTOFF



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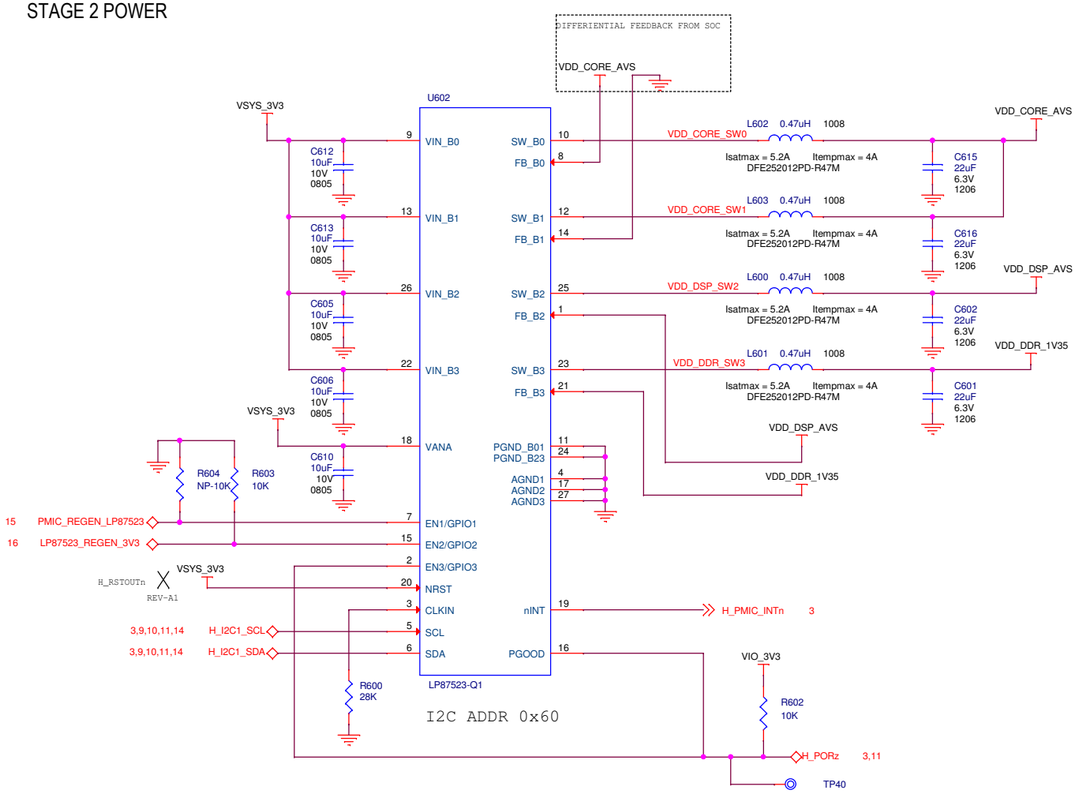
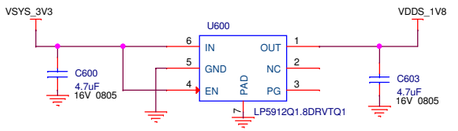
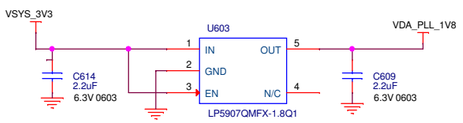
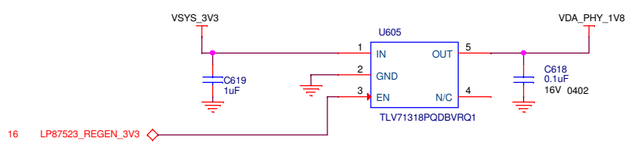
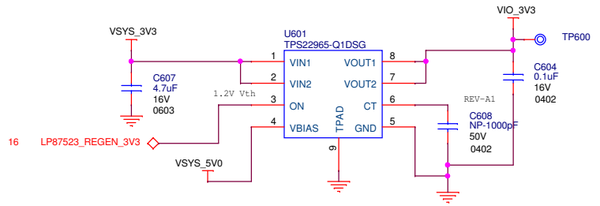
STAGE 2 POWER



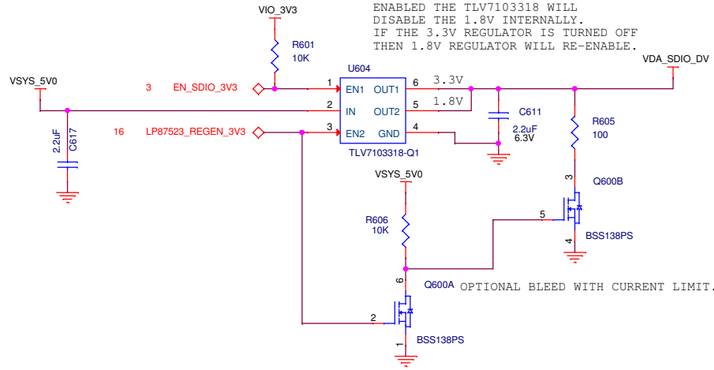


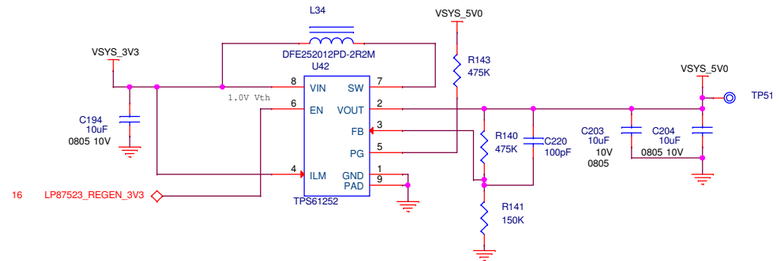






THE 1.8V REGULATOR IS ENABLED BY DEFAULT. IF THE 3.3V REGULATOR IS ENABLED THE TLV7103318 WILL DISABLE THE 1.8V INTERNALLY. IF THE 3.3V REGULATOR IS TURNED OFF THEN 1.8V REGULATOR WILL RE-ENABLE.





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Preliminary Information - Subject to change			
Title: DRA71x DCARD CPU Board			
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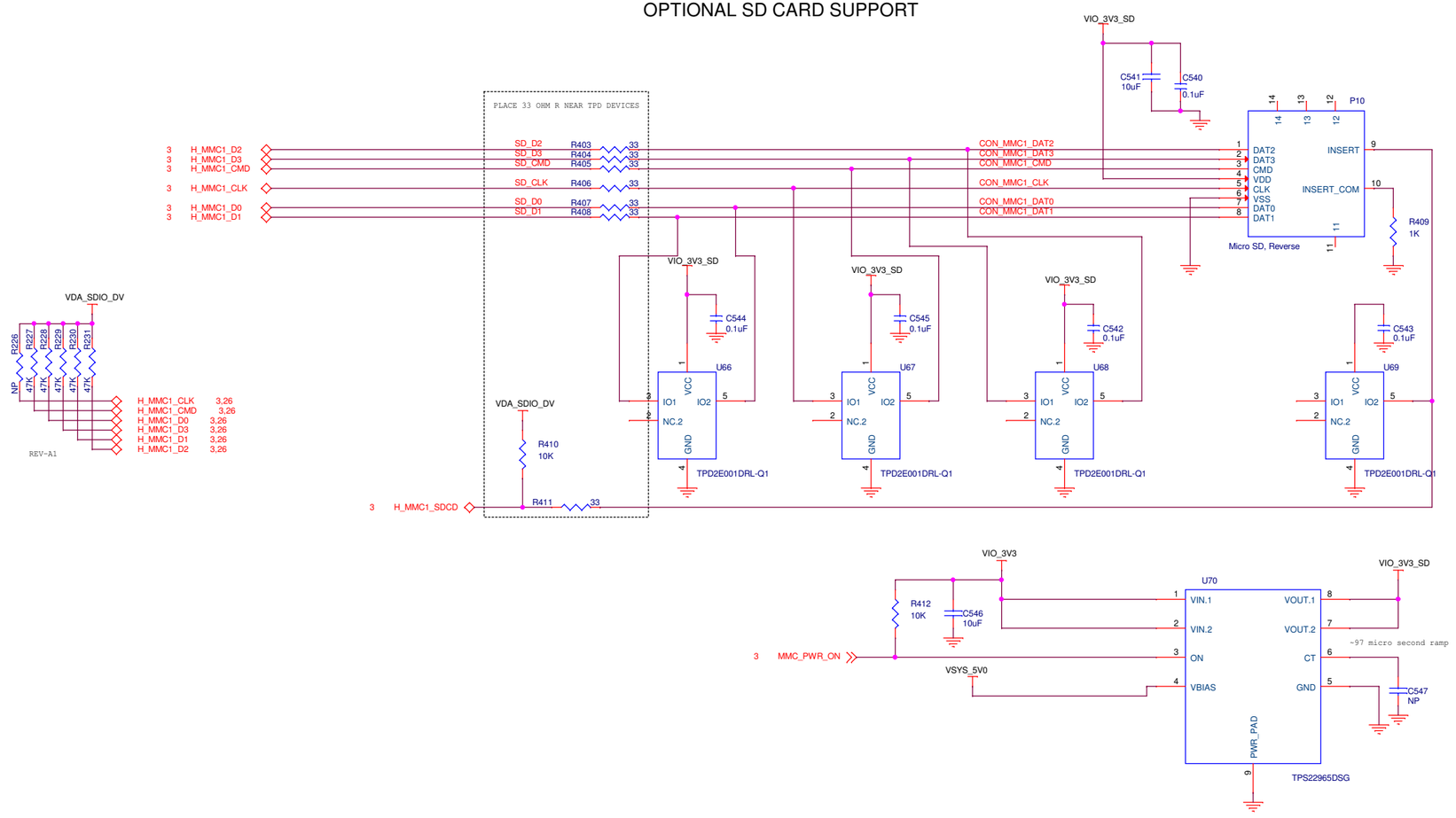
OPTIONAL SD CARD SUPPORT



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Title: DRA71x DCARD CPU Board		
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