TI Designs

10-W, 15 to 36-V Isolated Power Supply With ±15 V and 5 V for Analog PLC Modules

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TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00401	Design Folder
TIDA-00237	Tool Folder
LM5160	Product Folder
TPS7A4700	Product Folder
TPS7A4901	Product Folder
TPS7A3001	Product Folder
TPS70933	Product Folder

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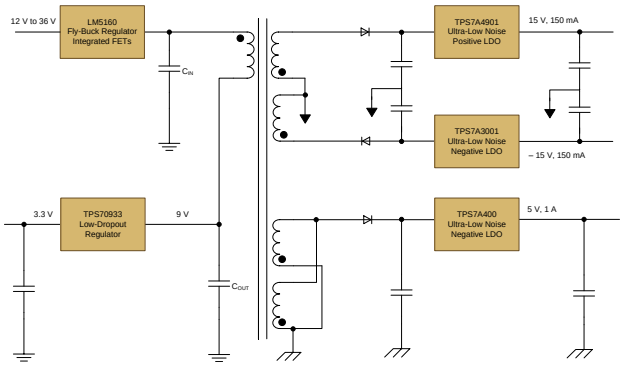
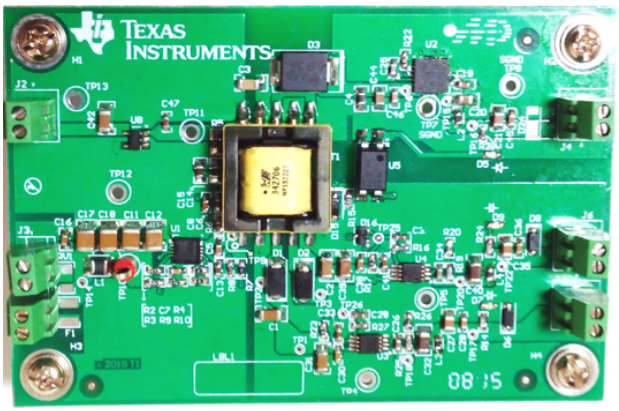
Design Features

- Wide Input Voltage Range: 15 to 36 V (24 V_{NOM})
- Three Isolated Outputs:
  - 15 V_{ISO} at 150-mA Ultra-Low Noise
  - –15 V_{ISO} at 150-mA Ultra-Low Noise
  - 5 V_{ISO} at 1 A
- ±5% Output Voltage Accuracy
- Low Profile < 10 mm
- Primary Side Regulation, No Need for Opto-coupler

Featured Applications

- PLC, DCS, and PAC:
  - Analog Input Module
  - Analog Output Module
  - CPU (PLC Controller)





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1 Key System Specifications

Table 1. Key System Specifications

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage	Normal operation	15	24	36	V
I_Q	Quiescent current	No output load	—	20	50	mA
V_{J4}	Output voltage connector J4	Normal operation	4.75	5	5.25	V
V_{J5}	Output voltage connector J5	Normal operation	14.25	15	15.75	V
V_{J6}	Output voltage connector J6	Normal operation	–14.25	–15	–15.75	V
I_{J4}	Output current	$V_{IN} > V_{IN(min)}$	0	—	1000	mA
I_{J5}	Output current	$V_{IN} > V_{IN(min)}$	0	—	150	mA
I_{J6}	Output current	$V_{IN} > V_{IN(min)}$	0	—	–150	mA
P_{OUT}	Output power	—	0	—	9.5	W
$V_{ISO(AC)}$	Isolation voltage	AC, 1 min	490	—	—	V
$V_{ISO(DC)}$	Isolation voltage	DC, 1 min	700	—	—	V
$V_{ISO(PERM)}$	Isolation voltage	DC, infinite min	70	—	—	V
η	Efficiency	V_{IN} = 15 V, P_{OUT} = max	—	65	—	%
		V_{IN} = 24 V, P_{OUT} = max	—	72	—	%
		V_{IN} = 36 V, P_{OUT} = max	—	64	—	%

2 System Description

A programmable logic controller (PLC) is a key component in factory automation. The PLC monitors input and output (I/O) modules in real-time and control the process according to the requirements. Thanks to flexible I/O modules, they can adapt too many different process requirements. The analog input and output modules, local or remote, acquire process data and set outputs to actuate the process. Figure 1 exhibits an analog input module with an emphasize on the power block.

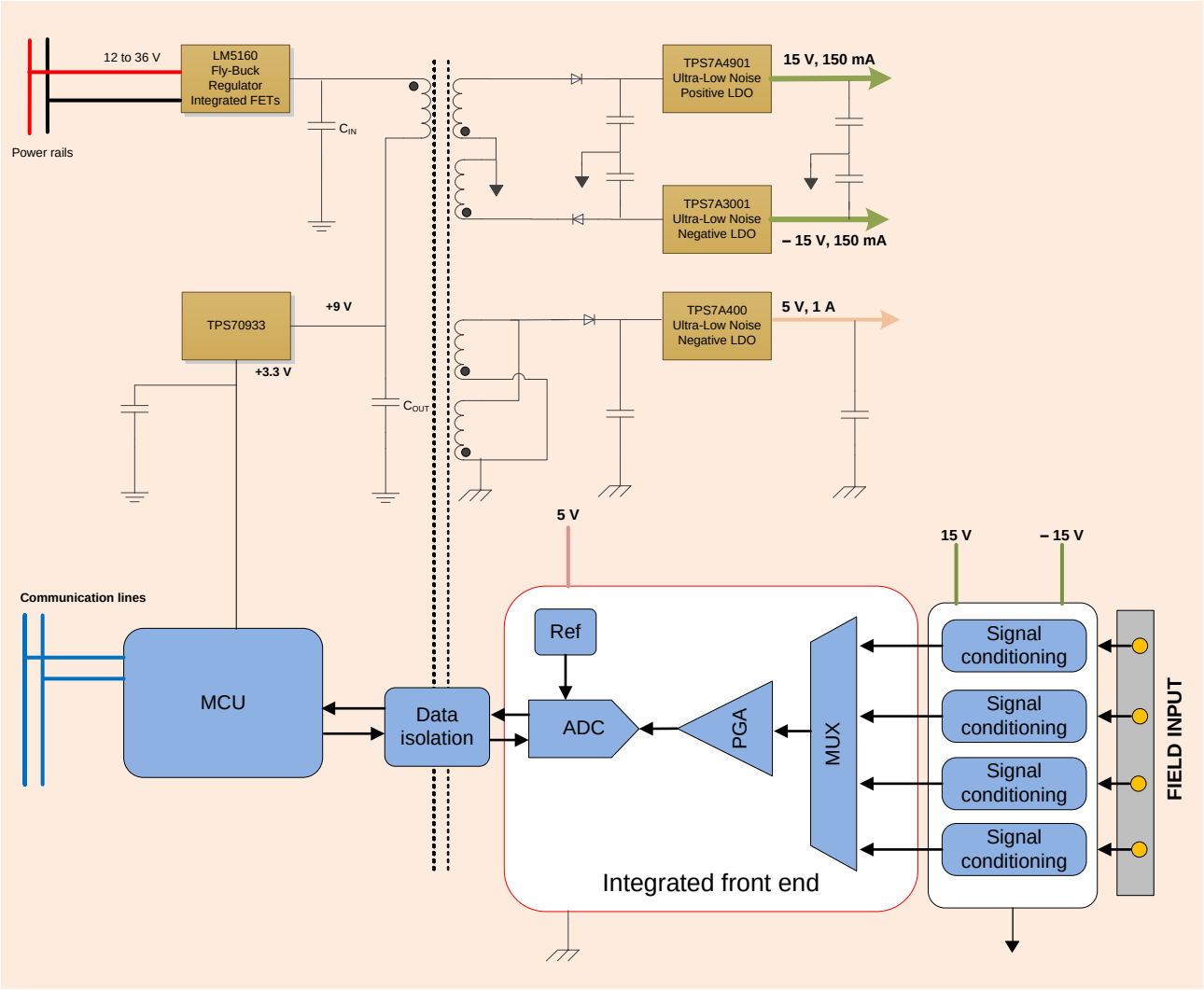


Figure 1. Generic Illustration of Analog Input Module

Analog input modules represent about 10% of all PLC I/O modules and analog output modules about 5%. Typical signaling are 4 to 20-mA current loop or ±10-V analog. The analog input and output modules use ADCs and DACs to convert analog process signals to digital values or vice versa in the output module.

A proper data conversion requires an ADC or DAC and potentially an amplifier stage to drive, level shift, filter, or impedance match the data converter to the input or output signal. To ensure the expected performance from the data converter and the amplifier stage, a dedicated low-noise isolated power supply solution is required, which is the main topic of the TIDA-00401. Figure 2 shows a block diagram of the design.

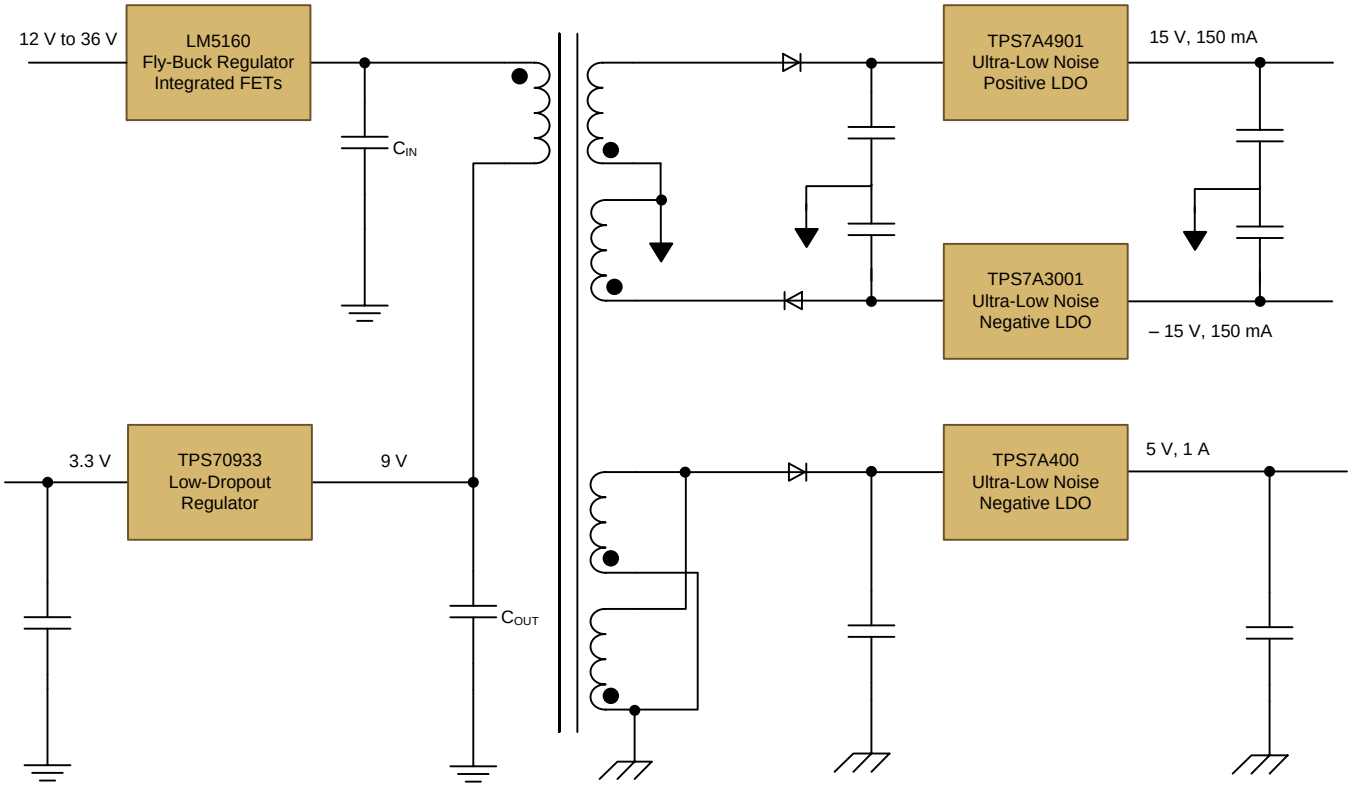


Figure 2. TIDA-00401 Isolated Power Supply Diagram for Analog Input Module

2.1 Highlighted Products

The TIDA-00401 provides the isolated analog and digital supply voltages for PLC analog input and output modules. For the analog section of the module TIDA-00401 generates 15 V and –15 V. These voltages are highly accurate and have minimal noise. An additional 5 V can be used as the digital supply for the data converter to supply a microcontroller or the isolation device.

2.1.1 LM5160

The LM5160 is a 65-V, 1.5-A synchronous step-down converter with integrated high-side and low-side MOSFETs. The constant-on-time control scheme requires no loop compensation and supports high step-down ratios with fast transient response. An internal feedback amplifier maintains ±1% output voltage regulation over the entire operating temperature range. The on-time varies inversely with input voltage resulting in nearly constant switching frequency. Peak and valley current limit circuits protect against overload conditions. The undervoltage lockout (EN/UVLO) circuit provides independently adjustable input undervoltage threshold and hysteresis. The LM5160 is programmed through the FPWM pin to operate in continuous conduction mode (CCM) from no load to full load or to automatically switch to discontinuous conduction mode (DCM) at light load for higher efficiency. Forced CCM operation supports multiple output and isolated Fly-Buck™ applications using a coupled inductor.

2.1.2 TPS7A4901

The TPS7A4901 is a positive, high-voltage (36 V), ultra-low noise (15.4-μV_{RMS}, 72-dB PSRR) linear regulator capable of sourcing a load of 150 mA.

This linear regulator includes a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A4901 is designed using bipolar technology and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes it an excellent choice to power operational amplifiers, ADCs, DACs, and other high-performance analog circuitry.

In addition, the TPS7A4901 is suitable for post DC/DC converter regulation. By filtering out the output voltage ripple inherent to DC/DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and radio frequency (RF) applications.

2.1.3 TPS7A3001

The TPS7A3001 is a negative, high-voltage (–36 V), ultra-low noise (15.1 μV_{RMS}, 72-dB PSRR) linear regulator capable of sourcing a maximum load of 200 mA.

This linear regulator includes a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A3001 is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes it an excellent choice to power operational amplifiers, ADCs, DACs, and other high-performance analog circuitry.

In addition, the TPS7A3001 is suitable for post DC/DC converter regulation. By filtering out the output voltage ripple inherent to DC/DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

2.1.4 TPS7A4700

The TPS7A4700 is a positive voltage (36 V), ultra-low noise (4 μV_{RMS}) low-dropout (LDO) linear regulator capable of sourcing a 1-A load.

The TPS7A4700 output voltages are user-programmable (up to 20.5 V) using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, thus reducing overall component count.

The TPS7A4701 output voltage can be configured with a user-programmable PCB layout (up to 20.5 V), or adjustable (up to 34 V) with external feedback resistors.

The TPS7A4700 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, ADCs, DACs, and other high-performance analog circuitry in critical applications such as medical, RF, and test and measurement.

In addition, the TPS7A4700 is ideal for post DC/DC converter regulation. By filtering out the output voltage ripple inherent to DC/DC switching conversions, maximum system performance is ensured in sensitive instrumentation, test and measurement, audio, and RF applications.

3 System Design Theory

For a 10-W isolated power supply with a wide input voltage range, no opto-coupler feedback, and low number of external components, the Fly-Buck topology is superior to a flyback design. This topology also allows design flexibility for a primary non-isolated power supply. For a high-end post regulation, LDOs with high PSRR are chosen to ensure a clean power supply for analog circuits. The 5-V rail is derived from the 6-V transformer output using a high efficiency LDO regulator. The Fly-Buck is implemented using an LM5160, which fulfils the Fly-Buck requirements, allows a small circuit footprint, and comes at a low BOM cost. Figure 3 shows the architecture of the LM5160.

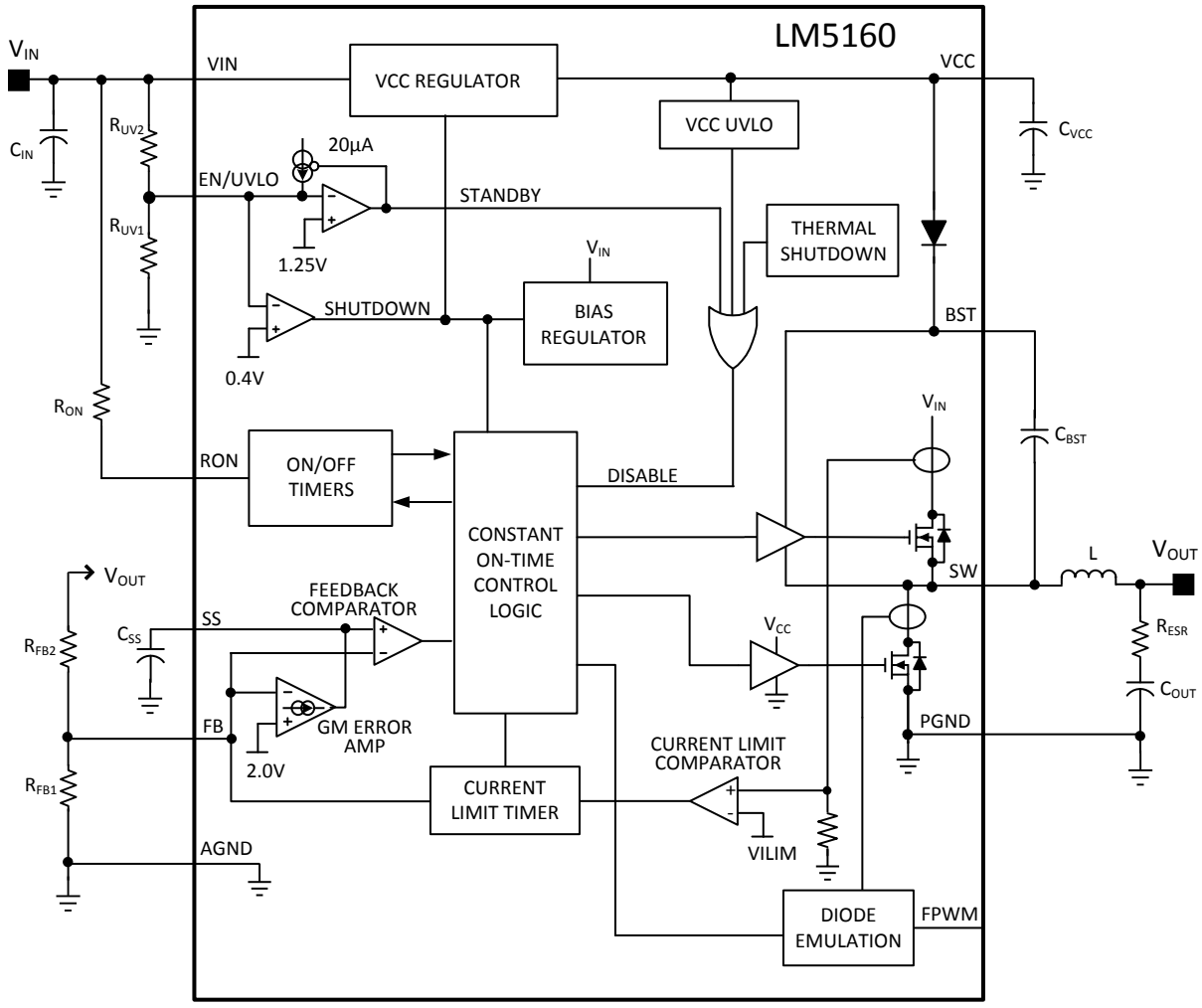


Figure 3. LM5160 Circuit Diagram

As most of the analog PLC I/O modules are space constrained, the TIDA-00401 aims at keeping the transformer T1 height below 9 mm and a small overall footprint. As the transformer has to be below a 9-mm height, an EFD15 core is the largest acceptable size for the required load demand.

3.1 Transformer Calculation

Figure 4 shows that for optimal performance, the frequency should be in the range of 150 to 450 KHz. Core loss is directly proportional to switching frequency. Also for lower frequency, the transformer size increases as required inductance increases. Therefore, to obtain the optimum transformer size and core loss, choose 300 KHz as the switching frequency.

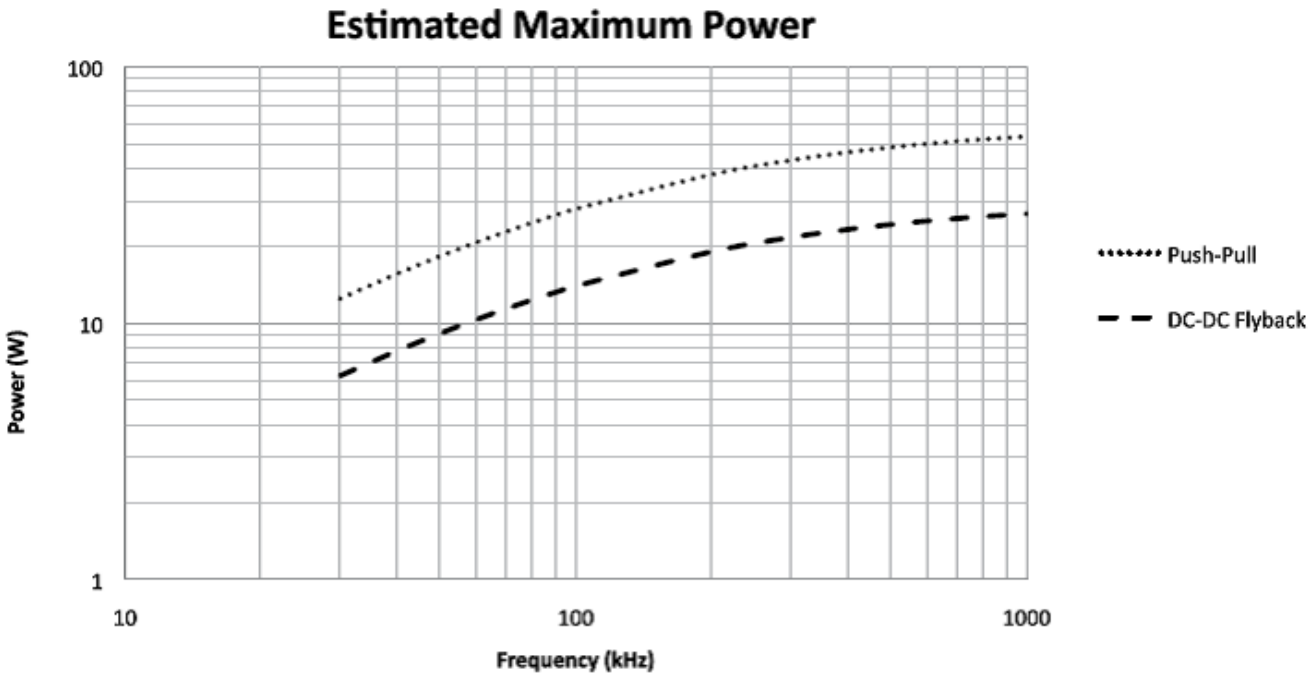


Figure 4. EFD15 Power versus Frequency Curve (Würth 070-5939)

The detailed calculation to verify the potential for correct operation is shown in Table 2.

Table 2. V_{J5}/V_{J6} Transformer T1 Voltage Calculation

PARAMETER	CONDITIONS	VALUE
V_{J5}/V_{J6}	Full load	15 V
LDO (U3, U4) drop-out voltage	150 mA, 25°C	0.6 V
Diode D1 and D2 drop-out voltage	Vf	0.5 V
Transformer T1, secondary winding loss	= R × I_{RMS} = 2 × 0.35	0.7 V
Required transformer T1, secondary winding voltage		16.8 V
Load regulation accuracy	$V_{IN(MIN)}$ to $V_{IN(MAX)}$	1.68 V (10%)
Required transformer T1, secondary winding voltage (including load reg.)	$V_{IN(MIN)}$ to $V_{IN(MAX)}$	18.48 ~ 20 V
Transformer T1, primary winding voltage	Winding ratio 1:2.04 with respect to 20 V	9.80 V
Transformer T1, primary winding loss	= R × I_{RMS} = 0.065 × 1.57	–0.1V
U1 synchronous switch loss	Low-side FET R_{ON} 0.13 V = I_{RMS} × 0.13 = 1.57 × 0.13	–0.2 V
Required V_{C1} voltage	Average	9.5 V
$V_{IN(MIN)}$ duty cycle	$V_{IN(MIN)}$ = 15 V $V_{C1(MIN)}$ = 9.5 V	63.30%

NOTE: The average current while the synchronous switch is on is a simulated value.

As per fundamentals of the transformer, input power is same as output power. Considering outputs of 18 V, –18 V at 150 mA, and 6 V at 1 A, the total output power is 11.4 W. Therefore, for 11.4 W, the primary current will be:

$$I_{DC} = \frac{P_{tot}}{V_{C1}} + I_{OUTPRIMARY_{3.3V}} \quad (1)$$

$$\Delta I = I_{DC} \times \text{Ripple factor} \quad (2)$$

$$I_{PEAK} = I_{DC} + \frac{\Delta I}{2} \quad (3)$$

So I_{DC} for 9.5 V and 11.4 W, power is 1.2 A. Considering a ripple factor of 0.4, the ripple current will be 0.48 A.

The I_{PEAK} max peak current using Equation 3 is 1.5 A considering 0.05 mA as $I_{OUTPRIMARY\_3.3V}$.

So I_{PEAK} is less than 2.125 A (minimum of high-side FET in specification of LM5160).

Primary inductance is given by

$$L_{PRIM} = \frac{V_{C1} \times \left(V_{IN(MAX)} - V_{C1}\right)}{V_{IN(MAX)} \times F_{SW} \times I_{PEAK} \times 0.4} \quad (4)$$

So L_{PRIM} computes to 38.3 µH.

Considering a 10% tolerance, the next standard value is 47 µH. Therefore, the primary inductance of T1 is 47 µH.

Duty cycle is given as

$$D_{MAX} = \frac{V_{OUTPUTPRIMARY}}{V_{MINIMUM}} = \frac{9.5}{15} = 0.63 \quad (5)$$

$$D_{MIN} = \frac{V_{OUTPUTPRIMARY}}{V_{MAXIMUM}} = \frac{9.5}{36} = 0.26 \quad (6)$$

As the LM5160 is the constant frequency driver, the on-time will vary from 2.1 µs to 866 ns for an input range of 15 to 36 V.

The standard equation for magnetic design:

$$B_{\text{flux density}} = \frac{P_{\text{core loss}}}{V_{\text{core volume}} \times K_{fe}} \tag{7}$$

$$N_{\text{turns requiered}} = \frac{L_{\text{inductance}} \times I_{PEAK}}{A_{\text{core sectional area}} \times B_{\text{flux density}}} \tag{8}$$

$$d_{\text{wire diameter}} = \sqrt{\frac{4 \times I_{PEAK}}{J_{\text{current density}} \times \pi}} \tag{9}$$

$$\frac{N_{\text{secondary turns}}}{N_{\text{primary turns}}} = \frac{V_{\text{secondary}}}{V_{\text{primary}}} \tag{10}$$

For a detailed magnetic design, see the TI Magnetic design handbook by Lloyd H Dixon.

3.2 Buck Output Capacitors

Select an output capacitor to reduce ripple in the output voltage.

$$C_{OUT,pri} = \frac{I_{L,ripple(max)}}{8 \times F_{SW} \times V_{ripple}} \tag{11}$$

Considering a ripple of 10 mV gives a capacitor value of 20.5 µF.
So C14, C15, and C47 compute to 21 µF.

The ESR of capacitor is given as follows:

$$R_{ESR} > \frac{25\ \text{mV} \times V_{C1}}{V_{REF} \times I_{L,ripple(max)}} \tag{12}$$

So ESR of capacitor should be greater than 0.24 Ω.

3.3 Isolated Output Capacitors

Isolated capacitors need to reduce ripples as well as store energy for supply during negative cycle of conduction.

$$I = C\frac{dV}{dT} \tag{13}$$

$$dT = \frac{VC1}{V_{IN(MIN)}} \times \frac{1}{F_{SW}} = 2.75\ \mu s \tag{14}$$

Considering dV of 0.1 V, the output capacitor of 18-V isolated output is

$$C > \frac{0.15 \times 2.75 \times 10^{-6}}{0.1} = 4.1\ \mu F \tag{15}$$

The next standard value is 4.7 µF.

3.4 Input Capacitors

The input capacitor should be quite large to minimize input ripple to acceptable value.

$$C_{IN} > \frac{I_{O,max} \times T_{ON(MAX)}}{0.5\ V} \tag{16}$$

For C_{IN} to be greater than 8.47 µF, C11 and C12 of 10 µF have been connected in parallel of the input side of the LM5160.

3.5 Feedback Resistors

The feedback resistor network calculates as per the following formulas. Resistor R_{FB1} is set to 2.7 kΩ, resulting in a divider current of ~0.6 mA or a power loss of 10 mW. If the design is located in a noise-free environment, a smaller divider current could be selected. For an industrial design, however, 2 kΩ is a good starting point.

$$V_{OUT} = V_{FB} \times \left(\frac{R_{FB2}}{R_{FB1}} + 1 \right) = 2\ V \times \left(\frac{R8}{R6} + 1 \right) \quad (17)$$

R8 = 10 kΩ and R6 = 2.7 kΩ are chosen to respect standard resistor values.

3.6 Operating Switching Frequency

From Section 3.1, the switching frequency was determined with 300 kHz. R_{ON} sets the nominal switching frequency based on the following equations:

$$\frac{R8}{R6} = \frac{9.5\ V}{2\ V} - 1 = 3.75 \quad (18)$$

$$F_{SW} = \frac{V_{C1}}{10^{-10} \times R_{ON}} \quad (19)$$

The next closest standard resistor value is 330 kΩ.

3.7 Output Ripple Configuration

The LM5160 uses a constant on-time control scheme, which requires an appropriate voltage ripple of > 25 mV at the feedback node.

This design uses Type 3 configuration, which injects ripples current in R_r and C_r and switch node voltage to generate triangular ramp. It is then AC coupled using C_{ac} to the feedback node.

The purpose of adding compensation to the error amplifier is to counteract some of the gains and phases contained in the control-to-output transfer function that could jeopardize the stability of the power supply.

The Type 3 compensator is used to have more than 90 degrees of phase boost.

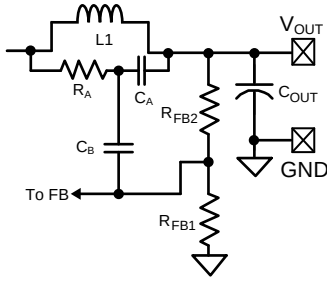


Figure 5. Typical Noise Amplification Scheme

$$R_{ON} = \frac{V_{C1}}{10^{-10} \times F_{SW}} \quad (20)$$

Assuming C_r to be 2200 pF, R_r is 64.8 KΩ, which can be rounded to 100 KΩ.
A 0.1-µF capacitor can be used as C_{ac} in ripple circuit.

3.8 EN/UVLO Resistors

The UVLO resistors R3 and R9 set the input UVLO threshold and hysteresis according to the following equations:

$$R_{ON} = \frac{9.5\ V}{10^{-10}\ A \times 300000} = 300\ k\Omega \quad (21)$$

Considering V_{HYS} as 2 V, R3 is 100K.

$$RrCr \leq \frac{\left(V_{IN(MIN)} - V_{OUT}\right) \times T_{ON}}{25\ mV} \quad (22)$$

Considering 9 V as the undervoltage rising voltage gets R9 as 16K. The next standard value is 18.2K. Thus, R3 is 100K and R9 is 18.2K.

3.9 Soft-Start Time

The capacitor at the SS pin determines the soft-start time (that is, the time for the output voltage to reach its final steady state value). The capacitor C7 value is 22 nF considering 4 ms as T_{SS}

$$V_{HYS} = 20 \times 10^{-6} \times R3 \quad (23)$$

4 Getting Started Hardware

The design can be operated directly out of the box. Load resistors with a power rating of at least 5 W can be connected directly to the output terminals. For performing a maximum power test use 100 Ω on the 15-V (J5) and –15-V (J6) terminals and 5 Ω for the 5-V output (J4). I_{J5} and I_{J6} will settle to 150 mA and I_{J4} to 1 A.

5 Test Setup

This design is tested for a minimum input voltage of 15 V ($V_{IN(MIN)}$) and maximum of 36 V ($V_{IN(MAX)}$). Output currents are hereby set to 0, 50, 100, and 150 mA for the ±15-V outputs symmetric as well as asymmetric. The 5-V output is loaded with 0 mA, 250 mA, 500 mA, and 1 A either at the same time with ±15 V or individually. Startup behavior is checked with 100% load.

Table 3. Test Results

INPUT VOLTAGE (V) V_{IN}	OUTPUT CURRENT (mA) I_{J4}, I_{J5}, I_{J6}	LOADED OUTPUTS	OUTPUT VOLTAGES (V)		
			V_{J4}	V_{J5}	V_{J6}
15	0	None	5.172	14.99	–14.85
24			5.172	14.99	–14.85
36			5.172	14.99	–14.85
15	250	J4 only	5.164	14.99	–14.84
	50	J5 only	5.172	14.84	–14.84
	50	J6 only	5.172	14.99	–14.84
	350	All	5.164	14.84	–14.84
	500	J4 only	5.162	14.99	–14.85
	100	J5 only	5.172	14.84	–14.84
	100	J6 only	5.172	14.99	–14.84
	700	All	4.930	14.62	–14.84
	1000	J4 only	4.054	14.99	–14.85
	150	J5 only	5.172	14.84	–14.84
	150	J6 only	5.172	14.99	–14.84
	1300	All	3.730	14.36	–14.81
24	250	J4 only	5.166	14.99	–14.84
	50	J5 only	5.172	14.84	–14.84
	50	J6 only	5.172	14.99	–14.84
	350	All	5.166	14.84	–14.84
	500	J4 only	5.161	14.99	–14.85
	100	J5 only	5.172	14.84	–14.84
	100	J6 only	5.172	14.99	–14.84
	700	All	5.161	14.62	–14.84
	1000	J4 only	5.084	14.99	–14.85
	150	J5 only	5.172	14.84	–14.84
	150	J6 only	5.172	14.99	–14.84
	1300	All	4.895	14.50	–14.84
36	250	J4 only	5.168	14.99	–14.84
	50	J5 only	5.172	14.84	–14.84
	50	J6 only	5.172	14.99	–14.84
	350	All	5.168	14.84	–14.84
	500	J4 only	5.163	14.99	–14.85
	100	J5 only	5.172	14.84	–14.84
	100	J6 only	5.172	14.99	–14.84
	700	All	5.161	14.62	–14.84
	1000	J4 only	5.144	14.99	–14.85
	150	J5 only	5.172	14.84	–14.84
	150	J6 only	5.172	14.99	–14.84
	1300	All	5.140	14.40	–14.84

6 Test Results

6.1 Startup and Shutdown

The following plots reflect the design behavior during startup and shutdown mode at full load conditions.

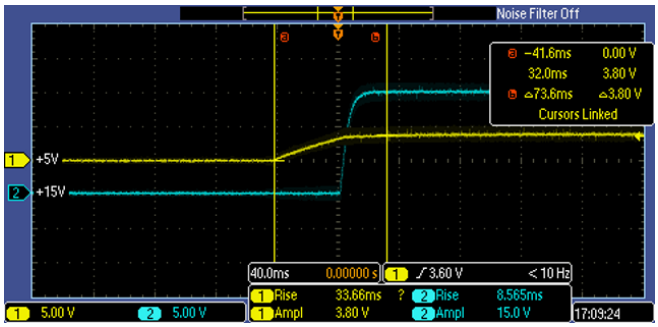


Figure 6. Startup of V_{J5} = 15 V at V_{IN} = 15 V

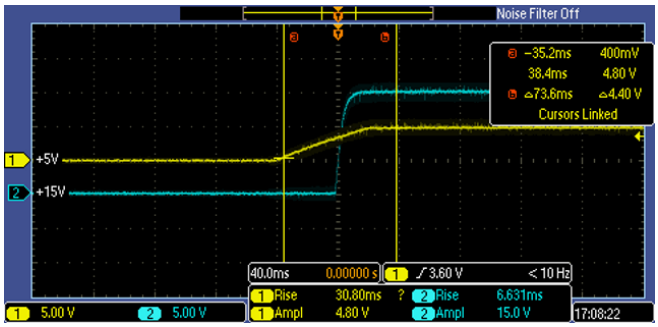


Figure 7. Startup of V_{J5} = 15 V at V_{IN} = 24 V

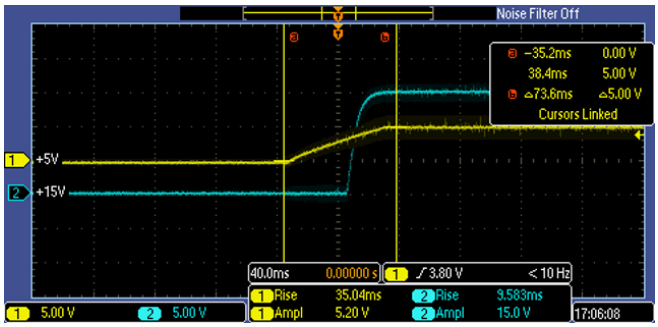


Figure 8. Startup of V_{J5} = 15 V at V_{IN} = 36 V

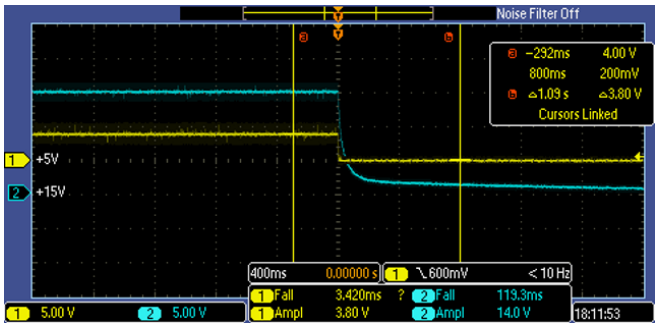


Figure 9. Shutdown of at V_{IN} = 15 V

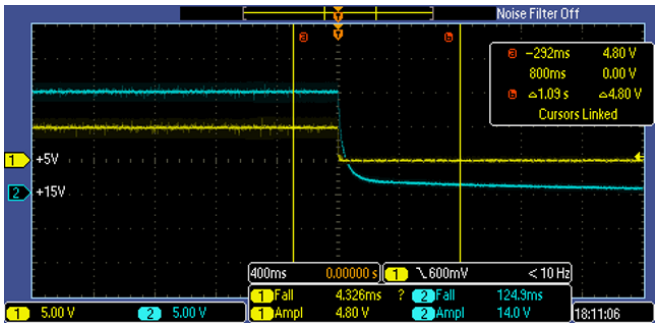


Figure 10. Shutdown at V_{IN} = 24 V

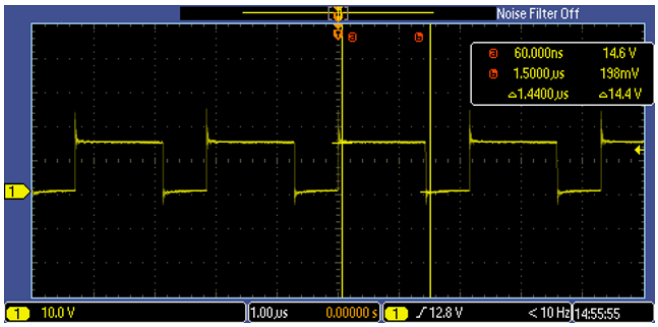


Figure 11. Switching at V_{IN} = 15 V

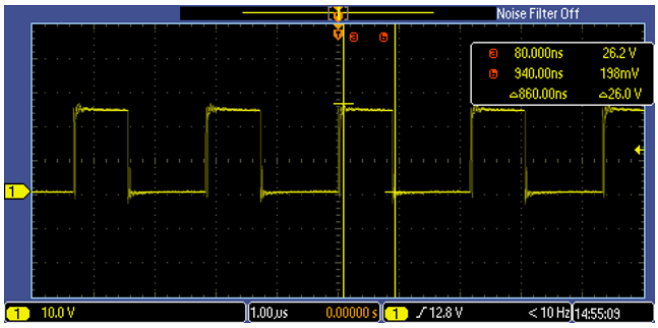


Figure 12. Switching at V_{IN} = 24 V

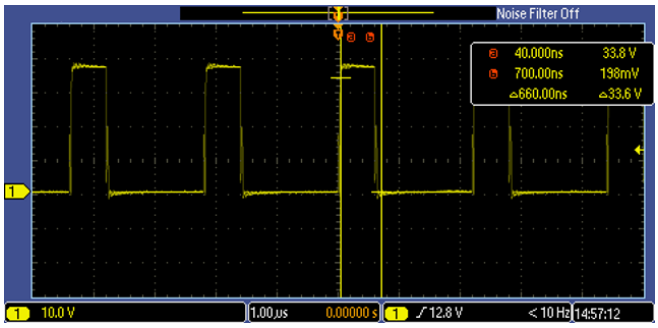


Figure 13. Switching at V_{IN} = 36 V

6.2 Efficiency

Input current at 24 V ($V_{IN(NOM)}$) is measured as 534 mA under full load. This corresponds to an input power of 12.8 W. The output power (P_{OUT}) at full load is 9 W. This results in efficiency of 70%.

Figure 14 shows the efficiency depending on input voltage, V_{IN}. Due to the post regulation with LDOs the efficiency peak comes at $V_{IN(NOM)}$ 24 V. The isolating converter has a line voltage dependency with regards to its output voltage. At higher input voltages, the output voltage increases, and as a consequence, the voltage drops are larger at the LDOs. This causes an efficiency loss at higher input voltages.

The effect could be mitigated by using a larger form factor transformer with a higher inductance and tighter coupling between the primary and secondary windings or by using buck regulators instead of LDO. By specifying a tighter $V_{IN(MIN)}$ to $V_{IN(MAX)}$ range, the regulation could be improved so that a smaller voltage drop at the LDOs could be used.

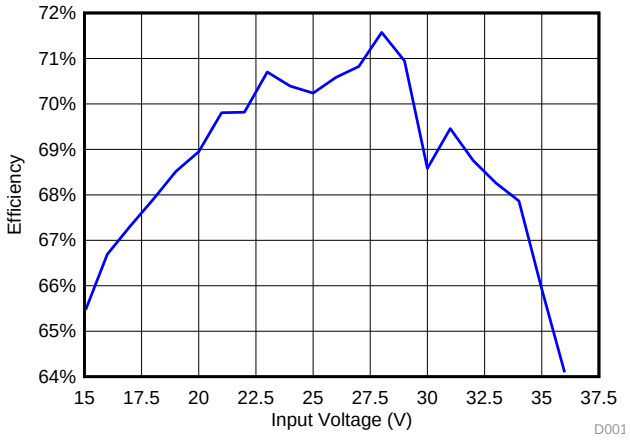


Figure 14. Overall Efficiency versus Input Voltage

6.3 Load and Line Regulation

Table 3 shows that the output voltages are not much affected by different load and line conditions. This is the effect of the post regulation using precision LDOs.

6.4 Thermal Analysis

Figure 15 and Figure 16 have been captured with a FLUKE Ti400 at 25°C. The scale in the two figures has been adjusted so that the color coding matches.

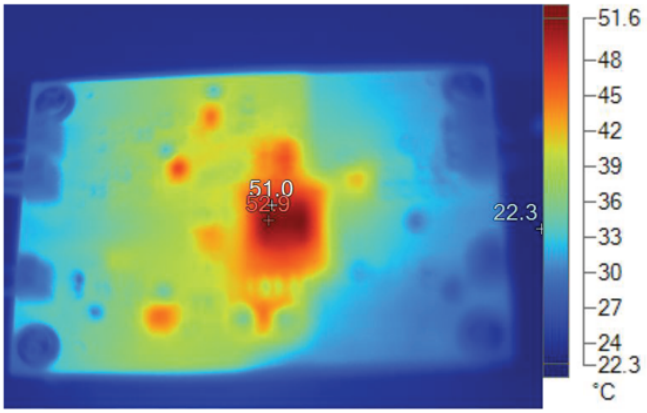


Figure 15. TIDA-00401 Thermal Analysis Full Load

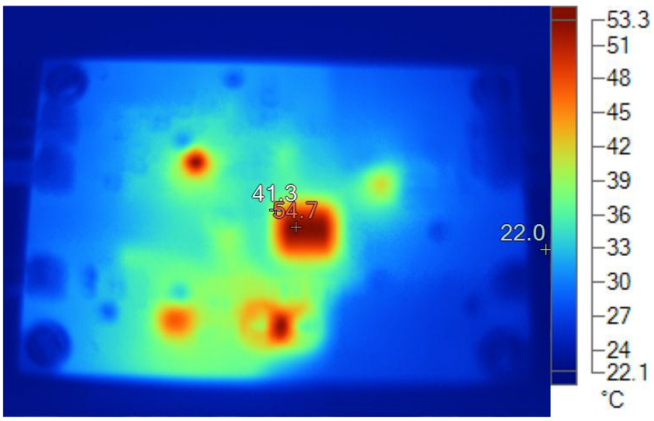


Figure 16. TIDA-00401 Thermal Analysis 50% Load

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00401.

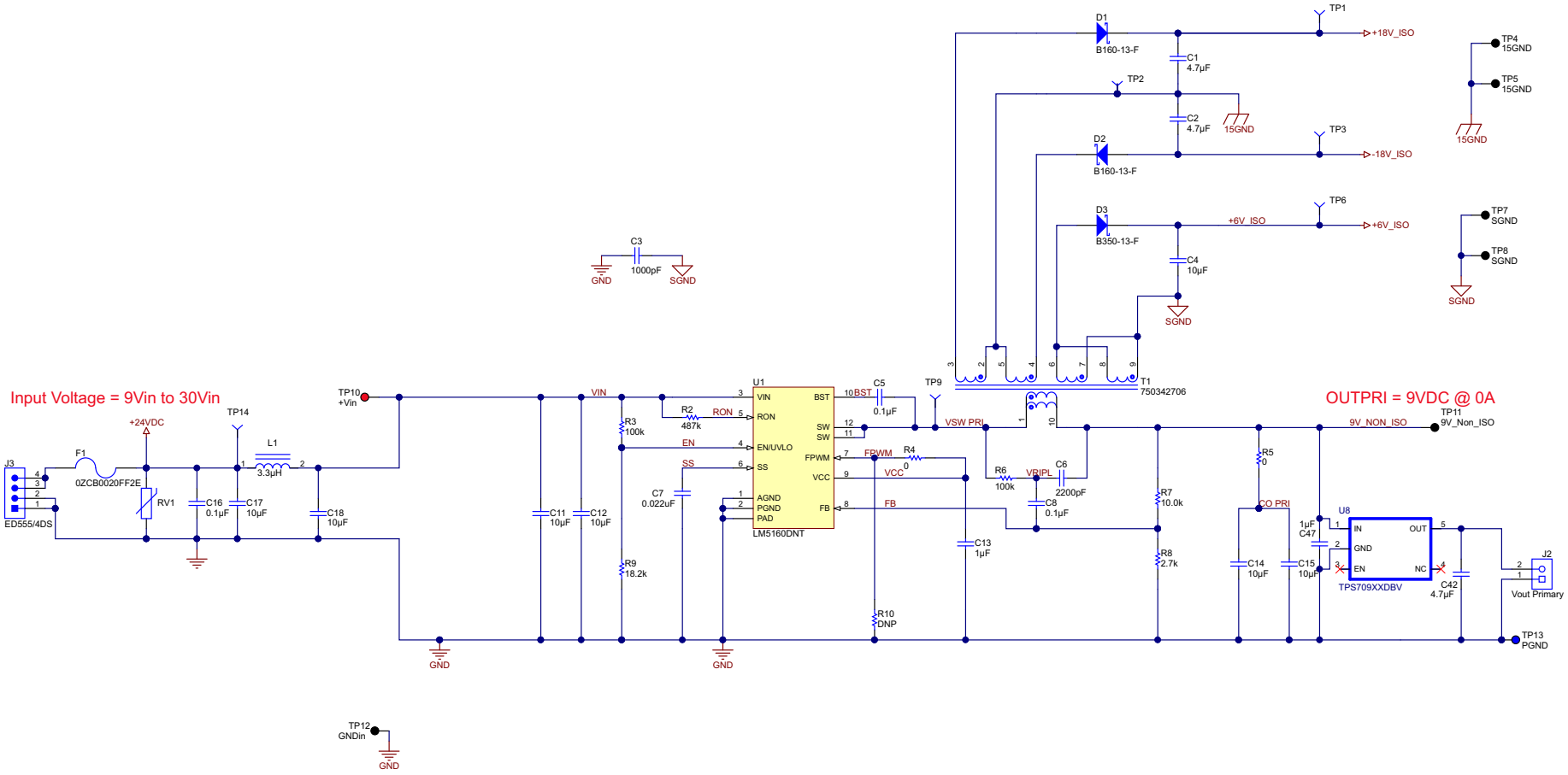


Figure 17. LM5160 Fly-Buck-Boost Page 1

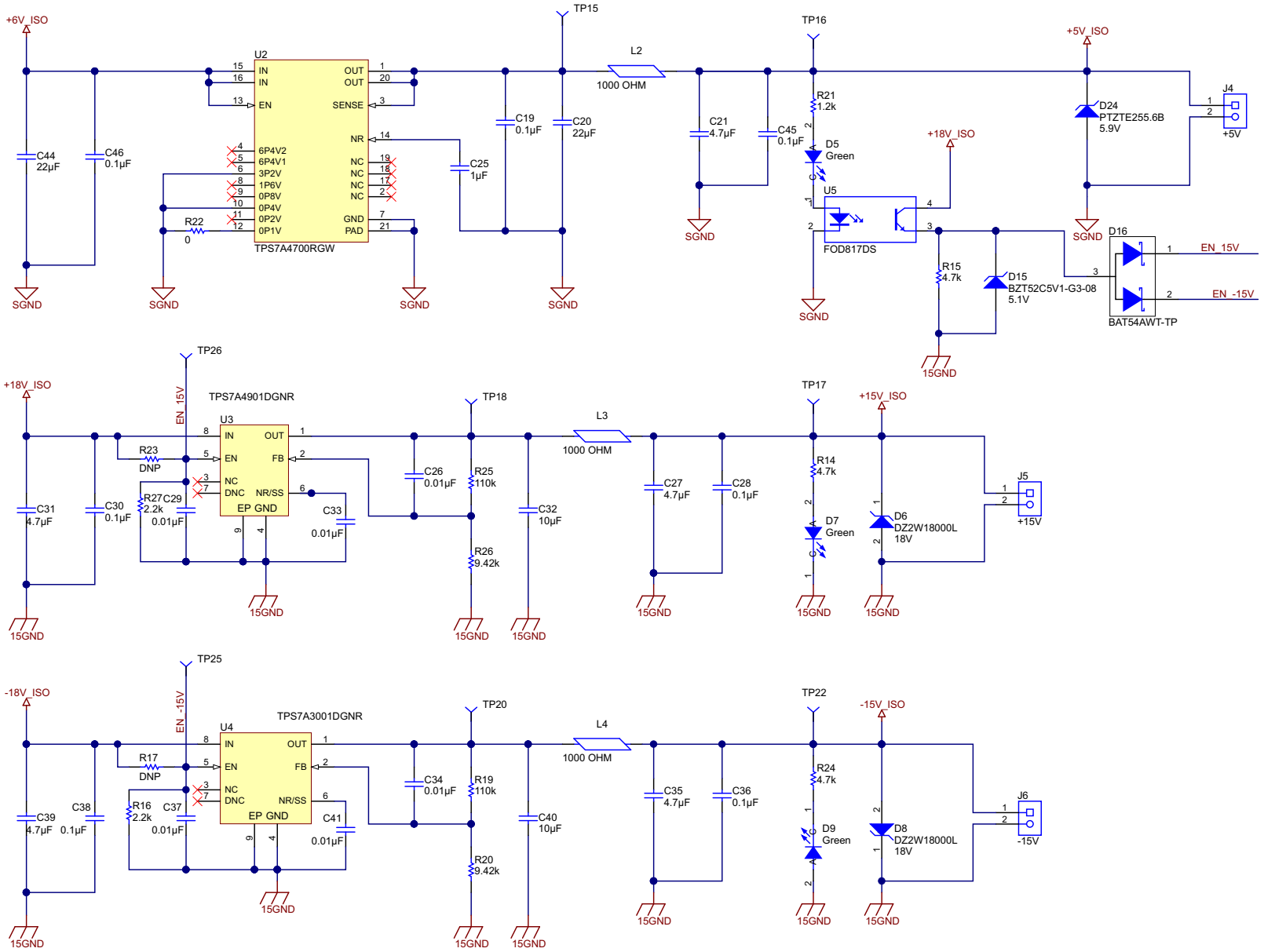


Figure 18. LM5160 Fly-Buck-Boost Page 2

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00401.

Table 4. TIDA-00401 BOM

ITEM	QTY	REFERENCE	DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
1	1	PCB1	Printed Circuit Board	Any	TIDA-00401	
2	5	C1, C2, C31, C39, C42	CAP, CERM, 4.7uF, 50V, +/-10%, X7R, 1206	MuRata	GRM31CR71H475KA12L	1206
3	1	C3	CAP, CERM, 1000pF, 1000V, +/-5%, C0G/NP0, 1206	Vishay-Vitramon	VJ1206A102JXGAT5Z	1206
4	3	C4, C14, C15	CAP, CERM, 10uF, 16V, +/-10%, X5R, 0805	Taiyo Yuden	EMK212BJ106KG-T	0805_HV
5	2	C5, C8	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	Kemet	C0603C104J3RAC	0603
6	1	C6	CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603	Kemet	C0603C222K5RAC	0603
7	1	C7	CAP, CERM, 0.022uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C223KA01D	0603
8	4	C11, C12, C17, C18	CAP, CERM, 10uF, 50V, +/-10%, X7R, 1210	MuRata	GRM32ER71H106KA12L	1210
9	1	C13	CAP, CERM, 1uF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E105KA12D	0603
10	1	C16	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0805	Kemet	C0805C104K1RACTU	0805
11	7	C19, C28, C30, C36, C38, C45, C46	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	AVX	06035C104KAT2A	0603
12	2	C20, C44	CAP, CERM, 22uF, 16V, +/-20%, X5R, 0805	MuRata	GRM21BR61C226ME44	0805_HV
13	3	C21, C27, C35	CAP, CERM, 4.7uF, 50V, +/-10%, X5R, 0805	TDK	C2012X5R1H475K125AB	0805_HV
14	1	C25	CAP, CERM, 1uF, 25V, +/-10%, X7R, 0603	TDK	C1608X7R1E105K080AB	0603
15	6	C26, C29, C33, C34, C37, C41	CAP, CERM, 0.01uF, 100V, +/-5%, X7R, 0603	AVX	06031C103JAT2A	0603
16	2	C32, C40	CAP, CERM, 10uF, 25V, +/-10%, X7R, 1206	MuRata	GRM31CR71E106KA12L	1206
17	1	C47	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603	Taiyo Yuden	EMK107B7105KA-T	0603
18	2	D1, D2	Diode, Schottky, 60 V, 1 A, SMA	Diodes Inc.	B160-13-F	SMA
19	1	D3	Diode, Schottky, 50 V, 3 A, SMC	Diodes Inc.	B350-13-F	SMC

Table 4. TIDA-00401 BOM (continued)

ITEM	QTY	REFERENCE	DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
20	3	D5, D7, D9	LED SmartLED Green 570NM	OSRAM	LG L29K-G2J1-24-Z	LED0603AA
21	2	D6, D8	Diode, Zener, 18V, 1W, SOD-123	Panasonic	DZ2W18000L	SOD-123
22	1	D15	Diode, Zener, 5.1 V, 500 mW, SOD-123	Vishay-Semiconductor	BZT52C5V1-G3-08	SOD-123
23	1	D16	Diode, Schottky, 30 V, 0.2 A, SOT-323	Micro Commercial Components	BAT54AWT-TP	SOT-323
24	1	D24	DIODE ZENER 5.9V 1W PMDS	Rohm Semiconductor	PTZTE255.6B	powerDI123
25	1	F1	PTC RESTTBLE 0.05A 60V CHIP 1210	Bel Fuse Inc	0ZCB0020FF2E	1210
26	3	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial10-20
27	4	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	NY PMS 440 0025 PH
28	4	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	Keystone_1902C
29	1	J2	Conn Term Block, 2POS, 3.81mm, TH	Phoenix Contact	1727010	PhoenixConact_1727010
30	1	J3	Terminal Block, 6A, 3.5mm Pitch, 4-Pos, TH	On-Shore Technology	ED555/4DS	TERM_BLK_ED555-4DS
31	1	J4	Conn Term Block, 2POS, 3.81mm, TH	Phoenix Contact	1727010	PhoenixConact_1727010
32	1	J5	Conn Term Block, 2POS, 3.81mm, TH	Phoenix Contact	1727010	PhoenixConact_1727010
33	1	J6	Conn Term Block, 2POS, 3.81mm, TH	Phoenix Contact	1727010	PhoenixConact_1727010
34	1	L1	Inductor, Chip, ±10%	EPCOS INC.	B82422H1332K	IND_B82422H
35	3	L2, L3, L4	FERRITE CHIP 1000 OHM 1500MA 0805, FERRITE CHIP 1000 OHM 300MA 0603, FERRITE CHIP 1000 OHM 300MA 0603	TDK Corporation	MPZ2012S102AT000, MMZ1608B102C, MMZ1608B102C	FB0603
36	1	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	Label_650x200
37	1	R2	RES, 487k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603487KFKEA	0603
38	2	R3, R6	RES, 100 k, 1%, 0.1 W, 0603, RES, 100k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100KFKEA	0603
39	5	R4, R10, R17, R22, R23	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603
40	1	R5	RES, 0, 5%, 0.125 W, 0805	Vishay-Dale	CRCW08050000Z0EA	0805_HV
41	1	R7	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	0603
42	1	R8	RES, 2.7 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06032K70JNEA	0603
43	1	R9	RES, 18.2k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060318K2FKEA	0603
44	3	R14, R15, R24	RES, 4.7k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06034K70JNEA	0603
45	2	R16, R27	RES, 2.2 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06032K20JNEA	0603
46	2	R19, R25	RES, 110k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW0402110KFKED	0603

Table 4. TIDA-00401 BOM (continued)

ITEM	QTY	REFERENCE	DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
47	2	R20, R26	RES, 9.42k ohm, 1%, 0.063W, 0402	Vishay-Dale	TNPW04029K42BEED	0603
48	1	R21	RES, 1.2k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04021K20JNED	0402
49	1	RV1	VARISTOR 36.9V 30A 0805	AVX	VC080530A650DP	1206
50	1	T1	Transformer, 50 uH, SMT	Wurth Elektronik eiSos	750342706	TR_750342706
51	11	TP1, TP2, TP3, TP6, TP9, TP14, TP15, TP18, TP20, TP25, TP26	Test Point 40mil pad 20mil drill	STD	STD	TP1_PD40_D0.5_S50
52	2	TP4, TP5	Test Point, Multipurpose, Black, TH	Keystone	5011	Keystone5011
53	2	TP7, TP8	Test Point, Multipurpose, Black, TH	Keystone	5011	Keystone5011
54	1	TP10	Test Point, Multipurpose, Red, TH	Keystone	5010	Keystone5010
55	1	TP11	Test Point, Multipurpose, Black, TH	Keystone	5011	Keystone5011
56	1	TP12	Test Point, Multipurpose, Black, TH	Keystone	5011	Keystone5011
57	1	TP13	Test Point, Multipurpose, Blue, TH	Keystone	5127	Keystone5127
58	3	TP16, TP17, TP22	Test Point 40mil pad 20mil drill	STD	STD	TP1_PD40_D0.5_S50
59	1	U1	Wide Input 65V, 1.5A Synchronous Step-Down DC-DC Converter, DNT0012B	Texas Instruments	LM5160DNT	DNT0012B
60	1	U2	36-V, 1-A, 4.17-µVRMS, RF LDO Voltage Regulator, RGW0020A	Texas Instruments	TPS7A4700RGW	RGW0020A
61	1	U3	Single Output High PSRR LDO, 150 mA, Adjustable 1.2 to 33 V Output, 3 to 36 V Input, with Ultra-Low Noise, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS7A4901DGNR	DGN0008D_N
62	1	U4	Single Output High PSRR LDO, 200 mA, Adjustable -1.18 to -33 V Output, -3 to -36 V Input, with Ultra-Low Noise, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS7A3001DGNR	DGN0008D_N
63	1	U5	Optocoupler, 5kV RMS, SMT	Fairchild Semiconductor	FOD817DS	N04C
64	1	U8	IC,150mA, Ultra Low IQ, 1uA LDO Regulator with Enable	TI	TPS709xxDBV	DBV-5

7.3 PCB Layout Recommendations

The PCB layout recommendation is driven by low EMI and good thermal performance. The layout has been implemented on a two-layer board with 35-µm copper. Each IC is provided enough copper heat sink area in order to limit the device temperature below 85°C.

Figure 19 shows the switch current path during t_{OFF} and t_{ON} phases of the buck converter. During t_{ON} the current takes the Paths 1, 2, 3 and 4 from capacitors C11 and C12. The loop area of switch current during t_{ON} should be minimized to reduce EMI.

During t_{OFF} the current takes Paths 3 and 4 from T1 primary winding. The loop area of switch current during t_{OFF} should be minimized to reduce EMI. The bootstrap capacitor C5 should be as close as possible to U1 to prevent unwanted glitches in switching of U1. The layout shows as an example how to achieve reduced EMI and thermal resistance.

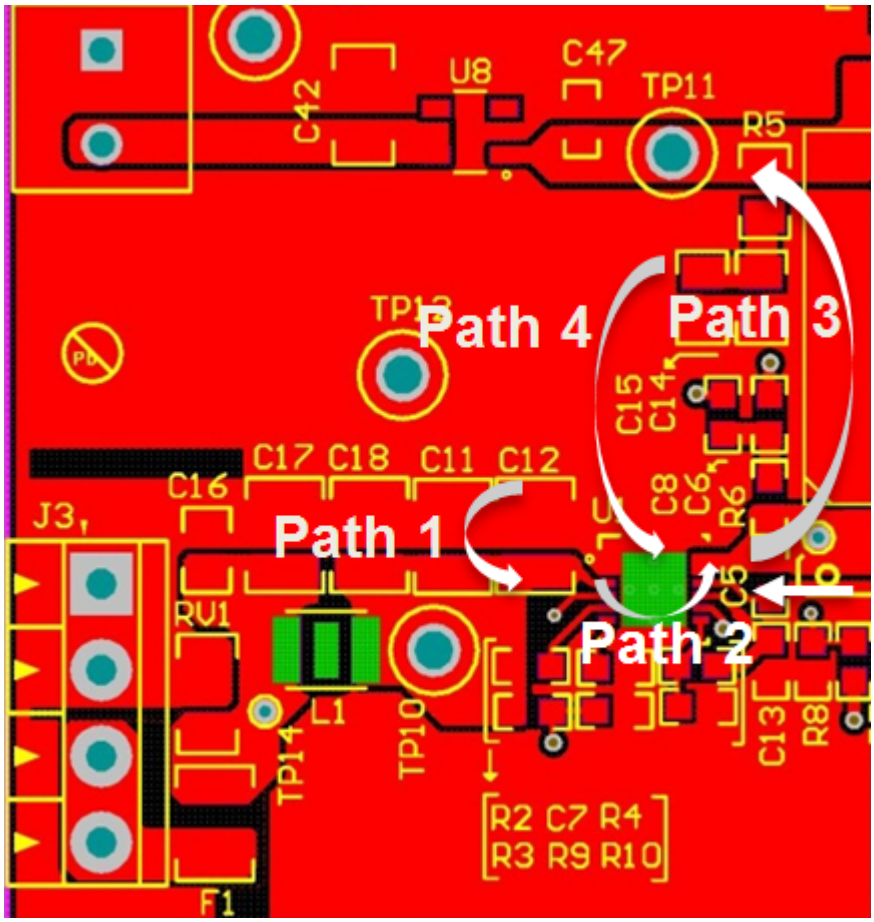


Figure 19. Isolating Converter Primary Side

Figure 20 shows the critical parts of the layout for the secondary side. To reduce EMI, the current loops shown by ellipses Loop 4, 5, and 6 are kept as small as possible. Therefore, D1-C1, D2-C2, and D3-C4 are placed near to each other and the transformer.

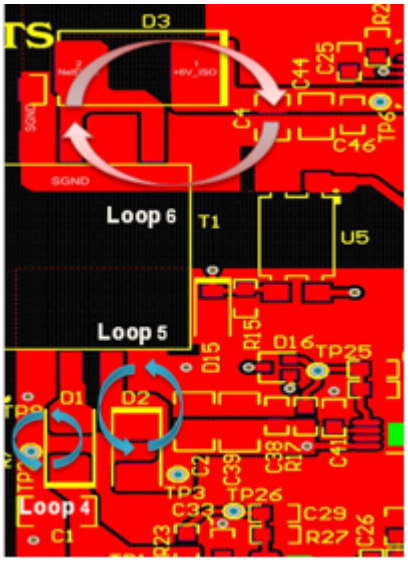


Figure 20. Isolating Converter Secondary Side

7.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00401.

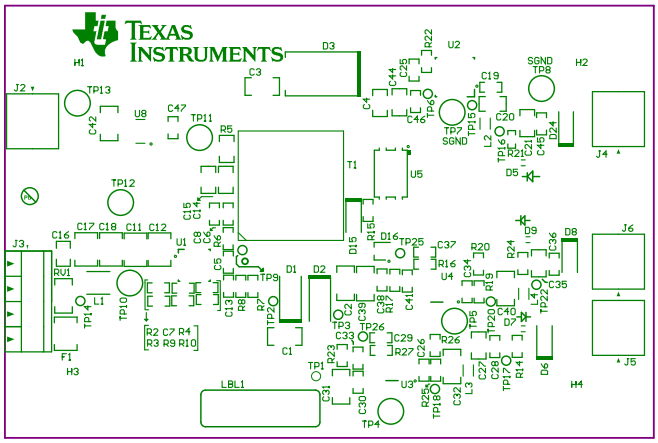


Figure 21. Top Silkscreen Overlay

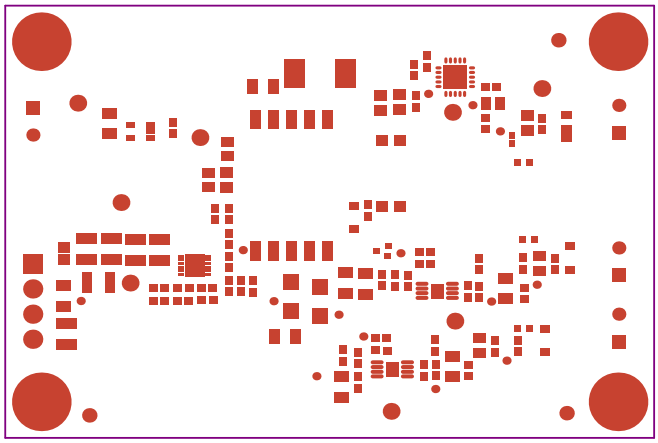


Figure 22. Top Solder Mask

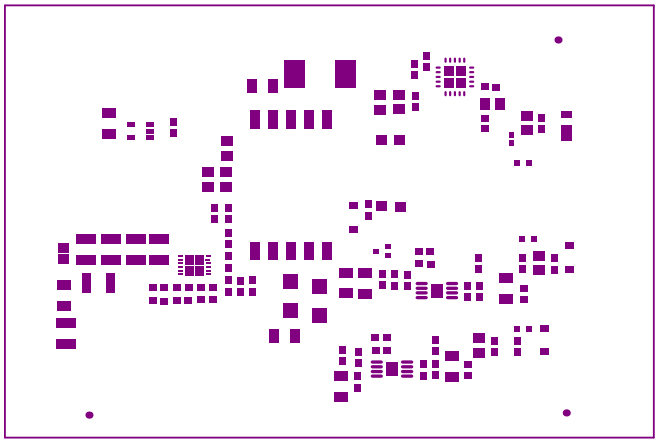


Figure 23. Top Paste Mask

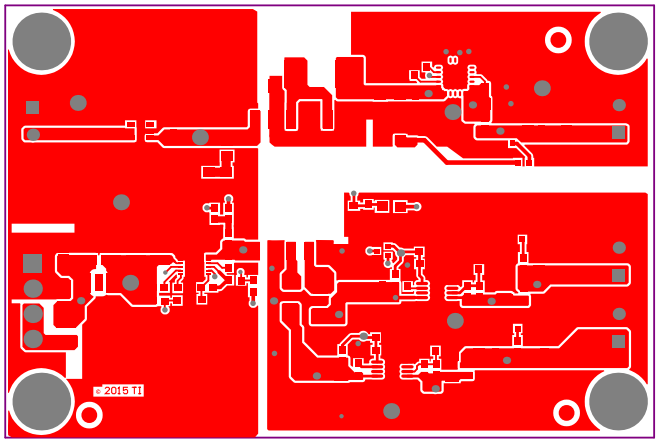


Figure 24. Top Layer

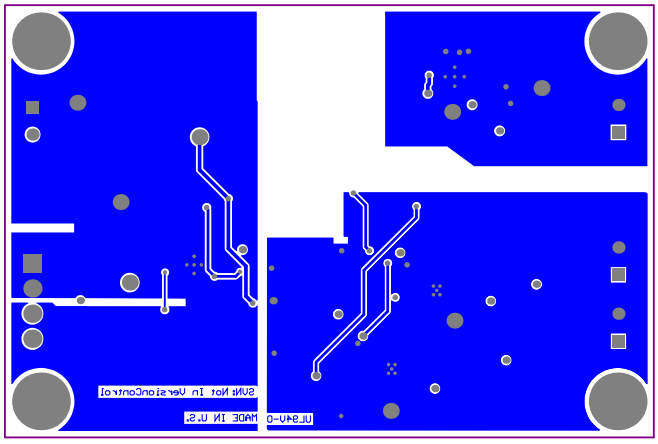


Figure 25. Bottom Layer

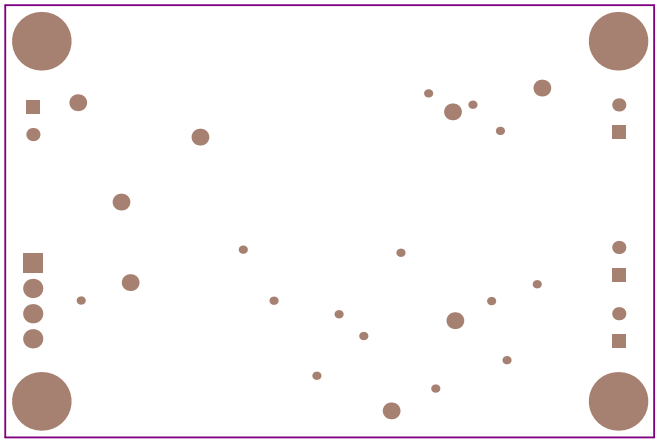
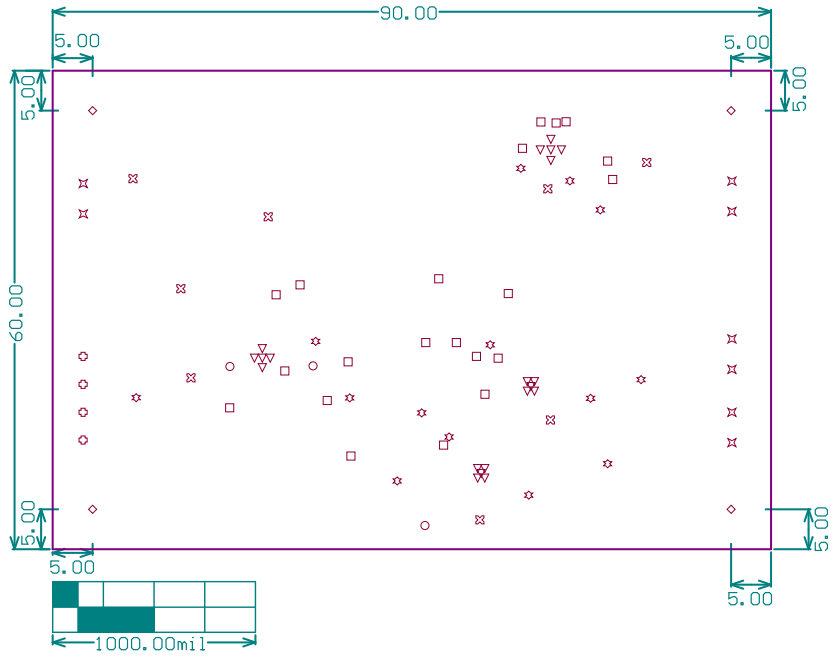


Figure 26. Bottom Solder Mask



Symbol	Hit Count	Tool Size	Plated	Hole Type
▽	20	7.874mil (0.2mm)	PTH	Round
○	3	12mil (0.305mm)	PTH	Round
□	21	16mil (0.406mm)	PTH	Round
✲	14	20mil (0.508mm)	PTH	Round
✲	8	43.307mil (1.1mm)	PTH	Round
○	4	50mil (1.27mm)	PTH	Round
⊠	8	63mil (1.6mm)	PTH	Round
◇	4	125.984mil (3.2mm)	PTH	Round
	82 Total			

Drill Table

Figure 27. Drill Drawing

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00401.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00401.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00401.

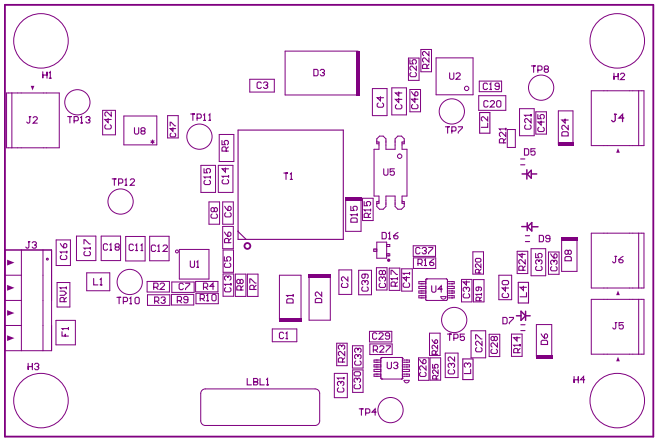


Figure 28. Top Assembly Drawing

Figure 29. Bottom Assembly Drawing

8 References

1. Texas Instruments, *Ultra-Thin, Small Footprint 1-W, 12- to 36-V Isolated Power Supply With ±15 V and 5 V for Analog PLC Modules*, TIDA-00237 Design Guide (TIDU855).
2. Texas Instruments, *AN-2292 Designing an Isolated Buck (Flybuck) Converter*, Application Report (SNVA674).

9 About the Authors

SANKAR SADASIVAM is Chief Technologist for Industrial Systems Engineering at Texas Instruments where he is responsible for architecting and developing reference design solutions for the industrial segment. Sankar brings to this role his extensive experience in analog, RF, wireless, signal processing, high-speed digital and power electronics. Sankar earned his master of science (MS) in electrical engineering from the Indian Institute of Technology, Madras.

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Revision History

Changes from Original (June 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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