

TestSetUp:

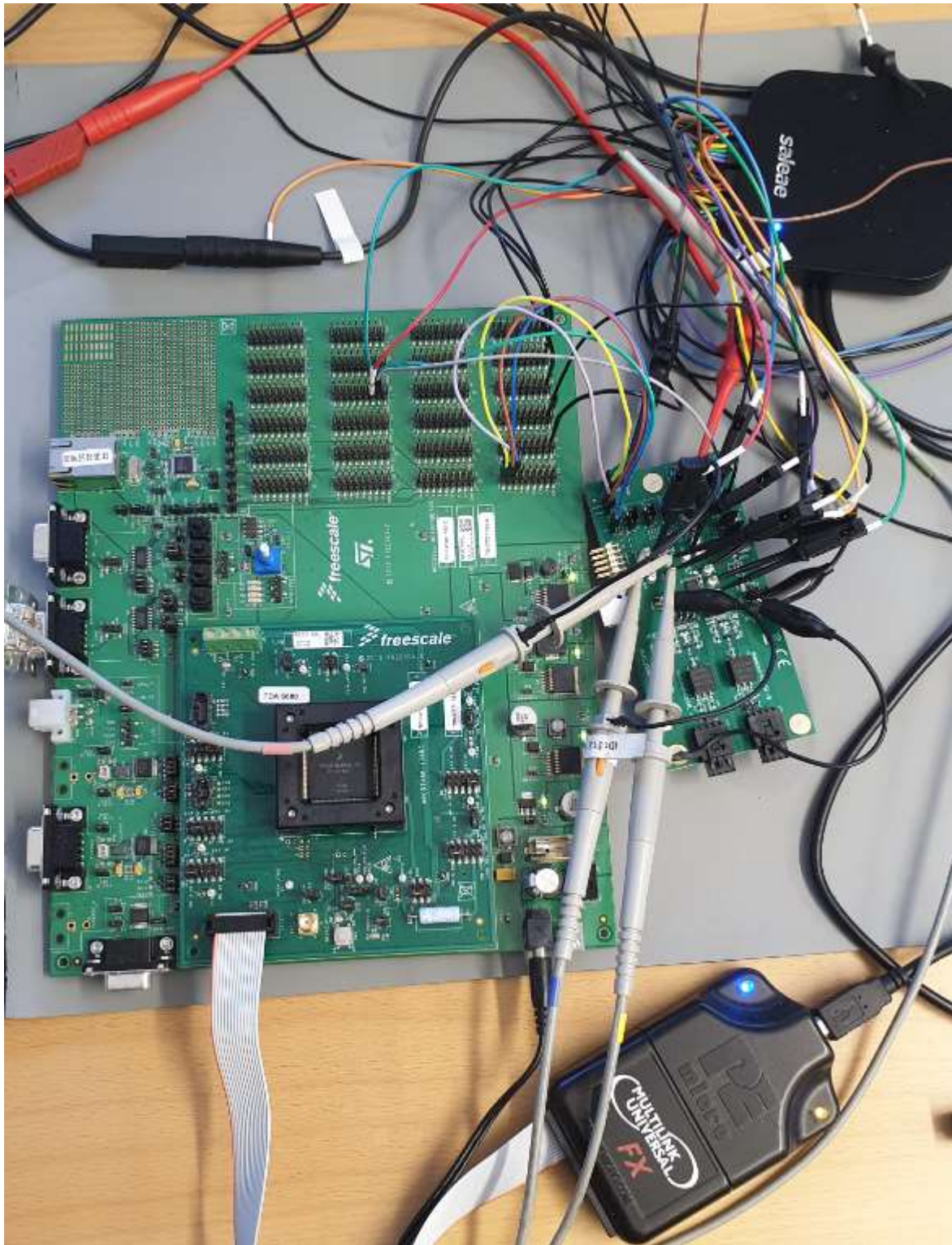
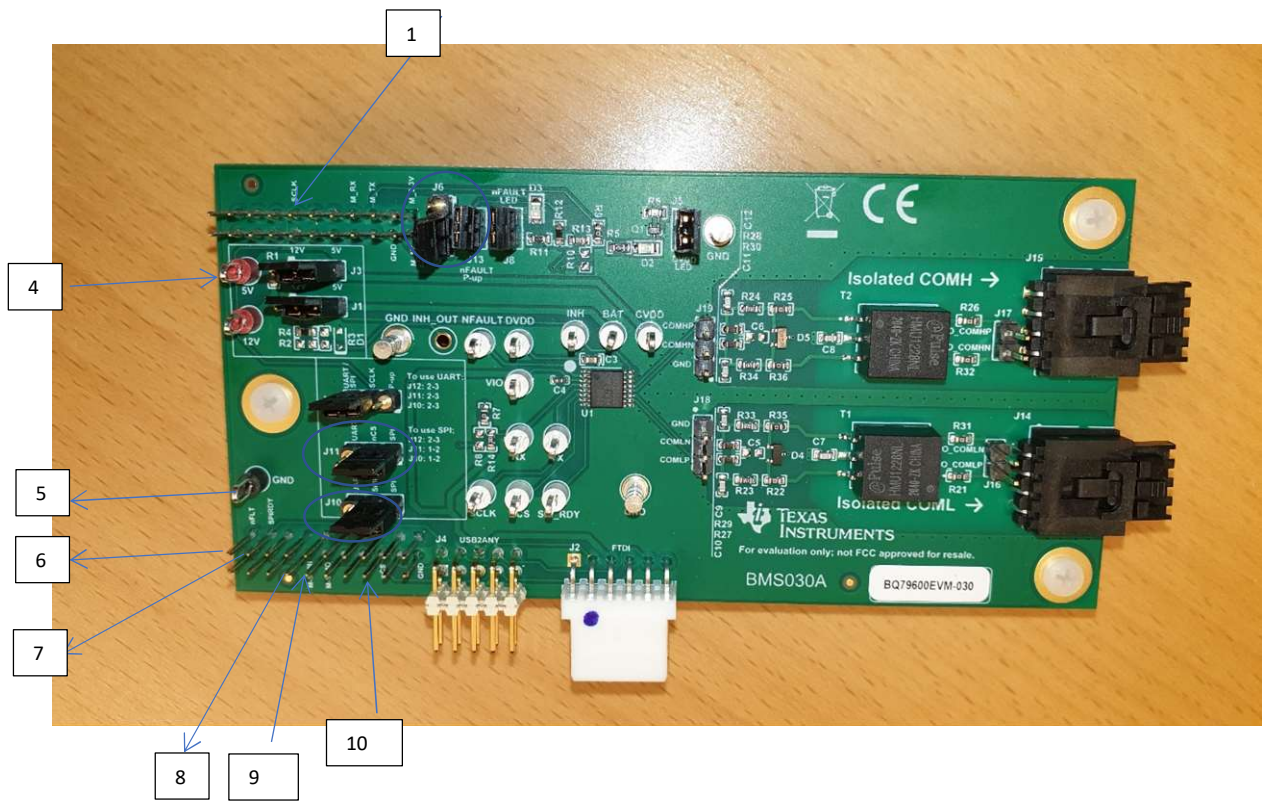


Figure -1 Test setup, NXP EVM board Master on SPI bus, BQ79600 slave

Connection EVM BQ79600.



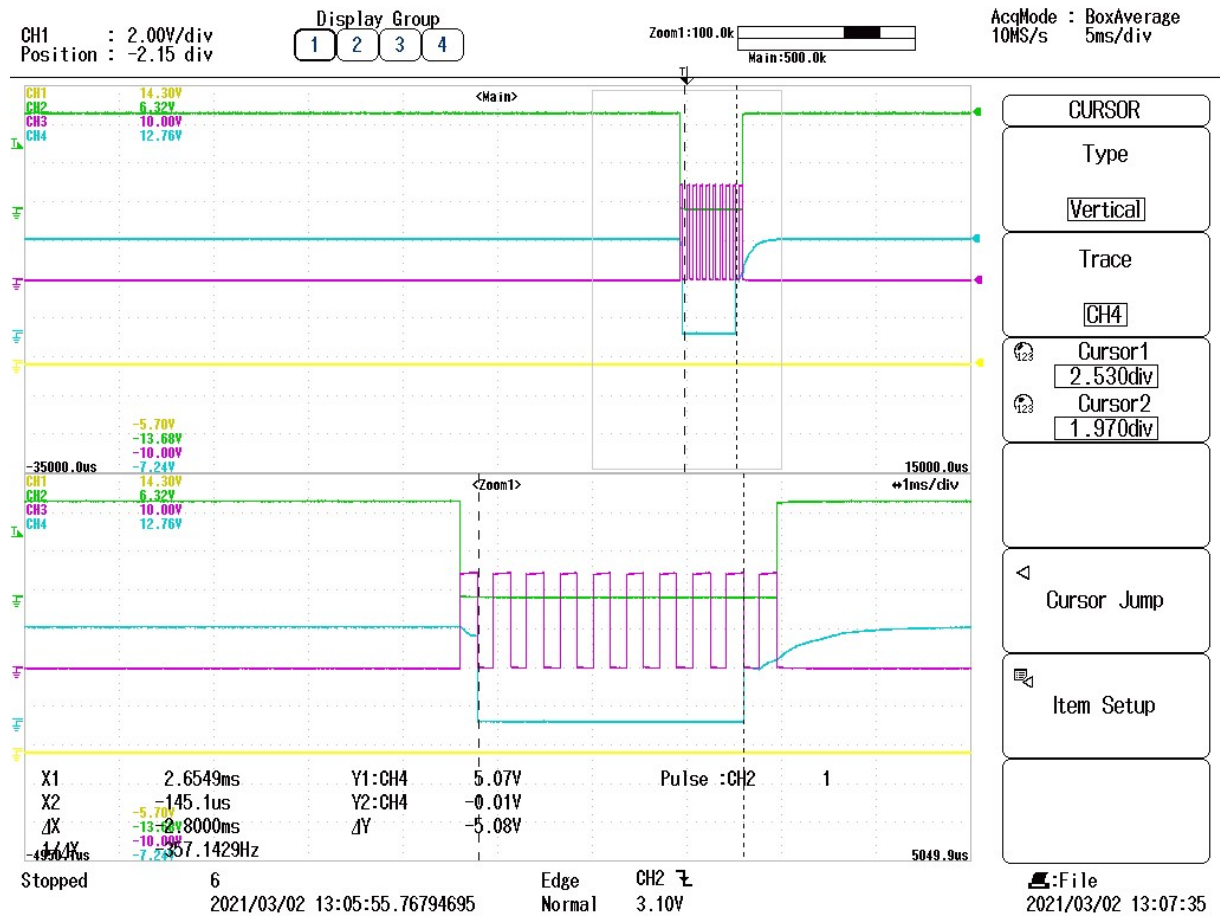
- 1: SCLK (PJ[14])
- 4: 5V
- 5: Gnd
- 6: nFLT(GPIO IN PJ[15])
- 7: SPI_RDY(GPIO IN, PK[0])
- 8: MISO(PK[1])
- 9: MOSI(PK[2])
- 10: CS(PK[5])

On the EVM board is also resistors moved.

00hms R7 is moved to R8.

00hms R9 is moved to R10.

PING.



CH1: MISO
CH2: nCS
CH3: SPI CLK
CH4: MOSI
Signal level on SPI is 5V.

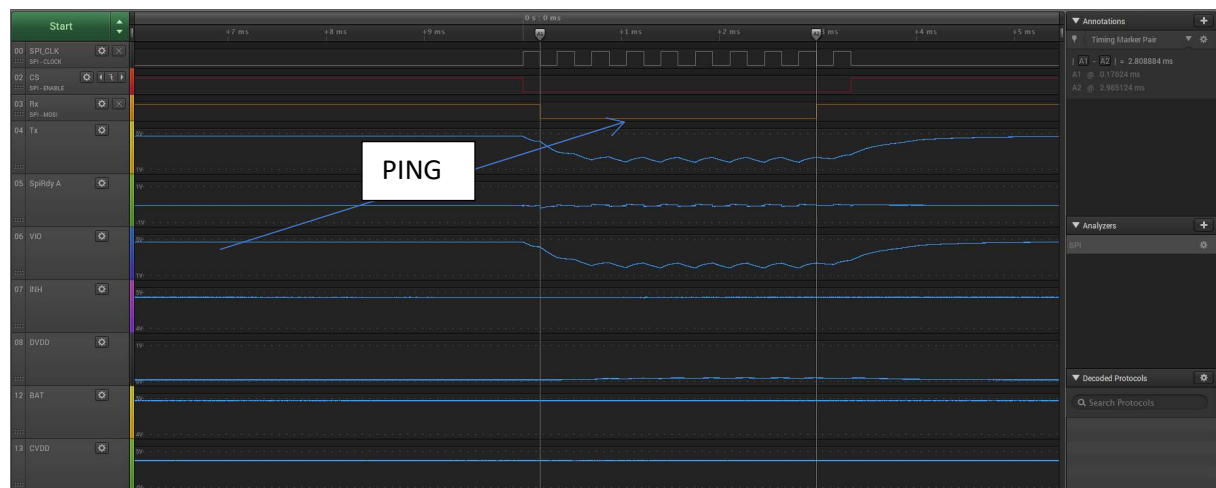


Figure-3 PING @ 2.8 ms on MOSI

Tabell 1 SIGNALS @ PING

Channel	Name	Description
0	SPI_CLK	2.857 kHz
1	nFault	State -1, (5V)
2	nCS	Transition to active 0.175 ms before MOSI enter low state. Transition to inactive 0.35 ms after MOSI enter high state.
3	RX Connector	Low state 2.8ms
4	Tx	Follow VIO
5	SPIRdy	0 V
6	VIO	Follow Tx
7	INH	5V
8	DVDD	0V
12	BAT	5V
13	CVDD	5V

SPI bus signals on EVM BQ79600

SCLK 6 DI: SPI clock input. If SPI interface is used, this pin is connected to SPI master controller. Connect to GND with a **10-100kohm pull-down resistor**. If not used, connect to GND.

nCS 7 DI: Active low chip select pin for SPI interface. Connect to **VIO with 10-100kohm pull-up resistor** in SPI mode. Cannot hardwire to GND in SPI mode. Connect to GND in UART mode.

RX/MOSI 4 DI: UART receiver input or SPI master out slave in. Connect to **VIO with a 10-100kohm pull-up resistor**. Don't leave it unconnected.

TX/MISO 5 DO: UART transmitter output or SPI master in slave out. Pull up to **VIO with a 10-100kohm pull-up resistor** at MCU side. MISO pin drives high in SPI idle mode, cannot directly support SPI multidrop, if multidrop is needed, add a tri-state buffer between BQ79600-Q1 and MCU.

Configuration on master nxp EVM board:

SCLK: Output Driver control as Push-Pull.

MISO: Input

MOSI: Output driver control as Open-Drain.

CS: Output driver control as Open-Drain.

Auto addressing:

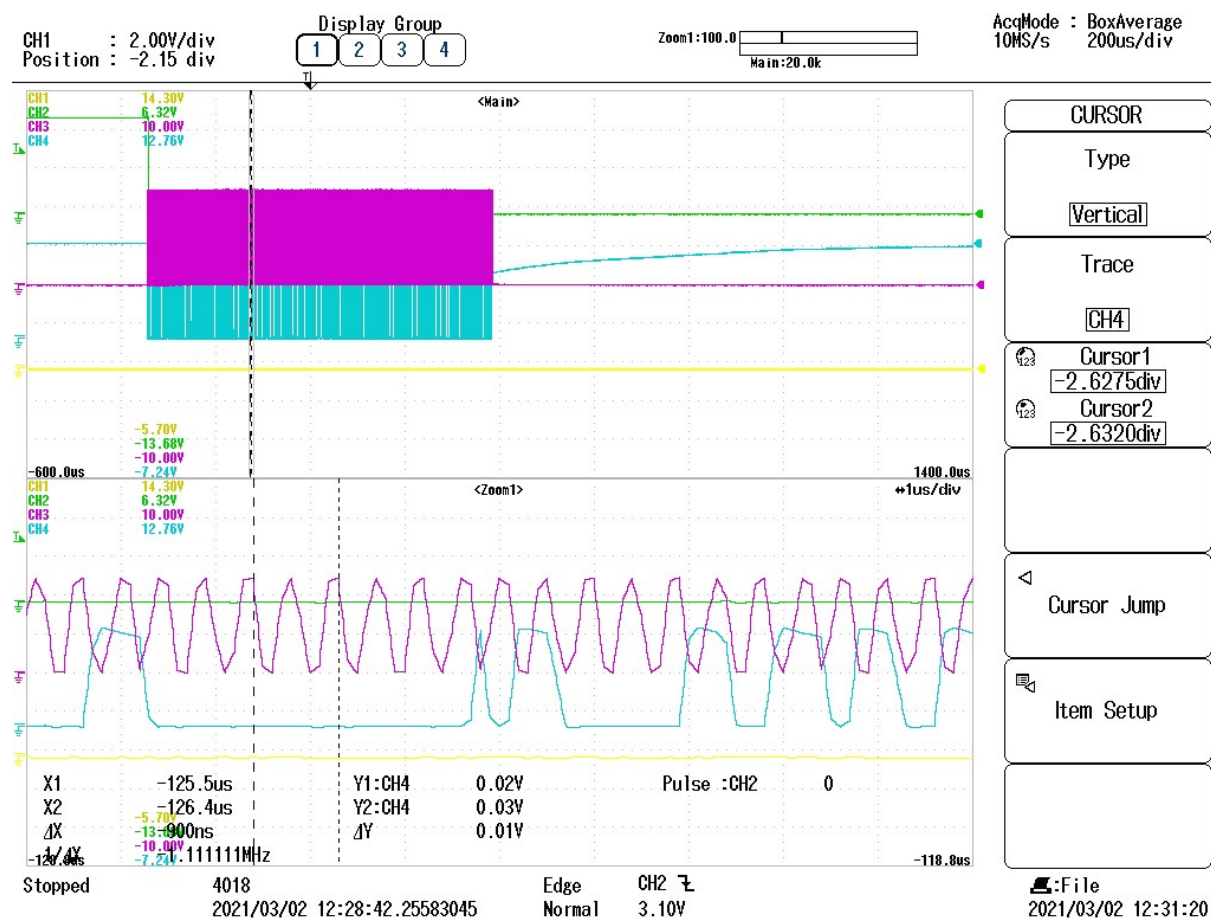
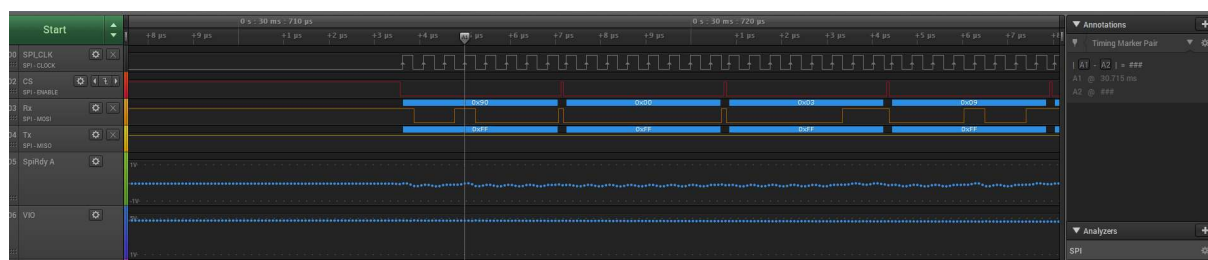


Figure --2 oscilloscope measurement on SPI bus @ auto addressing frame.

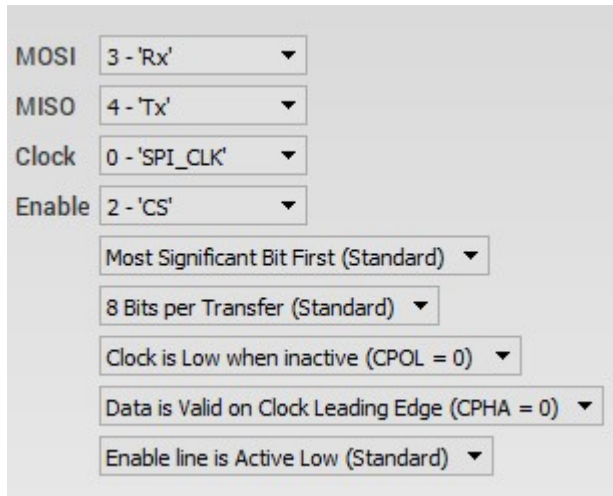
- CH1: MISO
- CH2: Extern Trigg signal @ start of auto addressing frame
- CH3: SPI CLK @ 2.5 MHz
- CH4: MOSI

Start Of AUTO ADDRESSING Frame.



Extraction of auto addressing SPI data frame.

Data extracted from SPI bus, MOSI and CLK.



MOSI 3 - 'Rx' ▼

MISO 4 - 'Tx' ▼

Clock 0 - 'SPI_CLK' ▼

Enable 2 - 'CS' ▼

Most Significant Bit First (Standard) ▼

8 Bits per Transfer (Standard) ▼

Clock is Low when inactive (CPOL = 0) ▼

Data is Valid on Clock Leading Edge (CPHA = 0) ▼

Enable line is Active Low (Standard) ▼

single device write to BQ79600-Q1 control 1 [DIR_SEL] = 1 (change BQ79600-Q1 direction) + CRC polynomial.
0x90 0x00 0x03 0x09 0x80 0xC8 0xB7

single device write to BQ79600-Q1 CONTROL1 [SEND_WAKE] = 1 (wake up stack devices) + CRC polynomial.
0x90 0x00 0x03 0x09 0x20 0xC8 0xA9

dummy stack write data 0x00 to registers 0x343 to 0x34A (sync up internal DLL). These are 8 separate write commands + CRC polynomial.

0xB0 0x00 0x03 0x43 0x00 0x25 0x57
0xB0 0x00 0x03 0x44 0x00 0x65 0x5B
0xB0 0x00 0x03 0x45 0x00 0xE5 0x52
0xB0 0x00 0x03 0x46 0x00 0xE5 0x5D
0xB0 0x00 0x03 0x47 0x00 0x65 0x54
0xB0 0x00 0x03 0x48 0x00 0xC5 0x5B
0xB0 0x00 0x03 0x49 0x00 0x45 0x52
0xB0 0x00 0x03 0x4A 0x00 0x45 0x5D

brdcast write reverse 0x80 to address 0x309 (change stack devices direction DIR_SEL =1) + CRC polynomial
0xE0 0x00 0x03 0x09 0x80 0x4A 0x64

brdcast Write 0x02 to address 0x308 + CRC polynomial
0xD0 0x00 0x03 0x08 0x02 0xC9 0xCB

brdcast Write 0x81 to address 0x309 (enable BQ7961X-Q1 auto addressing) + CRC polynomial
0xD0 0x00 0x03 0x09 0x81 0xCB 0x47

brdcast Write consecutively to address 0x307 = 0,1,2,3 (address 1-3 assigned to BQ7961X-Q1, 0 assigned to BQ79600-Q1) + CRC polynomial

0xD0 0x00 0x03 0x07 0x00 0xE8 0x47
0xD0 0x00 0x03 0x07 0x01 0x6B 0x44
0xD0 0x00 0x03 0x07 0x02 0x69 0xC4
0xD0 0x00 0x03 0x07 0x03 0xEA 0xC7

brdcast write 0x02 to address 0x308 (set BQ7961X-Q1 as stack device) + CRC polynomial
0xD0 0x00 0x03 0x08 0x02 0xC9 0xCB

single device write to device 3: data 0x03 to address 0x308 (set 3rd BQ7961X-Q1 as top of stack, BQ79600-Q1 is default to base) + CRC polynomial
0x90 0x00 0x03 0x08 0x03 0xCA 0x3B

dummy stack read registers 0x343 to 0x34A (sync up internal DLL). These are 8 separate read commands. + CRC polynomial
0xA0 0x00 0x03 0x43 0x00 0xA6 0x94
0xA0 0x00 0x03 0x44 0x00 0xE6 0x98
0xA0 0x00 0x03 0x45 0x00 0x66 0x91
0xA0 0x00 0x03 0x46 0x00 0x66 0x9E
0xA0 0x00 0x03 0x47 0x00 0xE6 0x97
0xA0 0x00 0x03 0x48 0x00 0x46 0x98
0xA0 0x00 0x03 0x49 0x00 0xC6 0x91
0xA0 0x00 0x03 0x4A 0x00 0xC6 0x9E

stack read address 0x307 (read back to verify address are correct for stack device) + CRC polynomial
0xA0 0x00 0x03 0x07 0x00 0x6A 0x94

single device read to BQ79600-Q1, verify $0x2001 = 0x14 + \text{CRC polynomial}$
0x80 0x00 0x03 0x07 0x00 0xEB 0x77