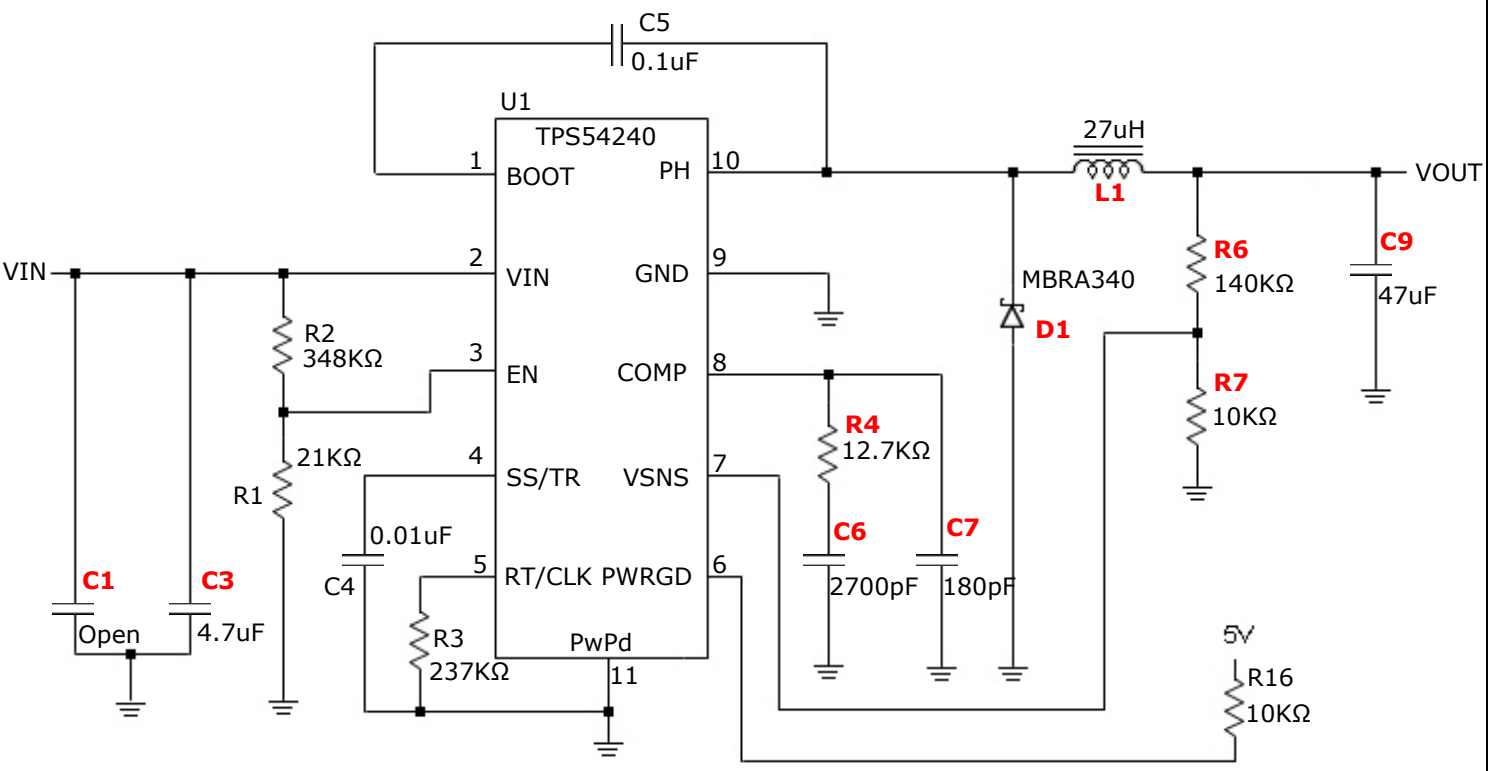
SwitcherPro Design Report
Schematic

Design Name: TPS54240 30V to 12V @ 2A **Part:** TPS54240

VinMin: 24V **VinMax:** 30V **Vout:** 12V **Iout:** 2A



SwitcherPro Design Report
Analysis - Main

Design Name: TPS54240 30V to 12V @ 2A **Part:** TPS54240

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Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Input Voltage Volts - V	24.00	-	30.00	-	-	-	-	-	-
Input Ripple mVp-p - mVp-p	-	-	-	-	-	600	-	-	286.0
UVLO(Start) Volts - V	-	-	-	-	-	-	-	21.65	-
UVLO(Stop) Volts - V	-	-	-	-	-	-	-	20.64	-
Switching Frequency KHz - KHz	-	-	-	-	500	-	-	-	-
Slow Start ms - ms	-	-	-	-	4.00	-	-	-	-
Estimated PCB Area mm² - mm²	-	-	-	-	-	-	-	441	-
Max Component Height mm - mm	-	-	-	-	-	25	-	-	6

SwitcherPro Design Report
Analysis - Output1

Design Name: TPS54240 30V to 12V @ 2A **Part:** TPS54240

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Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Output Voltage Volts - V	-	12.000	-	-	-	-	11.543	-	12.471
Output Ripple mVp-p - mVp-p	-	-	-	-	-	240	-	-	7.7
Output Current Amps - A	-	-	2.000	0.100	-	-	-	-	-
Inductor Peak to Peak Current Amps - A	-	-	-	-	-	-	0.576	-	0.699
Current Limit Threshold Amps - A	-	-	-	-	2.700	-	-	-	-
Gain Margin dB - dB	-	-	-	-10	-	-	-	-23	-
Phase Margin Deg. - Deg.	-	-	-	60	-	-	-	61	-
Upper FET RDSon mOhms - mΩ	-	-	-	-	-	-	246	-	248
Duty Cycle % - %	-	-	-	-	-	-	41.6	-	52.1
On Time Min (switch) ns - ns	-	-	-	-	-	-	679.7	-	1344.6
Cross Over Frequency KHz - KHz	-	-	-	-	-	-	-	15	-

SwitcherPro Design Report
Stress Results

Design Name: TPS54240 30V to 12V @ 2A **Part:** TPS54240

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Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C3 (High Freq. Input Cap)	50V	30.2V	3A	1.01A	-	5mW	-
C9 (Bulk Output Cap)	16V	12.1V	4.16A	0.2A	-	65uW	-
L1 (Output Inductor)	-	-	2.97A	2.01A	-	162mW	-
D1 (Catch Diode)	40V	30.2V	3A	1.17A	-	412mW	58°C
U1 (Converter)	60V	30.2V	4A	1.45A	-	1.2W	73°C

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Efficiency

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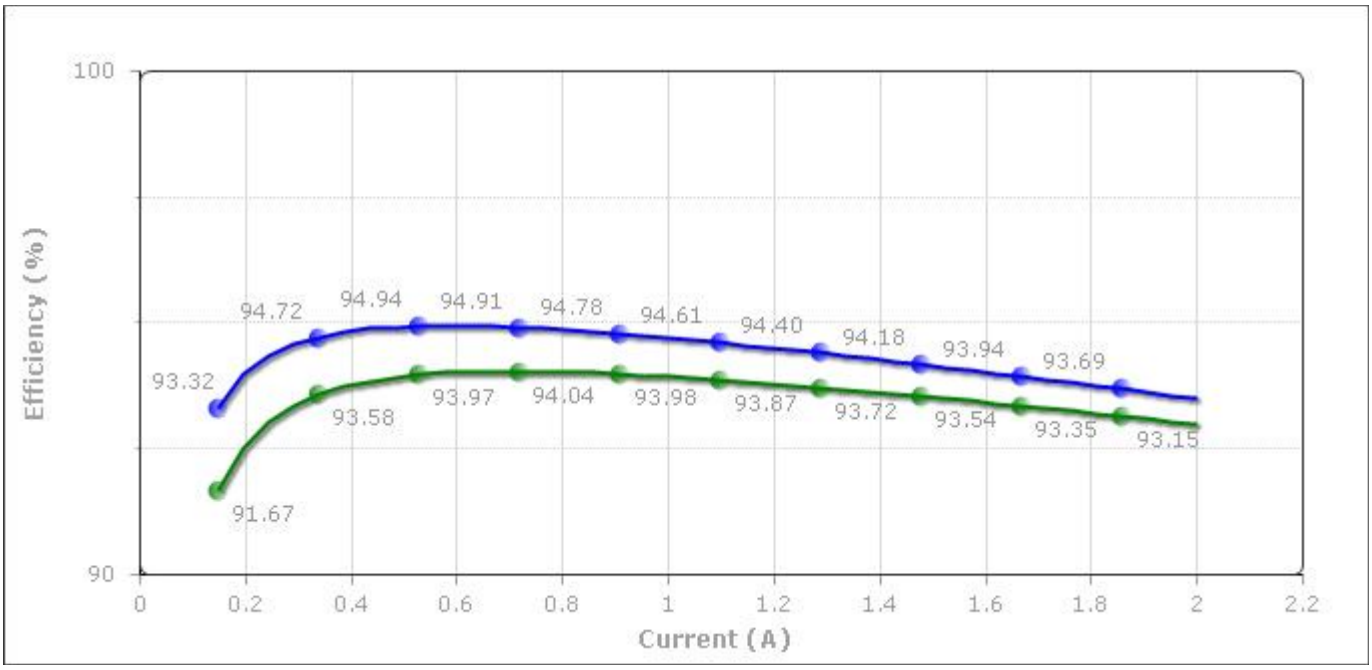

Efficiency For Vin Max
Efficiency For Vin Min

SwitcherPro Design Report
Loop Response

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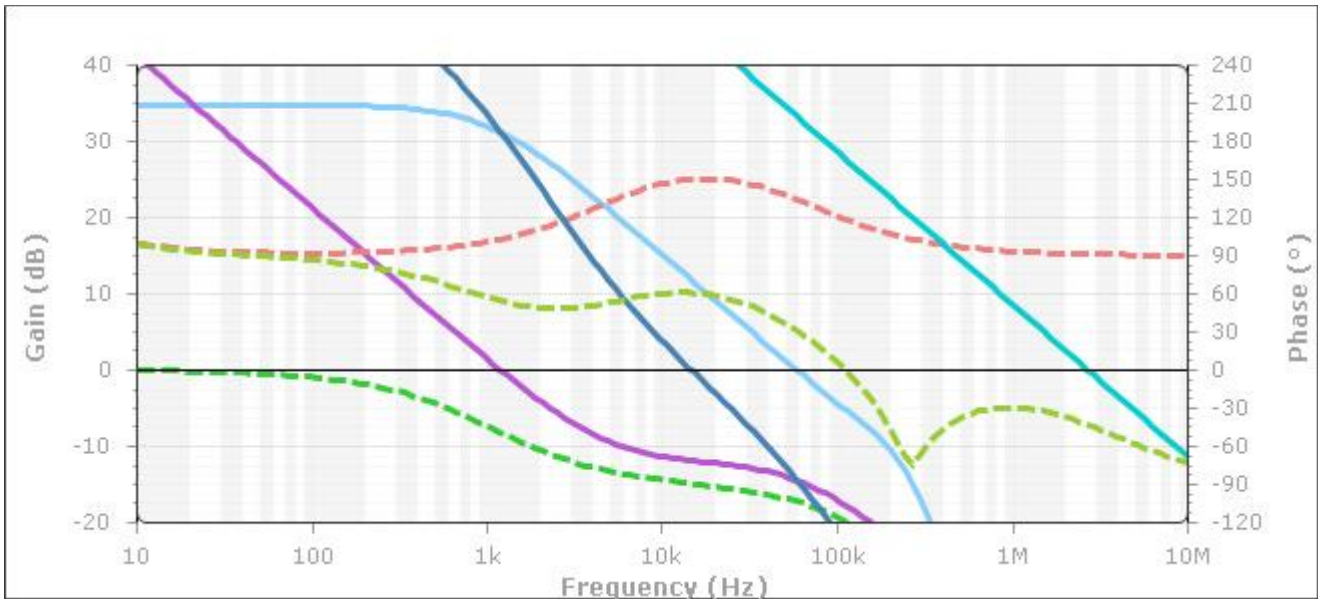

- Power Stage Gain
- Power Stage Phase
- Compensation Gain
- Compensation Phase
- Error Amp Gain
- Total Gain
- Total Phase

SwitcherPro Design Report
Bill of Materials

Design Name: TPS54240 30V to 12V @ 2A **Part:** TPS54240

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Name	Quantity	Part Number	Description	Manufacturer	Package	Area(mm²)	Height(mm)
C3	1	GRM32ER71H475KA88L	Capacitor, Ceramic, 4.7uF, 50V, 10%	Murata Manufacturing	1210	10	2
C4	1	Standard	Capacitor, Ceramic, 0.01uF, 10V, 20%	Standard	0603	2	1
C5	1	Standard	Capacitor, Ceramic, 0.1uF, 20V, 10%	Standard	0603	2	1
C6	1	Standard	Capacitor, Ceramic, 2700pF, 20V, 20%	Standard	0603	2	1
C7	1	Standard	Capacitor, Ceramic, 180pF, 20V, 20%	Standard	0603	2	1
C9	1	C5750X5R1C476M	Capacitor, Ceramic, 47uF, 16V, 20%	TDK	C5750 2220	31	2
D1	1	MBRA340	Diode, Schottky, 40V, 3A	On Semiconductor	SMA	12	2
L1	1	744771127	Inductor, 27uH, 2.97A, 40mΩ	Wurth Electronics	L	144	6
R1	1	Standard	Resistor, SurfaceMount, 21KΩ, 100mW, 1%	Standard	0603	2	1
R16	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
R2	1	Standard	Resistor, SurfaceMount, 348KΩ, 100mW, 1%	Standard	0603	2	1
R3	1	Standard	Resistor, SurfaceMount, 237KΩ, 100mW, 1%	Standard	0603	2	1
R4	1	Standard	Resistor, SurfaceMount, 12.7KΩ, 100mW, 1%	Standard	0603	2	1
R6	1	Standard	Resistor, SurfaceMount, 140KΩ, 62mW, 1%	Standard	0603	2	1
R7	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
U1	1	TPS54240	IC, Converter, 10 pins	Texas Instruments, Inc.	10MSOP-PowerPAD	15	1

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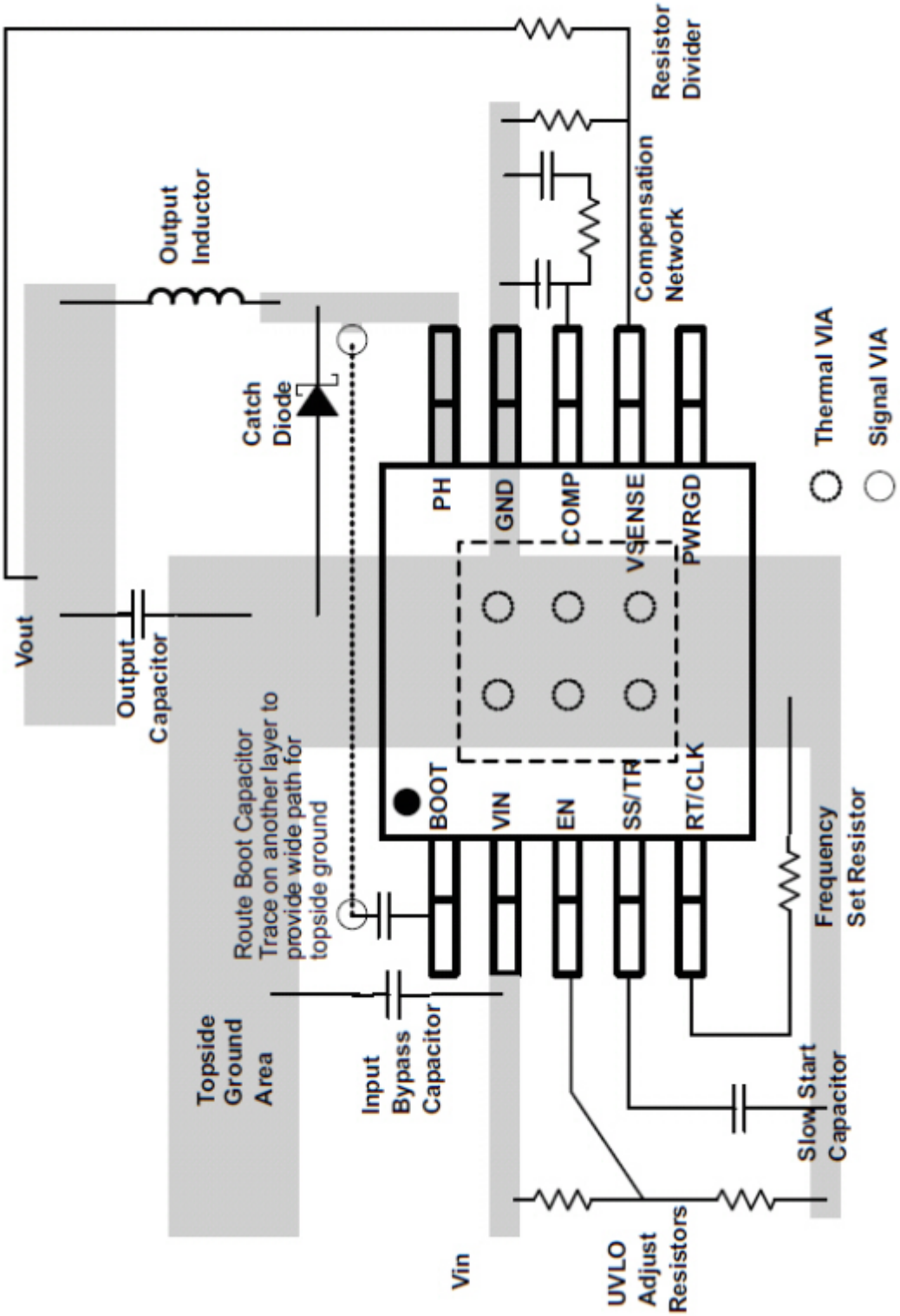

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Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure for a PCB layout example. The GND pin should be tied directly to the power pad under the IC and the power pad.The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Since the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.