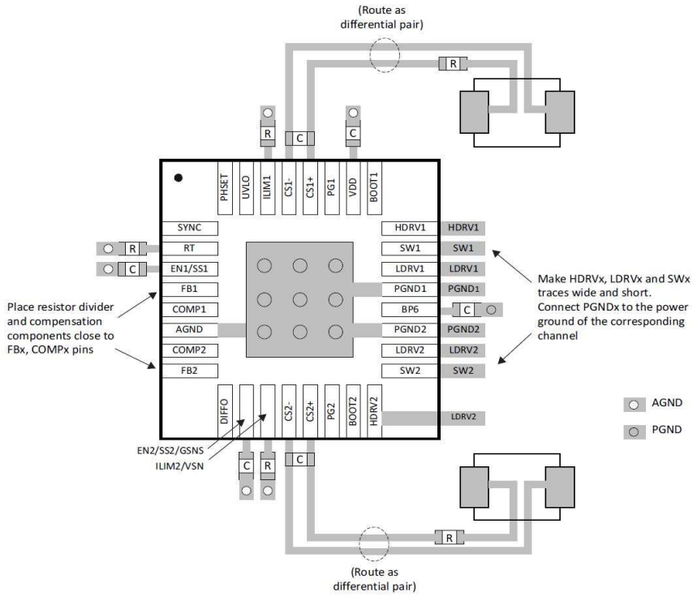
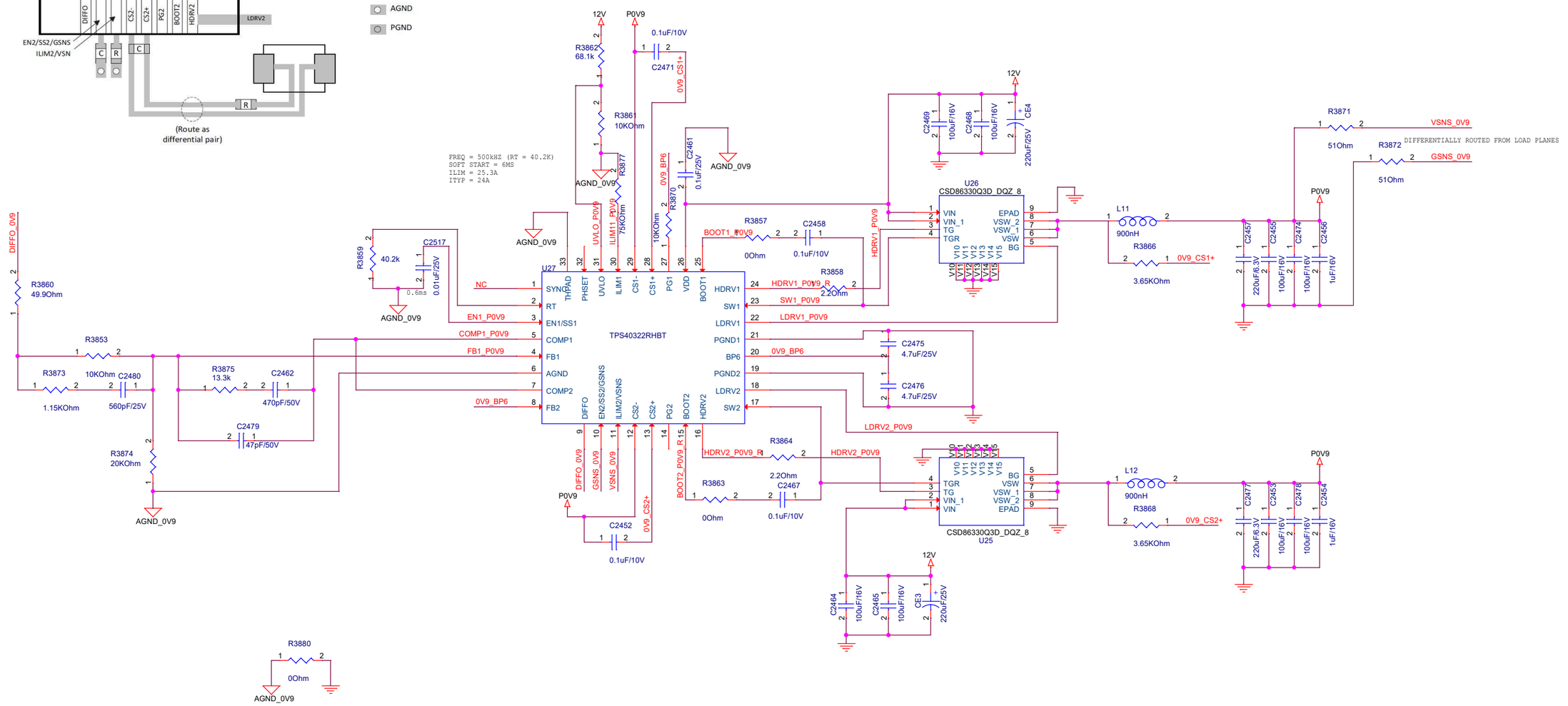




10.1.2 Device Peripheral

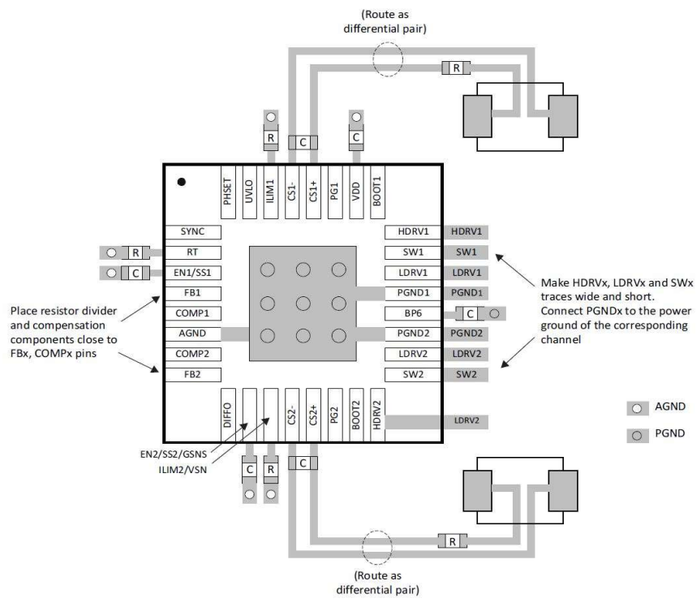
The TPS40322 provides separate signal ground (AGND) and power ground (PGND1 and PGND2) pins. It is required to properly separate the circuit grounds. The return path for the pins associated with the power stage must be through PGND. The other pins (especially for those sensitive pins such as FB1, FB2, RT, ILIM1, and ILIM2) must be through the low noise AGND. The AGND and PGND planes are suggested to be connected at the output capacitor with single 20-mil trace. A minimum 0.1-µF ceramic capacitor must be placed as close to the VDD pin and AGND as possible with at least 15-mil wide trace from the bypass capacitor to the AGND. A minimum value of 3.3-µF ceramic capacitor must be connected from BP6 to PGND, placed as close to the BP6 pin as possible. When DCR sensing method is applied, the sensing resistor must be placed close to the SW node and connected to the inductor with a kelvin connection. The sensing traces from the power stage to the chip must be away from the switching components. The sensing capacitor must be placed very close to the CS+ and CS- pins for each output. The frequency setting resistor must be placed as close to RT pin and AGND as possible. In two-phase mode, the ILIM2/VSNS and EN2/SS2/GSNS pins must be directly connected to the point of load where the voltage regulation is required. A parallel pair of 10-mil traces connects the regulated voltage back to the chip. They must be away from the switching components.

Bigstep
1 Fore Street, 1st Floor, London EC2Y 5EJ
www.bigstep.com

Size		Rev
C	BSMCY-BPXD P0V9	1.0
Authors:	Aurelian Timu <OrgAddr4>	
Modified:	Tuesday, October 17, 2017	Sheet 1 of 1

10.1.2 Device Peripheral

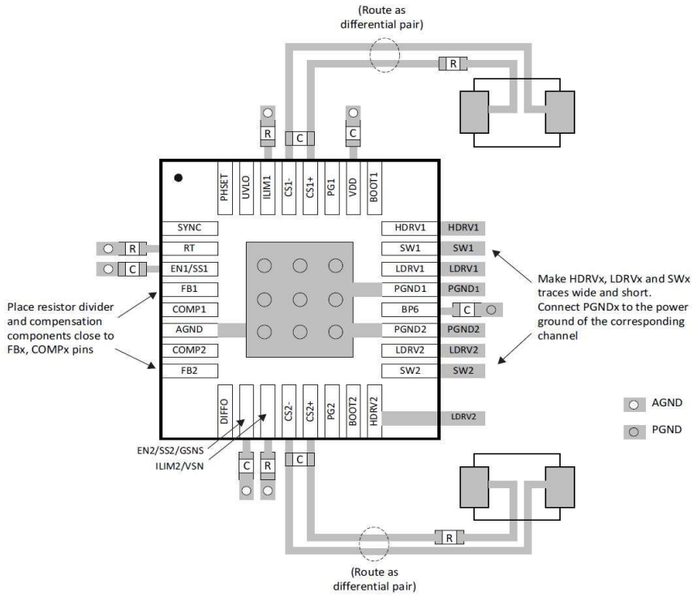
The TPS40322 provides separate signal ground (AGND) and power ground (PGND1 and PGND2) pins. It is required to properly separate the circuit grounds. The return path for the pins associated with the power stage must be through PGND. The other pins (especially for those sensitive pins such as FB1, FB2, RT, ILIM1, and ILIM2) must be through the low noise AGND. The AGND and PGND planes are suggested to be connected at the output capacitor with single 20-mil trace. A minimum 0.1-µF ceramic capacitor must be placed as close to the VDD pin and AGND as possible with at least 15-mil wide trace from the bypass capacitor to the AGND. A minimum value of 3.3-µF ceramic capacitor must be connected from BP6 to PGND, placed as close to the BP6 pin as possible. When DCR sensing method is applied, the sensing resistor must be placed close to the SW node and connected to the inductor with a kelvin connection. The sensing traces from the power stage to the chip must be away from the switching components. The sensing capacitor must be placed very close to the CS+ and CS- pins for each output. The frequency setting resistor must be placed as close to RT pin and AGND as possible. In two-phase mode, the ILIM2/VSNS and EN2/SS2/GSNS pins must be directly connected to the point of load where the voltage regulation is required. A parallel pair of 10-mil traces connects the regulated voltage back to the chip. They must be away from the switching components.

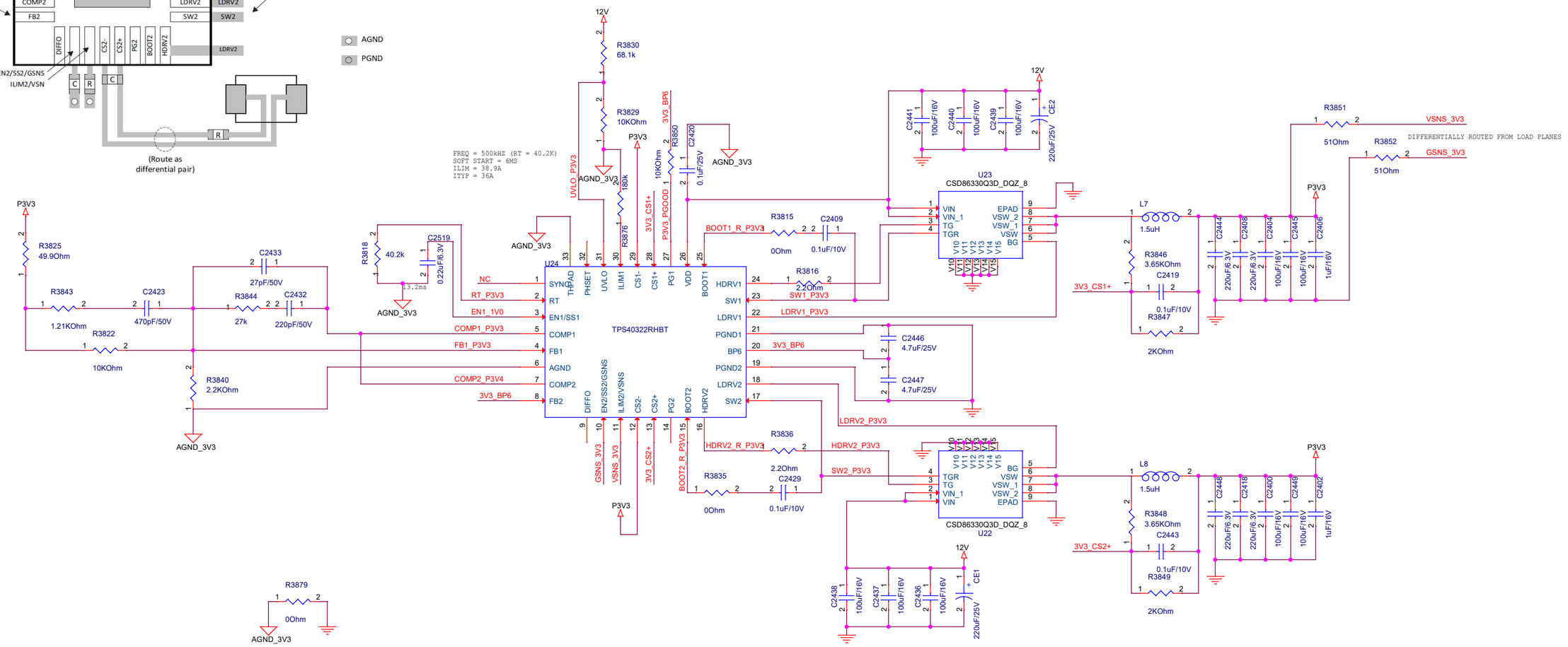


Bigstep
1 Fore Street, 1st Floor, London EC2Y 5EJ
www.bigstep.com

Size		Rev
C	BSMCY-BPXD P1V0_P1V8	1.0

Authors:	Aurelian Timu <OrgAddr4>		
Modified:	Tuesday, October 17, 2017	Sheet 1 of 1	





10.1.2 Device Peripheral

The TPS40322 provides separate signal ground (AGND) and power ground (PGND1 and PGND2) pins. It is required to properly separate the circuit grounds. The return path for the pins associated with the power stage must be through PGND. The other pins (especially for those sensitive pins such as FB1, FB2, RT, ILIM1, and ILIM2) must be through the low noise AGND. The AGND and PGND planes are suggested to be connected at the output capacitor with single 20-mil trace. A minimum 0.1-µF ceramic capacitor must be placed as close to the VDD pin and AGND as possible with at least 15-mil wide trace from the bypass capacitor to the AGND. A minimum value of 3.3-µF ceramic capacitor must be connected from BP6 to PGND, placed as close to the BP6 pin as possible. When DCR sensing method is applied, the sensing resistor must be placed close to the SW node and connected to the inductor with a kelvin connection. The sensing traces from the power stage to the chip must be away from the switching components. The sensing capacitor must be placed very close to the CS+ and CS- pins for each output. The frequency setting resistor must be placed as close to RT pin and AGND as possible. In two-phase mode, the ILIM2/VSNS and EN2/SS2/GSNS pins must be directly connected to the point of load where the voltage regulation is required. A parallel pair of 10-mil traces connects the regulated voltage back to the chip. They must be away from the switching components.

Bigstep
1 Fore Street, 1st Floor, London EC2Y 5EJ
www.bigstep.com

Size		Rev
C	BSMCY-BPXD P3V3	1.0
Authors:	Aurelian Timu <OrgAddr4>	
Modified:	Tuesday, October 17, 2017	Sheet 1 of 1