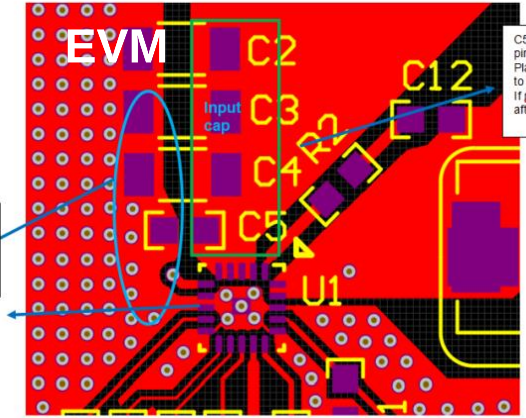
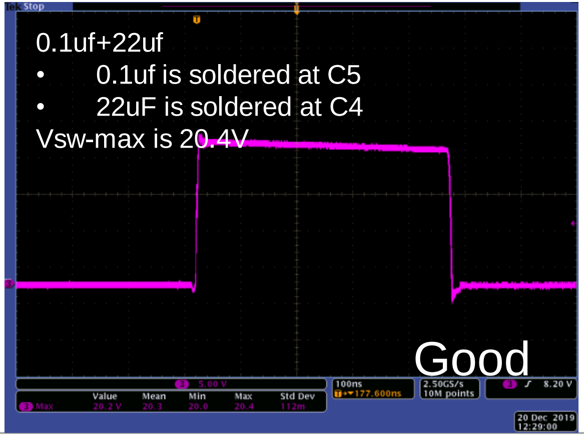
Ring comparison for different layout

- In order to understand the impact to the ring with different layout, below is EVM test data for reference.
- Vin=19V, Vout=5V, Iout=8A



C5-0.1uF should be closest to Vin pin2~5, recommend around 1mm. Place C2/C3/C4, 10uF cap close to C5.
If pos-caps is used, place them after Ceramic cap.

Input cap Ground trace should also be as short as possible to power ground of the chip,
Also add some vias to connect to other ground layers.

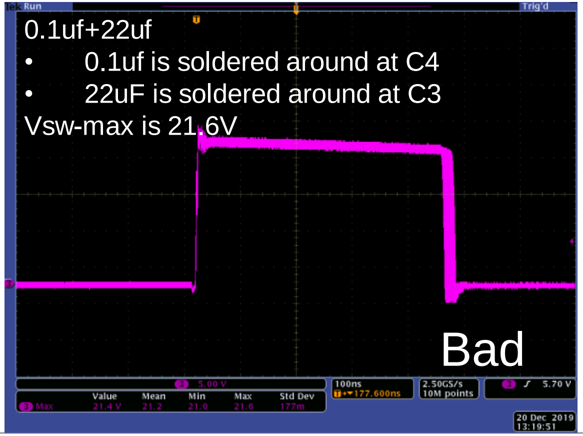


0.1uf+22uf
- 0.1uf is soldered at C5
- 22uF is soldered at C4

Vsw-max is 20.4V

Good

	Value	Mean	Min	Max	Std Dev
3 Max	20.2 V	20.3	20.0	20.4	112m

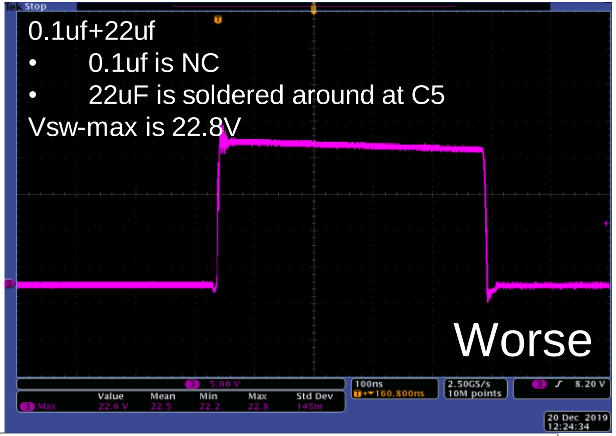


0.1uf+22uf
- 0.1uf is soldered around at C4
- 22uF is soldered around at C3

Vsw-max is 21.6V

Bad

	Value	Mean	Min	Max	Std Dev
3 Max	21.4 V	21.2	21.0	21.6	177m



0.1uf+22uf
- 0.1uf is NC
- 22uF is soldered around at C5

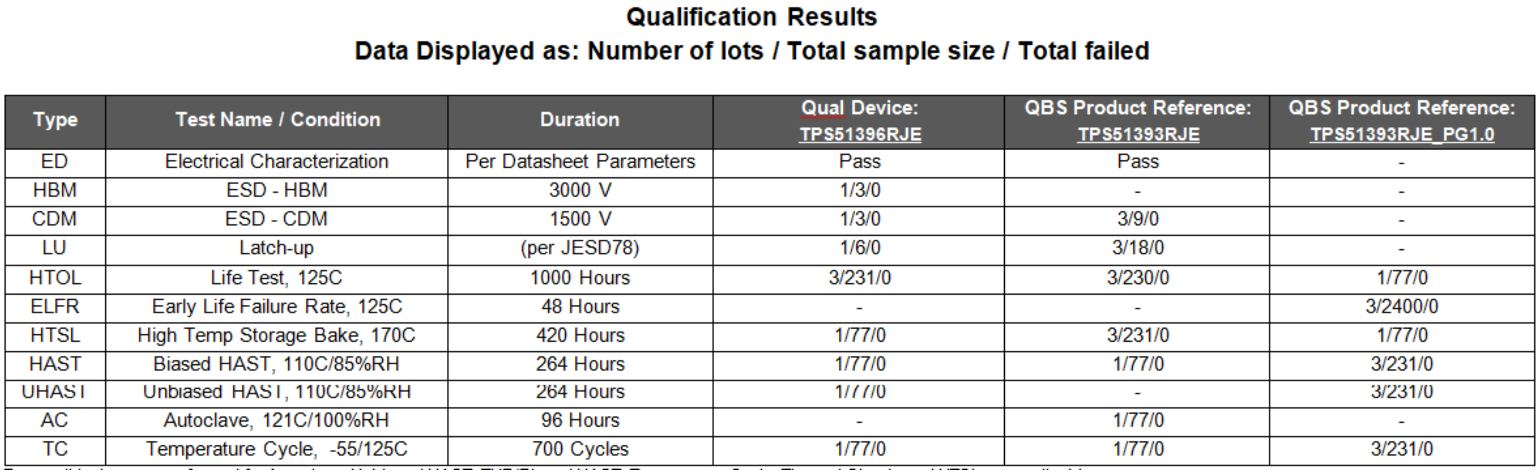
Vsw-max is 22.8V

Worse

	Value	Mean	Min	Max	Std Dev
3 Max	22.6 V	22.5	22.2	22.8	145m

Reliability test

➢ Qualification test (Pass)



Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	Test Name / Condition	Duration	Qual Device: TPS51396RJE	QBS Product Reference: TPS51393RJE	QBS Product Reference: TPS51393RJE_PG1.0
ED	Electrical Characterization	Per Datasheet Parameters	Pass	Pass	-
HBM	ESD - HBM	3000 V	1/3/0	-	-
CDM	ESD - CDM	1500 V	1/3/0	3/9/0	-
LU	Latch-up	(per JESD78)	1/6/0	3/18/0	-
HTOL	Life Test, 125C	1000 Hours	3/231/0	3/230/0	1/77/0
ELFR	Early Life Failure Rate, 125C	48 Hours	-	-	3/2400/0
HTSL	High Temp Storage Bake, 170C	420 Hours	1/77/0	3/231/0	1/77/0
HAST	Biased HAST, 110C/85%RH	264 Hours	1/77/0	1/77/0	3/231/0
UHAST	Unbiased HAST, 110C/85%RH	264 Hours	1/77/0	-	3/231/0
AC	Autoclave, 121C/100%RH	96 Hours	-	1/77/0	-
TC	Temperature Cycle, -55/125C	700 Cycles	1/77/0	1/77/0	3/231/0

➢ EVM aging test (Pass)

- Test Quantity: 10pcs
- Vin = 24V, Vout = 3.3V, Iout = 8A
- Run 720Hrs
- Room temperature