TPS650332-Q1 Automotive Camera PMIC

1 Features

- Qualified for automotive applications
- Systematic capability of up to ASIL D and SIL 3 targeted
- Hardware integrity up to ASIL B and SIL 2 targeted
- Advanced diagnostics and protection
- AEC-Q100 grade 1 qualified
  - -40°C to +125°C ambient operating temperature range
- Three step-down converters:
  - BUCK1 V_{IN} range from 4.0 V to 18.3 V
  - BUCK1 V_{OUT} range from 2.5 V to 4.0 V
  - BUCK1 output current up to 1500-mA
  - BUCK2 and BUCK3 V_{IN} range from 2.5 V to 5.5 V
  - BUCK2 and BUCK3 V_{OUT} range from 0.9 V to 1.9 V
  - BUCK2 and BUCK3 output current up to 1200-mA
  - Spread-spectrum clock (SSC) generation for reduced EMI
  - 2.3-MHz forced fixed switching frequency PWM operation
- One low dropout (LDO) regulator:
  - V_{IN} range from 2.5 V to 5.5 V
  - V_{OUT} range from 1.8 V to 3.3 V
  - Low noise and high PSRR
  - Adjustable output voltage through I^2C
  - Up to 300-mA output current
- 4.0-mm × 4.0-mm 24-pin VQFN with wettable flanks

2 Applications

- Automotive camera modules
  - Surround view camera modules
  - Rear view camera modules
  - Driver monitor camera modules
  - Power over coax (POC) camera modules
  - E-mirror camera modules
  - Front view camera modules

3 Description

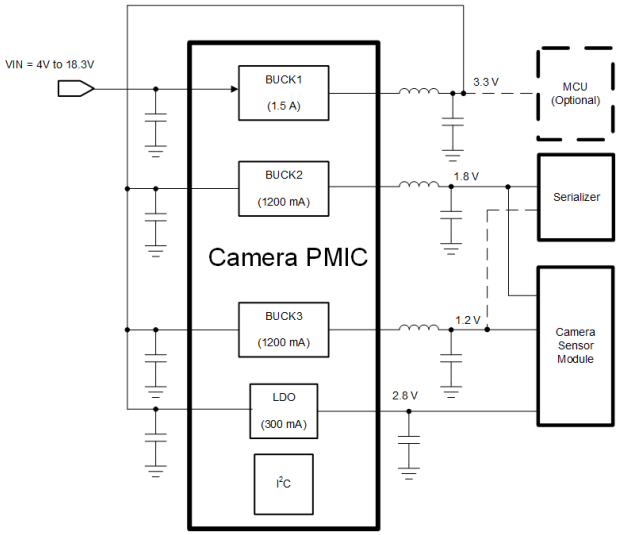
The TPS650332-Q1 device is a highly integrated power management IC for automotive camera modules. This device combines three step-down converters and one low-dropout (LDO) regulator. The BUCK1 step-down converter has an input voltage range up to 18.3 V for connections to power over coax (PoC). All converters operate in a forced fixed-frequency PWM mode. The LDO can supply 300 mA and operate with an input voltage range from 2.5 V to 5.5 V. The step-down converters and the LDO have separate voltage inputs that enable maximum design and sequencing flexibility.

The TPS650332-Q1 is available in a 24-pin VQFN package (4.00 mm × 4.00 mm).

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPS650332-Q1	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TPS650332-Q1 Application Circuit

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (September 2022)	Page
• Made cosmetic changes to registers with addresses 1Ah, 1Bh, 1Ch, 1Dh, 1Fh, 20h, 21h, 22h, 23h, 24h, 25h, and 26h	43

5 Pin Configuration and Functions

Figure 5-1 shows the 24-pin QFN pin assignments.

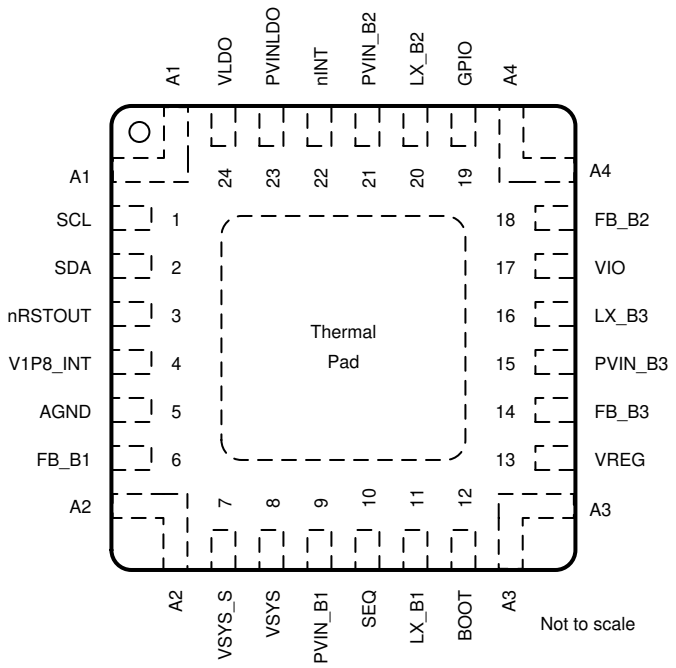


Figure 5-1. TPS650332-Q1 24-Pin QFN (Top View)

Table 5-1. Pin Functions

NO.	NAME	TYPE	DESCRIPTION
1	SCL	I	I2C Clock Line
2	SDA	I/O	I2C Data Line
3	nRSTOUT	O	Reset Output
4	V1P8_INT	O	Internal Reference Voltage - For Internal Use Only
5	AGND	GND	Analog Ground
6	FB_B1	I	BUCK1 (Mid Voltage Step-Down Converter) Feedback
7	VSYS_S	PWR	Device Input Power for Safety (Connect externally to the VSYS pin)
8	VSYS	PWR	Device Input Power (Connect externally to the VSYS_S pin)
9	PVIN_B1	PWR	BUCK1 (Mid Voltage Step-Down Converter) Input Voltage. Apply the voltage on PVIN_B1 at the same time or after the voltage on VSYS is applied.
10	SEQ	I	Sequence Control Pin
11	LX_B1	O	BUCK1 (Mid Voltage Step-Down Converter) Switch Node
12	BOOT	O	BOOTCAP pin for BUCK1 (Mid Voltage Step-Down Converter)
13	VREG	O	Gate Drive LDO Output for BUCK1 (Mid Voltage Step Down Converter)
14	FB_B3	I	BUCK3 (Low Voltage Step-Down Converter) Feedback
15	PVIN_B3	PWR	BUCK3 (Low Voltage Step-Down Converter) Input Voltage. Apply the voltage on PVIN_B3 at the same time or after the voltage on VSYS is applied.
16	LX_B3	O	BUCK3 (Low Voltage Step-Down Converter) Switch Node
17	VIO	I	IO Supply Voltage pin
18	FB_B2	I	BUCK2 (Low Voltage Step-Down Converter) Feedback
19	GPIO	I/O	General Purpose Input/Output

Table 5-1. Pin Functions (continued)

NO.	NAME	TYPE	DESCRIPTION
20	LX_B2	O	BUCK2 (Low Voltage Step-Down Converter) Switch Node
21	PVIN_B2	PWR	BUCK2 (Low Voltage Step-Down Converter) Input Voltage. Apply the voltage on PVIN_B2 at the same time or after the voltage on VSYS is applied.
22	nINT	O	Interrupt Request Output
23	PVINLDO	PWR	LDO Input Voltage. Apply the voltage on PVINLDO at the same time or after the voltage on VSYS is applied.
24	VLDO	O	LDO Output Voltage
A1-A4	Corner Anchors	GND	Corner Anchors for package stability (internally connected to the Power Pad)
	PowerPad™	GND	Device Thermal Pad and PGND connection. Must be connected to main ground plane for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

POS			MIN	MAX	UNIT
4.1.1	Input voltage	VSYS, VSYS_S	-0.3	20	V
4.1.2		PVIN_B1	-0.3	20	
4.1.3		FB_B1	-0.3	5.5	
4.1.4		BOOT	-0.3	V_{LX_B1} + 5.5	
4.1.5		PVIN_B2, PVIN_B3, PVINLDO	-0.3	6.0	
4.1.6		FB_B2, FB_B3	-0.3	5.5	
4.1.7		VIO	-0.3	5.5	
4.1.8		SEQ	-0.3	20	
4.1.9		GPIO	-0.3	5.5	
4.1.10	Output voltage	LX_B1 (2)	-2.0	20	V
4.1.10.a		LX_B1 for spikes with a pulse width less than 10ns (2)	-2.0	22	
4.1.11		LX_B2, LX_B3 (2)	-2.0	6.0	
4.1.12		VLDO	-0.3	5.0	
4.1.13		VREG	-0.3	5.5	
4.1.14		V1P8_INT	-0.3	1.98	
4.1.15		SDA, SCL	-0.5	5.0	
4.1.16		nINT, nRSTOUT	-0.3	5.0	
4.1.20	Operating junction temperature, T_J			150	°C
4.1.21	Storage temperature, T_{stg}			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Minimum voltage reduces from -2.0V to -0.4V at T_A = 125ºC.

6.2 ESD Ratings

POS					VALUE	UNIT
4.2.1	$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
4.2.2			Charged device model (CDM), per AEC Q100-011	Corner pins (1, 6, 7, 12, 13, 18, 19 and 24)	±750	
4.2.3				Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

POS			MIN	NOM	MAX	UNIT
4.3.1	VSYS, VSYS_S	Input voltage	4		18.3	V
4.3.2	PVIN_B1	BUCK1 Input Voltage (PVIN_B1 ≤ VSYS/ VSYS_S)	4		18.3	V
4.3.3	BOOT	BUCK1 Bootstrap Pin	0		V_{LX_B1} + 5.0	V
4.3.4	LX_B1	BUCK1 Switch Node Pin(1)	-0.5		20.0	V
4.3.5	C_{PVIN_B1}	BUCK1 Input Capacitance	6.8	10		uF

6.3 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

POS			MIN	NOM	MAX	UNIT
4.3.6	FB_B1	BUCK1 Feedback pin	0		4.0	V
4.3.7	FB_B2, FB_B3	BUCK2 and BUCK3 Feedback pin	0		2.0	V
4.3.8	PVIN_B2, PVIN_B3	BUCK2 and BUCK3 Input Voltage Pins	0		5.5	V
4.3.9	LX_B2, LX_B3	BUCK2 and BUCK3 Switch Node Pins(1)	-0.5		5.5	V
4.3.10	C_{PVIN_B2}, C_{PVIN_B3}	BUCK2 and BUCK3 Input Capacitance	6.8	10		uF
4.3.11	PVINLDO	LDO Input Voltage	0		5.5	V
4.3.12	LDOOUT	LDO Output Voltage Range	0		3.3	V
4.3.13	C_{LDOOUT}	LDO Output Capacitance	1		4	uF
4.3.14	VREG		0		5.0	V
4.3.15	V1P8_INT		0		1.85	V
4.3.16	VIO		0		3.3	V
4.3.17	nINT, nRSTOUT, SEQ, GPIO		0		3.3	V
4.3.18	SCL and SDA		0		3.3	V
4.3.19	T_A	Operating free-air temperature	–40		125	°C
4.3.20	T_J	Operating junction temperature	–40		150	°C

(1) Minimum voltage reduces from -0.5V to -0.4V at T_A = 125ºC.

6.4 Thermal Information

THERMAL METRIC(1)		RGE VQFN 24 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	31.7	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	27.2	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	10.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.5	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Reference System

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.5.1	VSYS , VSYS_S	Operating Input Voltage		4		18.3	V
4.5.5	I_{Q_ON}	Quiescent Current - On State	Measured on the VSYS pin, VSYS ≥ 4.0V, VSYS and VSYS_S are connected together			10	mA

6.5 Reference System (continued)

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.5.6	I_{Q_OFF}	Quiescent Current - Off State	VSYS = 0V to 3.5V, slow ramp rate, VSYS and VSYS_S are connected together		100	150	uA
4.5.7	C_{VSYS}	VSYS external Capacitance		4.0	10		uF
4.5.8	V_{V1P8_INT}	Internal LDO Output Voltage	VIN = VSYS	1.7	1.85	2.0	V
4.5.9	C_{V1P8_INT}	V1P8_INT external Capacitance		0.68	1	1.4	uF
4.5.10	V_{VREG}	BUCK1 Gate Drive LDO	VIN = VSYS ≥ 4.3	4.0	4.5	5.0	V
4.5.12	C_{VREG}	VREG external Capacitance		0.68	1	1.4	uF

6.6 BUCK1 Converter

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.6.1	V_{IN}	Input voltage		4		18.3	V
4.6.6	I_{OFF_STATE}	Off State Current	BUCK1 disabled measured at PVIN_B1			40	µA
4.6.7	$V_{OUT\_LOW\_VIN}$ (1)	Output voltage - Low VIN Range	V_{IN} = 4.0V to 18.3V	2.5	3.3	3.5	V
4.6.8	$V_{OUT\_HIGH\_VIN}$ (1)	Output voltage - High VIN Range	V_{IN} = 4.5V to 18.3V	2.5	3.8	4.0	V
4.6.10	$V_{OUT\_ACCURACY\_DC}$	DC Output Voltage Accuracy	V_{IN} = 12.0V, I_{OUT} = I_{OUT_MAX}, V_{OUT} = 2.5V to 4.0V	–1.5		1.5	%
4.6.11	$V_{OUT\_ACCURACY\_TOT}$	Total Output Voltage Accuracy (DC + AC)	V_{IN} = 4.0V to 18.3V for V_{OUT} = 3.3V, V_{IN} = 4.5V to 18.3V for V_{OUT} = 3.8V, I_{OUT} = 1mA to 50% of I_{OUT_MAX} in 1us for both cases.	–5		5	%
4.6.12	R_{FB_INPUT}	Feedback input impedance	Converter enabled	100		900	KΩ
4.6.13	$V_{LOAD\_REGULATION}$	DC Load Regulation	V_{IN} = 12.0V, V_{OUT} = 3.3V, I_{OUT} = 0 to I_{OUT_MAX}			0.1	%/A
4.6.15	$V_{LINE\_REGULATION}$	DC Line Regulation	V_{IN} = 4.0V to 18.3V, I_{OUT} = 500mA and 1500mA			1.5	%
4.6.16	$V_{LOAD\_TRANSIENT}$	Load Transient	V_{IN} = 12.0V, V_{OUT} = 3.3V, I_{OUT} = 1mA to 50% of I_{OUT_MAX} in 1us,			100	mV
4.6.18	$V_{LINE\_TRANSIENT}$	Line Transient	V_{IN} = 4.0V to 18.3V in 100uS, V_{OUT} = 3.3V, I_{OUT} = 1mA and I_{OUT_MAX},			100	mV
4.6.19	$V_{RIPPLE\_PWM\_PtoP}$	PWM Mode	C_{OUT} = 10uF, X7R, ESR = 10mohms, L = 1.5uH, DCR = 110 mΩ, QFN Package			20	mV
4.6.21	I_{OUT_MAX} (1)	Maximum Operating Current				1.5	A
4.6.22	$I_{CURRENT\_LIMIT}$	Short Circuit Current Limit	V_{IN} = (7.5 x 10^6) x L, V_{OUT} = 0V	1.8	2.4	3	A
4.6.23	R_{DSON_HS}	High Side MOSFET On Resistance	Measured Pin to Pin			300	mΩ
4.6.24	R_{DSON_LS}	Low Side MOSFET On Resistance	Measured Pin to Pin			165	mΩ
4.6.25	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is disabled, $R_{DISCHARGE}$ Setting = '00'		off		KΩ
4.6.26	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is disabled, $R_{DISCHARGE}$ Setting = '01'	60	125	250	Ω
4.6.27	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is disabled, $R_{DISCHARGE}$ Setting = '10'	120	250	450	Ω

6.6 BUCK1 Converter (continued)

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.6.28	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is disabled, $R_{DISCHARGE}$ Setting = '11'	240	500	850	Ω
4.6.34	$L_{SW\_1\_5}$	Output Inductance		1.0	1.5	2.0	µH
4.6.36	C_{OUT_LC}	LC Filter Output capacitance		6.8	10	14	µF
4.6.37	C_{BOOT}	Boot capacitance		0.07	0.1	0.13	µF
TIMING CHARACTERISTICS							
4.6.50	$V_{IN\_RAMP\_TIME\_NORMAL}$	Input voltage Ramp Time under normal operating conditions	Input voltage controlled by a pre-regulator. PVIN_B1 = 0V to 10V	0.1		100	ms
4.6.51	$V_{IN\_RAMP\_TIME\_HOT\_PLUG}$	Input voltage Ramp Time based on a Hot Plug scenario	Hot Plug occurring at the input of the device. PVIN_B1 = 0V to 10V.			1	V/µs
4.6.53	t_{START}	Start Time	Time from completion of I2C command to output voltage at 10%			200	µs
4.6.54	t_{RAMP}	Ramp Time	Measured from 10% to 90% of target value	200	480	800	µs
SWITCHING CHARACTERISTICS							
4.6.60	f_{SW}	Switching Frequency	PWM - Fixed Frequency	2.18	2.3	2.42	MHz
4.6.62	f_{SS_EN}	Converter Switching Frequency with Spread Spectrum Enabled		2.05		2.55	MHz
4.6.63	A_{DITHER_TRIAN}	Dither Amplitude of Spread Spectrum Clock for a Triangular Dither pattern				150	KHz
4.6.64	f_{DITHER_STEP}	Dither Step frequency				18	KHz
4.6.65	M_{DITHER}	Dither Slope of Spread Spectrum Clock				4.5	KHz/µs

(1) Load current capability depends on the Input Voltage and Output Voltage. The following formula can be used to determine the limits. $V_{IN} = [(R_{DSON} + L_{DCR}) * I_{LOAD}] + (V_{OUT} / 0.9)$

6.7 BUCK2 and BUCK3 Converters

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.7.1	V_{IN}	Input voltage		2.5		5.5	V
4.7.3	I_{OFF_STATE}	Off State Current	2.5V ≤ PVINx ≤ 5.5V. BUCKx Disabled, measured at PVIN_Bx			25	µA
4.7.5.a	V_{OUT}	Output voltage -	V_{IN} = 2.5V to 4.0V	0.9	1.2	1.9	V
4.7.10	$V_{OUT\_ACCURACY\_DC}$	DC Output Voltage Accuracy - Overall	V_{IN} = 3.3V, I_{OUT} = I_{OUT_MAX}, V_{OUT} = 0.9V to 1.9V	–1.5		1.5	%
4.7.11	$V_{OUT\_ACCURACY\_DC\_1\_8V}$	DC Output Voltage Accuracy	V_{IN} = 3.3V, I_{OUT} = I_{OUT_MAX}, V_{OUT} = 1.8V			30	mV
4.7.12	$V_{OUT\_ACCURACY\_DC\_1\_2V}$	DC Output Voltage Accuracy	V_{IN} = 3.3V, I_{OUT} = I_{OUT_MAX}, V_{OUT} = 1.2V			20	mV
4.7.13	$V_{OUT\_ACCURACY\_TOT}$	Total Output Voltage Accuracy (DC + AC)	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.2V and 1.8V, I_{OUT} = 1mA to 50% of I_{OUT_MAX} in 1us	–5		5	%
4.7.14	R_{FB_INPUT}	Feedback input impedance	Converter enabled	100		900	KΩ
4.7.15	$V_{LOAD\_REGULATION}$	DC Load Regulation	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 0 to I_{OUT_MAX}			0.1	%/A
4.7.16	$V_{LINE\_REGULATION}$	DC Line Regulation	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.8V and 1.2V, I_{OUT} = 250mA and 1000mA			1.5	%

6.7 BUCK2 and BUCK3 Converters (continued)

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.7.18	$V_{LOAD\_TRANSIENT}$	Load Transient	V_{IN} = 3.8V, V_{OUT} = 1.8V and 1.2V, I_{OUT} = 1mA to 500mA in 1us,			50	mV
4.7.19	$V_{LINE\_TRANSIENT}$	Line Transient	V_{IN} = 2.5V to 5.5V in 50uS, V_{OUT} = 1.8V and 1.2V, I_{OUT} = 1mA and I_{OUT_MAX},			50	mV
4.7.20	$V_{RIPPLE\_PWM\_PtoP}$	PWM Mode	C_{OUT} = 10uF, X7R, ESR = 10mohms, L = 1uH, DCR = 60mohms, QFN Package			20	mV
4.7.22	I_{OUT_MAX}	Maximum Operating Current				1.2	A
4.7.23	$I_{CURRENT\_LIMIT}$	Short Circuit Current Limit	V_{IN} = 3.3V, V_{OUT} = 0V	1.6	2.2	2.8	A
4.7.26	R_{DSON_HS}	High Side MOSFET On Resistance	Measured Pin to Pin, V_{IN} = 3.8V			160	mΩ
4.7.27	R_{DSON_LS}	Low Side MOSFET On Resistance	Measured Pin to Pin, V_{IN} = 3.8V			80	mΩ
4.7.28	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is disabled, $R_{DISCHARGE}$ Setting = '00'.		off		KΩ
4.7.29	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is disabled, $R_{DISCHARGE}$ Setting = '01'.	60	125	200	Ω
4.7.30	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is disabled, $R_{DISCHARGE}$ Setting = '10'.	120	250	400	Ω
4.7.31	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is disabled, $R_{DISCHARGE}$ Setting = '11'.	240	500	800	Ω
4.7.37	L_{SW}	Output Inductance		0.68	1	1.2	µH
4.7.38	C_{OUT}	Output capacitance		6.8	10	12	µF
TIMING CHARACTERISTICS							
4.7.50	t_{START}	Start Time	Time from completion of I2C command to output voltage at 10%			200	µs
4.7.51	t_{RAMP}	Ramp Time	Measured from 10% to 90% of target value	200	480	800	µs
SWITCHING CHARACTERISTICS							
4.7.60	f_{SW}	Switching Frequency	PWM - Fixed Frequency	2.18	2.3	2.42	MHz
4.7.62	f_{SS_EN}	Converter Switching Frequency with Spread Spectrum Enabled		2.05		2.55	MHz
4.7.63	A_{DITHER_TRIAN}	Dither Amplitude of Spread Spectrum Clock for a Triangular Dither pattern				150	KHz
4.7.64	f_{DITHER_STEP}	Dither Step frequency				18	KHz
4.7.65	M_{DITHER}	Dither Slope of Spread Spectrum Clock				4.5	KHz/µs

6.8 Low Noise LDO

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.8.1.a	V_{IN}	Input voltage		2.5		5.5	V
4.8.3	V_{OUT}	Output voltage	V_{IN} = 2.5V to 3.8V	1.8		3.3	V
4.8.5	R_{Bypass}	Bypass resistance	V_{IN} = 3.3V, I_{OUT} = 100mA, LDO Bypass Enabled			1	Ω
4.8.6	$V_{OUT\_DC\_ACCURACY}$	Total DC accuracy including DC load and line regulation for all valid output voltages	For all valid operating conditions, measured after the output voltage has settled	–1%		1%	

6.8 Low Noise LDO (continued)

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.8.11	$V_{LOAD\_TRANSIENT}$	Load Transient	V_{IN} = 3.3V, V_{OUT} = 2.80V, I_{OUT} = 20% of I_{OUT_MAX} to 80% of I_{OUT_MAX} in 1us, C_{OUT} = 2.2uF	–25		25	mV
4.8.12	$V_{LINE\_TRANSIENT}$	Line Transient	VIN step = 600 mVPP, T_R = T_F = 10 µs, LDO not in dropout condition, I_{OUT} = 1mA and I_{OUT_MAX2}	–25		25	mV
4.8.13	$V_{DROPOUT}$	Dropout Voltage	For full V_{IN} range and max operating current		150	300	mV
4.8.18	$NOISE_{RMS}$	RMS Noise	f=100Hz to 100KHz, V_{IN} = 3.3V, I_{OUT} = 300mA, V_{OUT} = 2.8V and 1.8V		15		uV_{RMS}
4.8.19	I_{OUT_MAX1}	Maximum Operating Current low				150	mA
4.8.20	I_{OUT_MAX2}	Maximum Operating Current high				300	mA
4.8.21	$I_{CURRENT\_LIMIT1}$	Short Circuit Current Limit low	V_{IN} = 3.6V, V_{OUT} = 0VTested under a pulsed load condition	200		450	mA
4.8.22	$I_{CURRENT\_LIMIT2}$	Short Circuit Current Limit high	V_{IN} = 3.6V, V_{OUT} = 0VTested under a pulsed load condition	400		900	mA
4.8.23	I_{IN_RUSH}	LDO inrush current	VIN = 3.3V and then LDO is enabled.			650	mA
4.8.24	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is disabled, $R_{DISCHARGE\_OTP}$ = '00'	35	50	65	KΩ
4.8.25			Active only when converter is disabled, $R_{DISCHARGE\_OTP}$ = '01'	60	125	200	Ω
4.8.26			Active only when converter is disabled, $R_{DISCHARGE\_OTP}$ = '10'	120	250	400	Ω
4.8.27			Active only when converter is disabled, $R_{DISCHARGE\_OTP}$ = '11'	240	500	800	Ω
4.8.28	I_{Qoff}	Quiescent current off mode				2	µA
4.8.29	I_{Qon}	Quiescent current on mode	Iload = 0A			40	µA
4.8.31	C_{IN}	Input filtering capacitance		1			µF
4.8.32	C_{OUT}	Output filtering capacitance		1		4	µF
4.8.34	C_{ESR}	Filtering capacitor ESR max	1MHz to 10MHz		10	20	mΩ
TIMING CHARACTERISTICS							
4.8.50	t_{START}	Start Time	Time from completion of I2C command to output voltage at 10%			150	us
4.8.52	t_{RAMP}	Ramp Time	Measured from 0.5V to 90% of target value			350	us
4.8.53	t_{RAMP_SLEW}	Ramp Up Slew Rate	Measured from 0.5V to 90% of target value			25	mv/us
4.8.54	t_{REG}	Time to regulation	From 90% to within +-2% of target			100	us

6.9 VIO

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.9.1	V_{IN_VIO}	VIO Input voltage	VIO present at the same time or after VREG is present	1.8		3.6	V

6.9 VIO (continued)

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.9.2	I_{IN_VIO}	Maximum input current on the VIO pin (assumes all inputs, outputs and input/outputs sourcing 2mA of current simultaneously)	VIO = 3.6V			8	mA
4.9.3	$I_{IN\_VIO\_STATIC}$	Maximum input current on the VIO pin when all buffers are static.	VIO = 3.6V			10	µA
4.9.5	C_{IN_VIO}	Internal input pin capacitance on VIO pin				30	pF

6.10 SEQ

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.10.1	V_{IL}	Low-level input voltage	VBIAS = VIO			0.54	V
4.10.2	V_{IH}	High-level input voltage	VBIAS = VIO	1.26			V
4.10.3	I_{LKG}	Input leakage current	VBIAS = VIO			4	µA
4.10.4	R_{INT_PD}	Internal pull-down resistance	V_{SEQ} = 1V	1		2	MΩ
4.10.5	C_{IN}	Internal input pin capacitance				10	pF
TIMING CHARACTERISTICS							
4.10.10	$t_{DEGLITCH}$	Deglitch time on both rising and falling edges		8		12	µs

6.11 nINT

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.11.1	V_{OL_OD}	Low-level output voltage (open drain)	VIO = 1.8V, I_{OL} = 2mA			0.4	V
4.11.2	$R_{INT\_PU\_OD}$	Internal pull-up resistor		7		15	kΩ
4.11.3	V_{OL_PP}	Low-level output voltage (push-pull)	VIO = 1.8V, I_{OL} = 2mA			0.4	V
4.11.4	V_{OH_PP}	High-level output voltage (push-pull)	VIO = 1.8V, I_{OH} = 2mA	0.8			V
4.11.5	I_{LKG}	Input leakage current	VIO = 3.6V			1	µA
TIMING CHARACTERISTICS							
4.11.11	t_{R_PP}	Output Voltage Rise Time (push-pull)	VIO = 1.8, C_{LOAD} = 10pF, Measured from 10% to 90%			5	ns
4.11.12	t_{F_PP}	Output Voltage Fall Time (push-pull)	VIO = 1.8, C_{LOAD} = 10pF, Measured from 90% to 10%			10	ns

6.12 nRSTOUT

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.12.1	V_{OL_OD}	Low-level output voltage (open drain)	VIO = 3.6V, I_{OL} = 2mA			0.4	V
4.12.2	$R_{INT\_PU\_OD}$	Internal pull-up resistor		7		15	kΩ
4.12.3	V_{OL_PP}	Low-level output voltage (push pull)	VIO = 3.6V, I_{OL} = 2mA			0.4	V

6.12 nRSTOUT (continued)

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.12.4	V_{OH_PP}	High-level output voltage (push pull)	VIO = 3.6V, I_{OL} = 2mA	0.8 *VIO			V
4.12.5	V_{OL_PP}	Low-level output voltage (push pull)	VIO = 1.8V, I_{OL} = 2mA			0.4	V
4.12.6	V_{OH_PP}	High-level output voltage (push pull)	VIO = 1.8V, I_{OL} = 2mA	0.7*VIO			V
4.12.7	I_{LKG}	Input leakage current	VIO = 3.6V			1	µA
TIMINIG CHARACTERISTICS							
4.12.10	t_{R_PP}	Output voltage rise time	VIO = 1.8V, C_{LOAD} = 10pF, Measured from 10% to 90%			5	ns
4.12.11	t_{F_PP}	Output voltage fall time	VIO = 1.8V, C_{LOAD} = 10pF, Measured from 90% to 10%			5	ns
4.12.12	$t_{DEGLITCH\_READBACK}$	Deglitch time on both rising and falling edges		8	10	12	µs

6.13 GPIO

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.13.1	V_{IL}	Low-level input voltage				0.54	V
4.13.2	V_{IH}	High-level input voltage		1.26			V
4.13.3	I_{LKG}	Input leakage current				1	µA
4.13.4	C_{IN}	Internal input pin capacitance				10	pF
4.13.5	V_{OL}	Low-level output voltage	VIO = 3.6V, I_{OL} = 2mA			0.4	V
4.13.6	V_{OH}	High-level output voltage	VIO = 3.6V, I_{OH} = 2mA	0.8			V
4.13.8	R_{PD}	Internal pull-down resistance when configured as an input	VIO = 1.8V or 3.3V	100	400		KΩ
TIMING CHARACTERISTICS							
4.13.11	t_R	Output Voltage Rise Time	VIO = 1.8, C_{LOAD} = 10pF, Measured from 10% to 90%			5	ns
4.13.12	t_F	Output Voltage Fall Time	VIO = 1.8, C_{LOAD} = 10pF, Measured from 90% to 10%			5	ns

6.14 I²C Interface

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.14.1	V_{IL_I2C}	Input Low Voltage Threshold				0.4	V
4.14.2	V_{IH_I2C}	Input High Voltage Threshold		1.26			V
4.14.3	V_{OL_I2C}	DATA output low voltage	V_{PULL_UP} = 1.8V and 3.3V			0.4	V
4.14.4	I_{LKG_I2C}	Leakage Current	V_{PULL_UP} = 1.8V and 3.3V		0.01	0.3	µA
4.14.9	C_I	Capacitance for each I/O pin	Standard Mode, Fast Mode, Fast Mode Plus and High-Speed Mode			10	pF
4.14.10	C_B	Load capacitance on SDA and SCL	Standard Mode and Fast Mode			400	pF
4.14.11	C_B	Load capacitance on SDA and SCL	Fast Mode Plus			550	pF
4.14.12	C_B	Load capacitance on SDA and SCL	High Speed Mode (3.4MHz)			100	pF

6.15 Monitor Ref Sys

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.15.1	$VSYS_{UVLO\_R}$	Internal under-voltage lockout threshold	VSYS rising	3.5		3.9	V
4.15.2	$VSYS_{UVLO\_HYS}$	Internal under-voltage lockout threshold hysteresis	VSYS falling	100	150	200	mV
4.15.3	$VSYS_{OVP}$	Supply over-voltage protection threshold	VSYS rising	18.5			V
4.15.4	$VSYS_{OVP\_HYS}$	Supply over-voltage protection threshold hysteresis	VSYS falling	0.925	1.0	1.2	V

6.16 Monitor BUCK1

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.16.1	VBUCK1_UV	MV BUCK1 under-voltage detection threshold expressed in percentage of target regulation voltage	VBUCK1 falling, Slew Rate = 50mV/ms	–5	**–4**	–3	%
4.16.2				–5.5	–4.5	–3.5	
4.16.3				–6	–5	–4	
4.16.4				–6.5	–5.5	–4.5	
4.16.5	VBUCK1_UV_HYS	MV BUCK1 under-voltage detection threshold hysteresis expressed in percentage of absolute value of VBUCK1_UV	VBUCK1 rising, Slew Rate = 50mV/ms		1.05		%
4.16.6	VBUCK1_OV	MV BUCK1 over-voltage detection threshold expressed in percentage of target regulation voltage	VBUCK1 rising, Slew Rate = 50mV/ms	3	**4**	5	%
4.16.7				3.5	4.5	5.5	
4.16.8				4	5	6	
4.16.9				4.5	5.5	6.5	
4.16.10	VBUCK1_OV_HYS	MV BUCK1 over-voltage detection threshold hysteresis expressed in percentage of absolute value of VBUCK1_OV	VBUCK1 falling, Slew Rate = 50mV/ms		0.95		%
4.16.11	VBUCK1_OVP	MV BUCK1 over-voltage protection detection threshold expressed in percentage of target regulation voltage	VBUCK1 rising, Slew Rate = 50mV/ms	9	12	15	%
4.16.12	VBUCK1_OVP_HYS	MV BUCK1 over-voltage protection detection threshold hysteresis expressed in percentage of absolute value of VBUCK1_OVP	VBUCK1 falling, Slew Rate = 50mV/ms		0.9		%
4.16.13	VBUCK1_SCG	MV BUCK1 short-circuit detection threshold	VBUCK1 falling, Slew Rate = 50mV/ms	250	300	350	mV
4.16.14	VBUCK1_SCG_HYS	MV BUCK1 short-circuit detection threshold hysteresis	VBUCK1 rising, Slew Rate = 50mV/ms		100		mV
TIMING CHARACTERISTICS							
4.16.20	$t_{BUCK1\_VMON\_DEG}$	MV BUCK1 output voltage fault detection deglitch time	Measured from UV/OV/OVP event to respective status bit being set	20		24	µs

6.17 Monitor BUCK2

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.17.1	VBUCK2_UV	LV BUCK2 under-voltage detection threshold expressed in percentage of target regulation voltage	VBUCK2 falling, Slew Rate = 50mV/ms	–5	**–4**	–3	%
4.17.2				–5.5	–4.5	–3.5	
4.17.3				–6	–5	–4	
4.17.4				–6.5	–5.5	–4.5	
4.17.5	VBUCK2_UV_HYS	LV BUCK2 under-voltage detection threshold hysteresis expressed in percentage of absolute value of VBUCK2_UV	VBUCK2 rising, Slew Rate = 50mV/ms		1.05		%
4.17.6	VBUCK2_OV	LV BUCK2 over-voltage detection threshold expressed in percentage of target regulation voltage	VBUCK2 rising, Slew Rate = 50mV/ms	3	**4**	5	%
4.17.7				3.5	4.5	5.5	
4.17.8				4	5	6	
4.17.9				4.5	5.5	6.5	
4.17.10	VBUCK2_OV_HYS	LV BUCK2 over-voltage detection threshold hysteresis expressed in percentage of absolute value of VBUCK2_OV	VBUCK2 falling, Slew Rate = 50mV/ms		0.95		%
4.17.11	VBUCK2_OVP	LV BUCK2 over-voltage protection detection threshold expressed in percentage of target regulation voltage	VBUCK2 rising, Slew Rate = 50mV/ms	9	12	15	%
4.17.12	VBUCK2_OVP_HYS	LV BUCK2 over-voltage protection detection threshold hysteresis expressed in percentage of absolute value of VBUCK2_OVP	VBUCK2 falling, Slew Rate = 50mV/ms		0.9		%
4.17.13	VBUCK2_SCG	LV BUCK2 short-circuit detection threshold	VBUCK2 falling, Slew Rate = 50mV/ms	250	300	350	mV
4.17.14	VBUCK2_SCG_HYS	LV BUCK2 short-circuit detection threshold hysteresis	VBUCK2 rising, Slew Rate = 50mV/ms		100		mV
TIMING CHARACTERISTICS							
4.17.20	$t_{BUCK2\_VMON\_DEG}$	LVBUCK2 output voltage fault detection deglitch time	Measured from UV/OV/OVP event to respective status bit being set	20		24	µs

6.18 Monitor BUCK3

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.18.1	VBUCK3_UV	LV BUCK3 under-voltage detection threshold expressed in percentage of target regulation voltage	VBUCK3 falling, Slew Rate = 50mV/ms	–5	**–4**	–3	%
4.18.2				–5.5	–4.5	–3.5	
4.18.3				–6	–5	–4	
4.18.4				–6.5	–5.5	–4.5	
4.18.5	VBUCK3_UV_HYS	LV BUCK3 under-voltage detection threshold hysteresis expressed in percentage of absolute value of VBUCK3_UV	VBUCK3 rising, Slew Rate = 50mV/ms		1.05		%
4.18.6	VBUCK3_OV	LV BUCK3 over-voltage detection threshold expressed in percentage of target regulation voltage	VBUCK3 rising, Slew Rate = 50mV/ms	3	**4**	5	%
4.18.7				3.5	4.5	5.5	
4.18.8				4	5	6	
4.18.9				4.5	5.5	6.5	

6.18 Monitor BUCK3 (continued)

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.18.10	VBUCK3_OV_HYS	LV BUCK3 over-voltage detection threshold hysteresis expressed in percentage of absolute value of VBUCK3_OV	VBUCK3 falling, Slew Rate = 50mV/ms		0.95		%
4.18.11	VBUCK3_OVP	LV BUCK3 over-voltage protection detection threshold expressed in percentage of target regulation voltage	VBUCK3 rising, Slew Rate = 50mV/ms	9	12	15	%
4.18.12	VBUCK3_OVP_HYS	LV BUCK3 over-voltage protection detection threshold hysteresis expressed in percentage of absolute value of VBUCK3_OVP	VBUCK3 falling, Slew Rate = 50mV/ms		0.9		%
4.18.13	VBUCK3_SCG	LV BUCK3 short-circuit detection threshold	VBUCK3 falling, Slew Rate = 50mV/ms	250	300	350	mV
4.18.14	VBUCK3_SCG_HYS	LV BUCK3 short-circuit detection threshold hysteresis	VBUCK3 rising, Slew Rate = 50mV/ms		100		mV
TIMING CHARACTERISTICS							
4.18.20	$t_{BUCK3\_VMON\_DEG}$	LV BUCK3 output voltage fault detection deglitch time	Measured from UV/OV/OVP event to respective status bit being set	20		24	µs

6.19 Monitor LDO

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.19.1	LDO_UV	LDO under-voltage detection threshold expressed in percentage of target regulation voltage	LDO falling, Slew Rate = 50mV/ms	–4.5	**–3.5**	–2.5	%
4.19.2				-5.0	-4.0	-3.0	
4.19.3				-5.5	-4.5	-3.5	
4.19.4				-6.0	-5.0	-4.0	
4.19.5	LDO_UV_HYS	LDO under-voltage detection threshold hysteresis expressed in percentage of absolute value of VLDO_UV	LDO rising, Slew Rate = 50mV/ms		1.05		%
4.19.6	LDO_OV	LDO over-voltage detection threshold expressed in percentage of target regulation voltage	LDO rising, Slew Rate = 50mV/ms	3	**4**	5	%
4.19.7				3.5	4.5	5.5	
4.19.8				4	5	6	
4.19.9				4.5	5.5	6.5	
4.19.10	LDO_OV_HYS	LDO over-voltage detection threshold hysteresis expressed in percentage of absolute value of VLDO_OV	LDO falling, Slew Rate = 50mV/ms		0.95		%
4.19.11	LDO_OVP	LDO over-voltage protection detection threshold expressed in percentage of target regulation voltage	LDO rising, Slew Rate = 50mV/ms	9	12	15	%
4.19.12	LDO_OVP_HYS	LDO over-voltage protection detection threshold hysteresis expressed in percentage of absolute value of VLDO_OVP	LDO falling, Slew Rate = 50mV/ms		0.9		%
4.19.13	LDO_SCG	LDO short-circuit detection threshold	LDO falling, Slew Rate = 50mV/ms	250	300	350	mV
4.19.14	LDO_SCG_HYS	LDO short-circuit detection threshold hysteresis	LDO rising, Slew Rate = 50mV/ms		100		mV

6.19 Monitor LDO (continued)

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING CHARACTERISTICS							
4.19.20	$t_{LDO\_VMON\_DEG}$	LDO output voltage fault detection deglitch time	Measured from UV/OV/OVP event to respective status bit being set	20		24	µs

6.20 Monitor Temperature Sensor

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.20.1	T_{WARM_TH}	Thermal warning threshold	T_J rising	110	120	130	°C
4.20.2	$T_{WARM\_TH\_HYS}$	Thermal warning threshold hysteresis	T_J falling	8	10	12	°C
4.20.3	$T_{SD\_FAULT\_TH}$	Thermal immediate shutdown threshold	T_J rising	140	150	160	°C
4.20.4	$T_{SD\_FAULT\_HYS}$	Thermal immediate shutdown hysteresis	T_J falling	8	10	12	°C

6.21 Monitor VREG

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.21.1	VREG_UV	VREG under-voltage detection threshold	VREG falling	2.576	2.8	3.024	V
4.21.2	VREG_UV_HYS	VREG under-voltage detection threshold hysteresis	VREG rising		37		mV
4.21.3	VREG_OVP	VREG over-voltage protection detection threshold	VREG rising	5.428	5.9	6.372	V
4.21.4	VREG_OVP_HYS	VREG over-voltage protection detection threshold hysteresis	VREG falling		37		mV
TIMING CHARACTERISTICS							
4.21.10	$t_{MVGD\_VMON\_DEG}$	VREG output voltage fault detection deglitch time	Measured from UV/OVP event to respective status bit being set	20		24	µs

Monitor Loss of Ground

Over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
TIMING CHARACTERISTICS							
4.22.10	t_{LOG_DEG}	Loss of ground detection deglitch time		10		12	µs

6.22 Monitor V1P8_INT

Over operating free-air temperature range (unless otherwise noted)

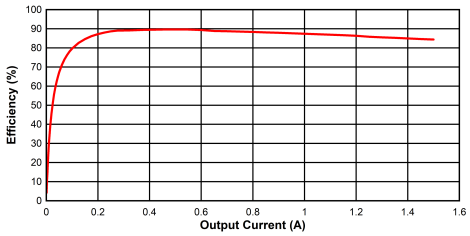
POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS							
4.24.1	V1P8_INT_UV	V1P8_INT under-voltage detection threshold	V1P8_INT falling	1.55		1.62	V

6.22 Monitor V1P8_INT (continued)

Over operating free-air temperature range (unless otherwise noted)

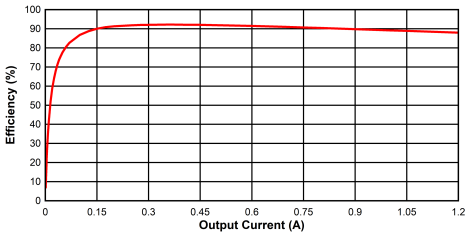
POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.24.2	V1P8_INT_UV_HYS	V1P8_INT under-voltage detection threshold hysteresis	V1P8_INT rising	30		55	mV
4.24.3	V1P8_INT_OVP	V1P8_INT over-voltage protection detection threshold	V1P8_INT rising	2.14		2.23	V
4.24.4	V1P8_INT_OVP_HYS	V1P8_INT over-voltage protection detection threshold hysteresis	V1P8_INT falling	35		55	mV
TIMING REQUIREMENTS							
4.24.10	$t_{V1P8\_VMON\_DEG}$	V1P8_INT output voltage fault detection deglitch time	Measured from UV/OVP event to respective status bit being set	10		50	µs

6.23 Typical Characteristics



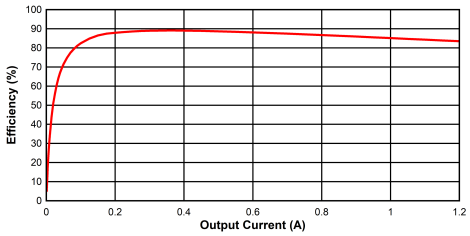
V_{IN} = 9.0 V V_{OUT} = 3.3 V T_A = 25°C

Figure 6-1. Efficiency (BUCK1) vs Output Current



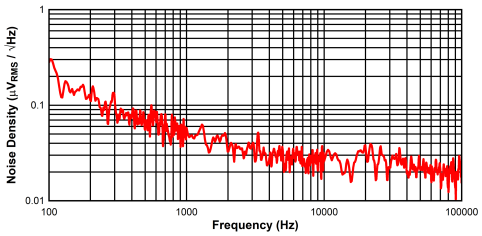
V_{IN} = 3.3 V V_{OUT} = 1.8 V T_A = 25°C

Figure 6-2. Efficiency (BUCK2) vs Output Current



V_{IN} = 3.3 V V_{OUT} = 1.2 V T_A = 25°C

Figure 6-3. Efficiency (BUCK3) vs Output Current



V_{IN} = 3.3 V V_{OUT} = 2.8 V I_{OUT} = 300 mA T_A = 25°C

Figure 6-4. LDO Noise Density

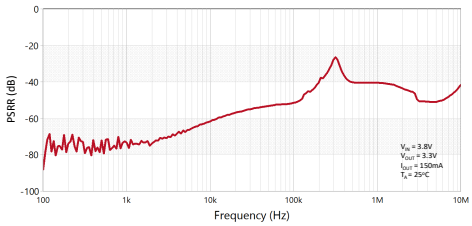


Figure 6-5. LDO PSRR (150 mA)

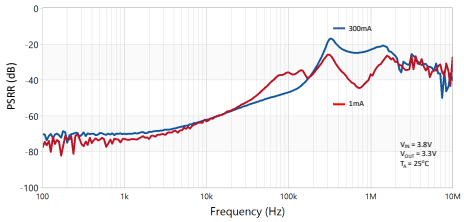


Figure 6-6. LDO PSRR

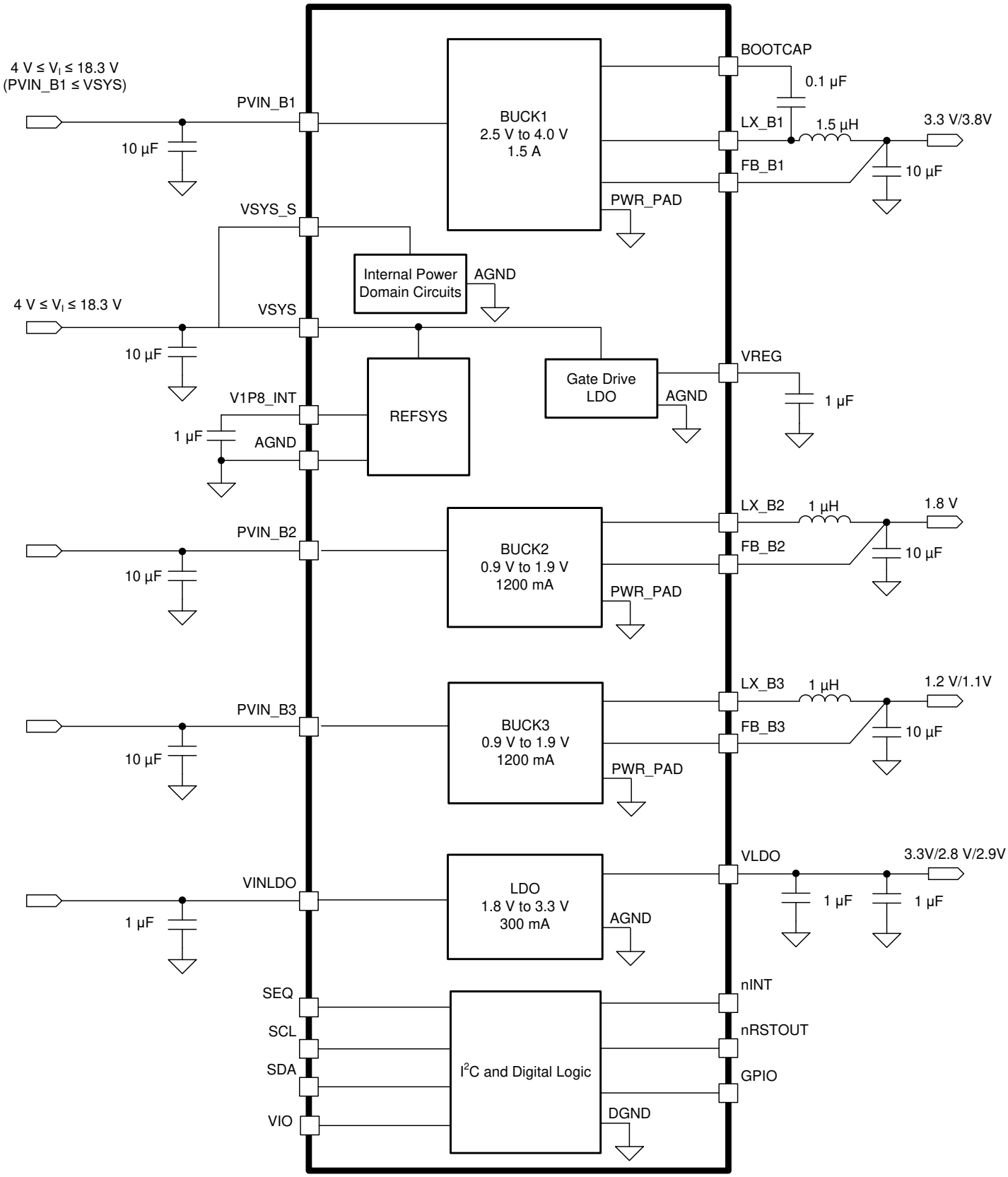
7 Detailed Description

7.1 Overview

The TPS650332-Q1 provides three step-down converters and one low dropout regulator. This device is intended, but not limited, to powering automotive surround view camera sensors.

The step-down converters have a spread spectrum feature. The spread spectrum clock (SSC) feature modulates the frequency so as to spread the power that may cause EMI.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Mid-Vin Step-Down Converter (BUCK1)

The TPS650332-Q1 synchronous step-down converter (BUCK1) uses a Forced Fixed Frequency topology.

7.3.1.1 Pulse Width Modulation (PWM)

The Forced Fixed Frequency topology operates in pulse width modulation (PWM) mode. In PWM mode, the converter operates at its nominal switching frequency. The block diagram for the Mid-Vin converter is shown in BUCK Block Diagram.

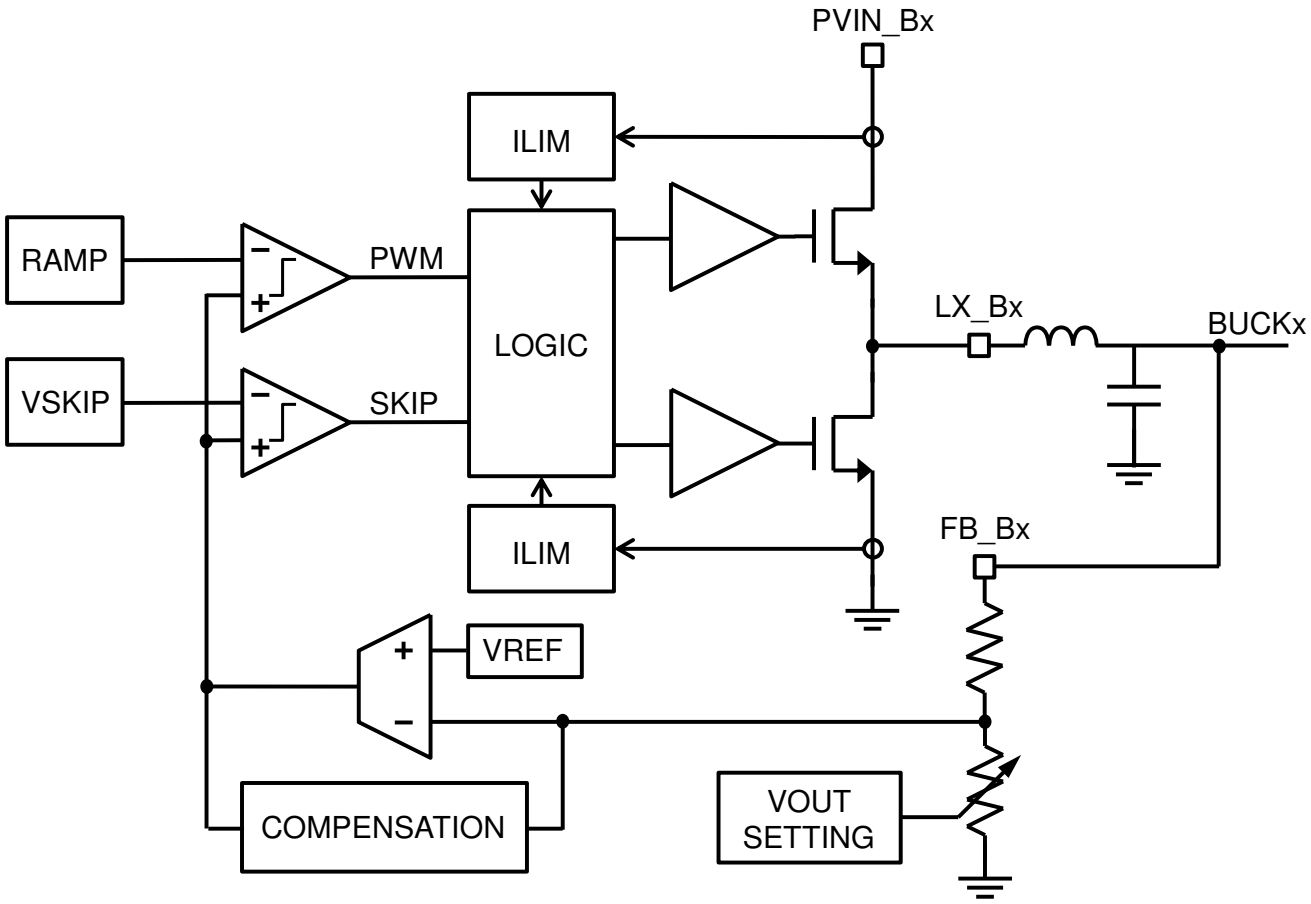


Figure 7-1. BUCK Block Diagram

7.3.1.2 Output Voltage Settings

The output voltage settings of the step-down converter are controlled through I^2C by setting the appropriate bits of the voltage select register. These register settings can be used to modify the output voltage from its default setting. Changing of the output voltage in real time is not recommended. Disable the converter before changing the output voltage setting.

7.3.1.3 Output Discharge

The step-down converter has an internal discharge resistor. If set through the register, the discharge resistor activates automatically when the converter is disabled.

7.3.1.4 Soft-Start Circuitry

The TPS650332-Q1 has an internal soft-start circuit. The soft-start circuit monotonically ramps up the output voltage and reaches the nominal output voltage during a specified ramp time. This feature avoids excessive

inrush current and creates a smooth output voltage slope. Figure 7-2 shows how the output voltage ramp up is controlled during a soft-start event.

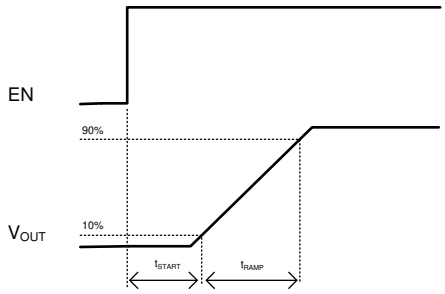


Figure 7-2. Soft Start

7.3.1.5 PVIN_B1 Undervoltage Lockout (UVLO)

The PVIN_B1 pin has an Undervoltage Lockout (UVLO) circuit different from the VSYS Undervoltage Lockout circuit. The PVIN_B1 UVLO can be used to keep all the regulators off until the PVIN_B1 UVLO threshold is surpassed. The PVIN_B1 UVLO threshold is programmable using I^2C. By programming the PVIN_B1 UVLO rising threshold higher than the VSYS UVLO threshold, a potential hiccup situation can be avoided as voltage on VSYS is rising. Once the PVIN_B1 UVLO rising threshold is surpassed, the PVIN_B1 UVLO falling threshold is monitored in order to detect a fault condition on the input voltage. The PVIN_B1 UVLO falling threshold must be set at least 0.5 V less than the rising threshold.

7.3.2 Low-Vin Step-Down Converters (BUCK2 and BUCK3)

The TPS650332-Q1 synchronous step-down converters, BUCK2 and BUCK3, use a Forced Fixed Frequency topology.

7.3.2.1 Pulse Width Modulation (PWM)

The Forced Fixed Frequency topology operates in pulse width modulation (PWM) mode. The converter operates at its nominal switching frequency in PWM mode. The block diagram for the Low-Vin converter is shown in Figure 7-3.

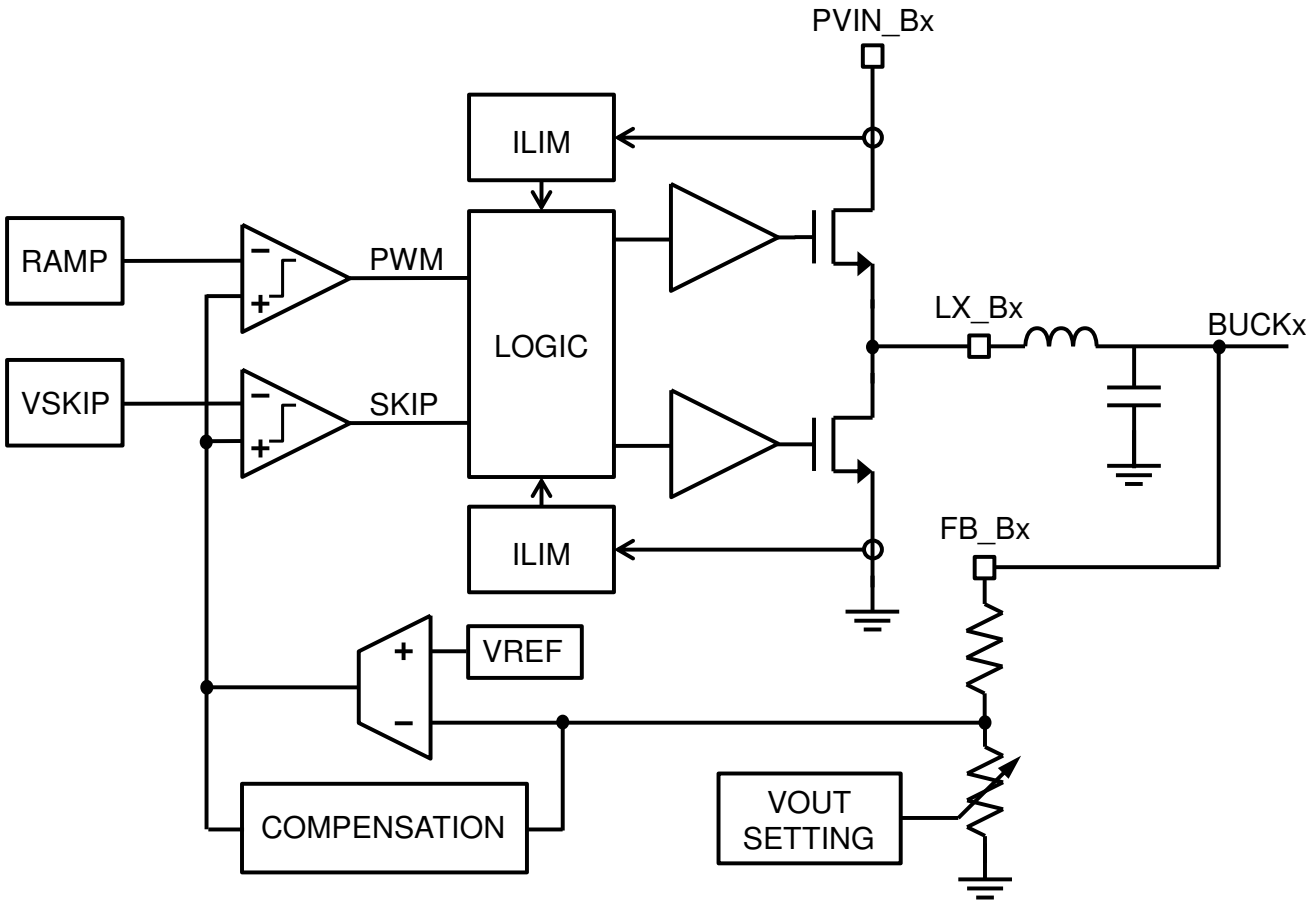


Figure 7-3. BUCK Block Diagram

7.3.2.2 Output Voltage Settings

The output voltage settings of the step-down converter are controlled through the I^2C by setting the appropriate bits of the voltage select register. Changing of the output voltage in real time is not recommended. Disable the converter before changing the output voltage setting.

7.3.2.3 Output Discharge

The step-down converter has an internal discharge resistor. If set through the register, the discharge resistor activates automatically when the converter is disabled.

7.3.2.4 Soft-Start Circuitry

The TPS650332-Q1 has an internal soft-start circuit. The soft-start circuit monotonically ramps up the output voltage and reaches the nominal output voltage during a specified ramp time. This feature avoids excessive inrush current and creates a smooth output voltage slope. Figure 7-4 shows how the output voltage ramp up is controlled during a soft-start event.

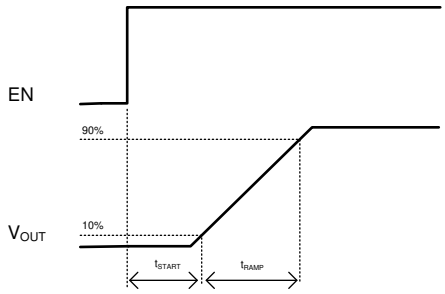


Figure 7-4. Soft Start

7.3.3 Linear Low Drop-Out (LDO) Regulator

The TPS650332-Q1 has an LDO regulator designed to provide flexibility in system design. The LDO regulator has a dedicated input voltage pin that can be tied to the output of BUCK1 or the output of another voltage source.

The LDO can be configured using a register setting to operate in a 'By-Pass Mode'. In 'By-Pass Mode', the LDO operates as a load switch.

7.3.3.1 Low Output Noise

The LDO regulator is designed to meet the requirements of sensitive analog circuits by providing low noise with high PSRR operation. Any internal noise at the reference voltage is reduced by a first-order low-pass RC filter before it is passed to the output buffer stage.

7.3.3.2 Output Voltage Setting

The output voltage settings of the LDO regulator are controlled through I^2C by setting the appropriate bits of the voltage select register. Changing of the output voltage in real time is not recommended. Disable the regulator before changing the output voltage setting.

7.3.3.3 Output Discharge

The LDO regulator has a separate output discharge to ground. If set through the register, the discharge resistor activates automatically when the LDO regulator is disabled. The discharge to ground also applies when the LDO is configured in the 'By-Pass Mode' and it is disabled.

7.3.4 Power On/Off Sequencing

This device has a programmable power On/Off sequence. Sequencing can be programmed as a timed event or based on the power good of the regulators.

7.3.5 SEQ pin

The SEQ pin can be used to initiate a power on or off sequence. A high level on this pin starts the power on sequence. Driving the pin low starts the power down sequence. If the SEQ pin is not used for power sequencing, driving it high or low is not necessary. An internal pull-down resistor maintains the logic level to the inactive state.

The device has a factory programmable option that latches the level of the SEQ pin. If this feature is enabled, an internal SEQ signal is asserted high upon application of power on the VSYS pin that can be used to start the power up sequence. The actual level of the SEQ pin is ignored for 60 ms. After 60 ms, the device acts on the state of the SEQ pin such that if it is driven low, a power down sequence is started. The internal SEQ signal stays low until VSYS drops below the device UVLO when the SEQ pin is driven low.

7.3.6 nRSTOUT pin

The nRSTOUT pin can be used to keep a peripheral in the reset condition until the desired voltage rails are active. The nRSTOUT pin is part of the power on or off sequence and its timing is programmable. The pin can be configured as push-pull or open drain. As an open-drain output, the pull-up resistor is integrated as part of the device and the pull-up voltage comes from the VIO pin.

7.3.7 nINT pin

The nINT output indicates when a fault has occurred. The I^2C bus can be used to query the device to determine the exact nature of the fault. The nINT pin can be configured as push-pull or open-drain. As an open-drain output, the pull-up resistor is integrated as part of the device. The pull-up voltage is connected to the VIO pin.

7.3.8 General Purpose Input/Output (GPIO) Pin

The GPIO pin can be configured as an input or an output. As an output, the GPIO pin operates in a push-pull configuration. The push-pull output is biased from the VIO pin and can be used as part of the power up sequence to enable an external voltage rail. If configured as an output, the GPIO has to be enabled by setting the GPIO_STATE register bit to a '1'.

As an input, it can be used as a control/enable for the power sequencing. When configured as an input, this pin has an internal pull-down resistor.

7.3.9 Input/Output Voltage (VIO) Pin

The Input/Output voltage (VIO) pin defines the voltage rail for the pins listed below. The voltage on this pin cannot be present prior to applying voltage on the VSYS pin. The voltage can be applied at the same time or after the voltage on the VREG pin is present. If the voltage on this pin is supplied by an external voltage rail, the voltage must be present before the nRSTOUT signal is de-asserted.

1. nRSTOUT pin (both push-pull and open-drain)
2. nINT pin (both push-pull and open-drain)
3. GPIO pin buffer when configured as an output.

7.4 Safety Description

7.4.1 Safety Functions and Diagnostic Features

7.4.1.1 Overview

This device is intended for use in safety-relevant automotive and transportation applications. The following list of features are implemented.

- Voltage monitoring on all regulator outputs
- Regulator current limit
- Loss-of-ground monitoring
- Temperature monitoring
- Built-in self-tests
- Output error monitor on nRSTOUT pin and nINT pin
- Cyclic Redundancy Check (CRC) on Device NVM Contents and Device Configuration Registers
- CRC on I^2C Interface

Figure 7-5 shows the concept and assumptions of this device.

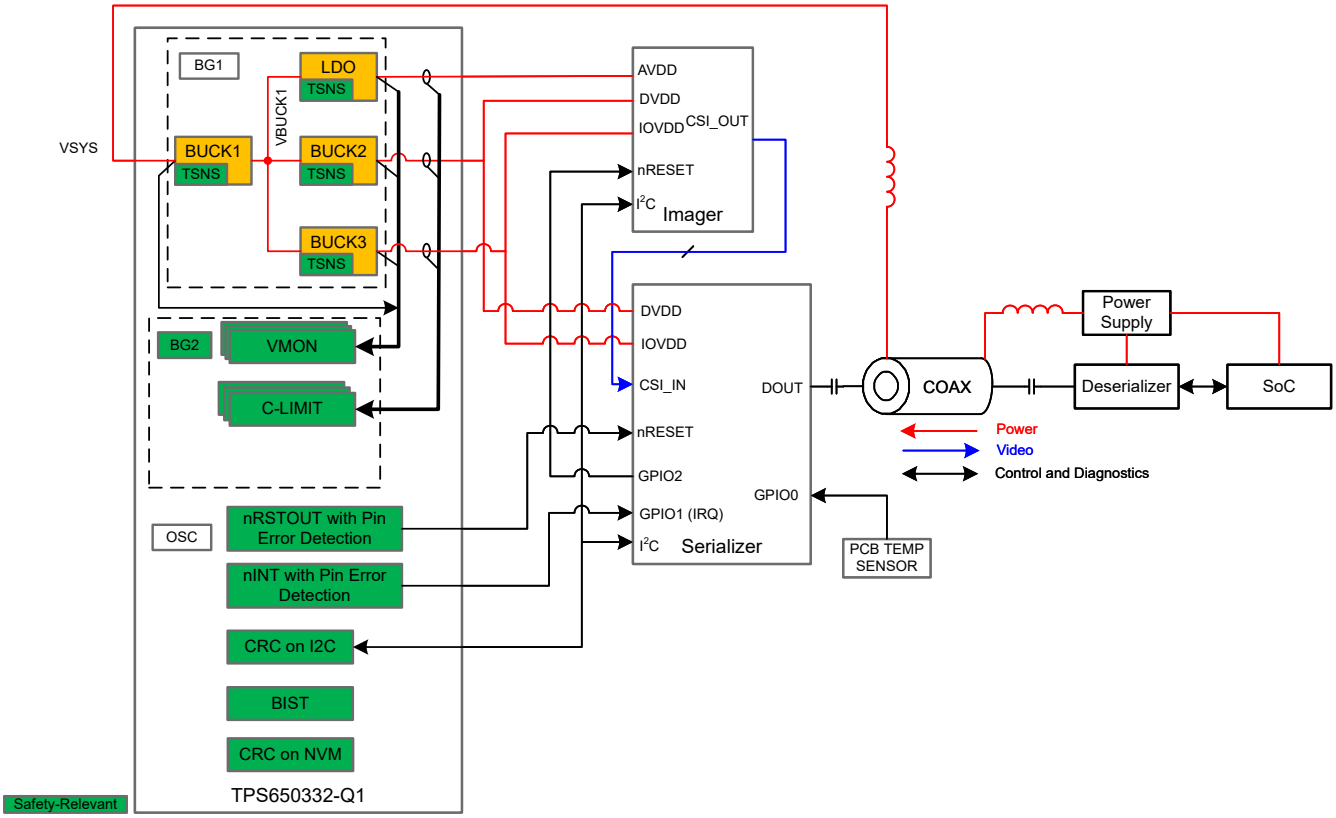


Figure 7-5. Safety Concept of the TPS650332-Q1

7.4.1.2 Device State Controller

The Finite State Machine (FSM) controls the transition of the device from the various states.

In the Safe State configuration, Priority 2 failures transition the state machine to the RESET State forcing a shutdown and Priority 3 failures generate an interrupt that transitions the state machine to the SAFE State.

7.4.1.2.1 State Machine - Remote MCU

OFF State:

- All regulator outputs are off

The device transitions from the OFF State to the RESET State if VSYS and VSYS_S exceed the $VSYS_{UVLO\_R}$ threshold.

RESET State:

- RESET State Entry
- Drives nRSTOUT low
- Resets all registers to their default state
- Loads the EEPROM

RESET State

- Runs the System ABIST

RESET State Exit

- Waits for all PMIC rails to discharge below the specified limit except for the LDO output if the LDO_PREBIAS_CTRL bit is set to '0'
- Waits for the temperature to fall below the WARM threshold level unless the WARM_THR_STARTUP_CTRL bit is set to '0'
- Waits for the BUCK1 PVIN_UVLO rising threshold to be exceeded

ACTIVE State:

- The internal state machine powers up all external rails enabled by the EEPROM settings and in the order defined by the sequencing registers (SEQ_TRIG_BUCKx, SEQ_TRIG_LDO, SEQ_TRIG_nRSTOUT, SEQ_TRIG_GPIO, BUCKx_SEQ_DLY, LDO_SEQ_DLY, nRSTOUT_SEQ_DLY, GPIO_SEQ_DLY)
- Runs the ABIST on all enabled rails
- Drives the nINT pin high
- The nRSTOUT pin is kept low for a programmed amount of time [RESET extension time, nRSTOUT_DLY_ON] to ensure proper reset of the MCU/Serializer before it is pulled high

SAFE State:

- If a Priority 3 fault is detected, the device enters the Safe State
- The nRSTOUT pin remains at a high level
- The nINT pin is pulled low
- The external rails remain enabled

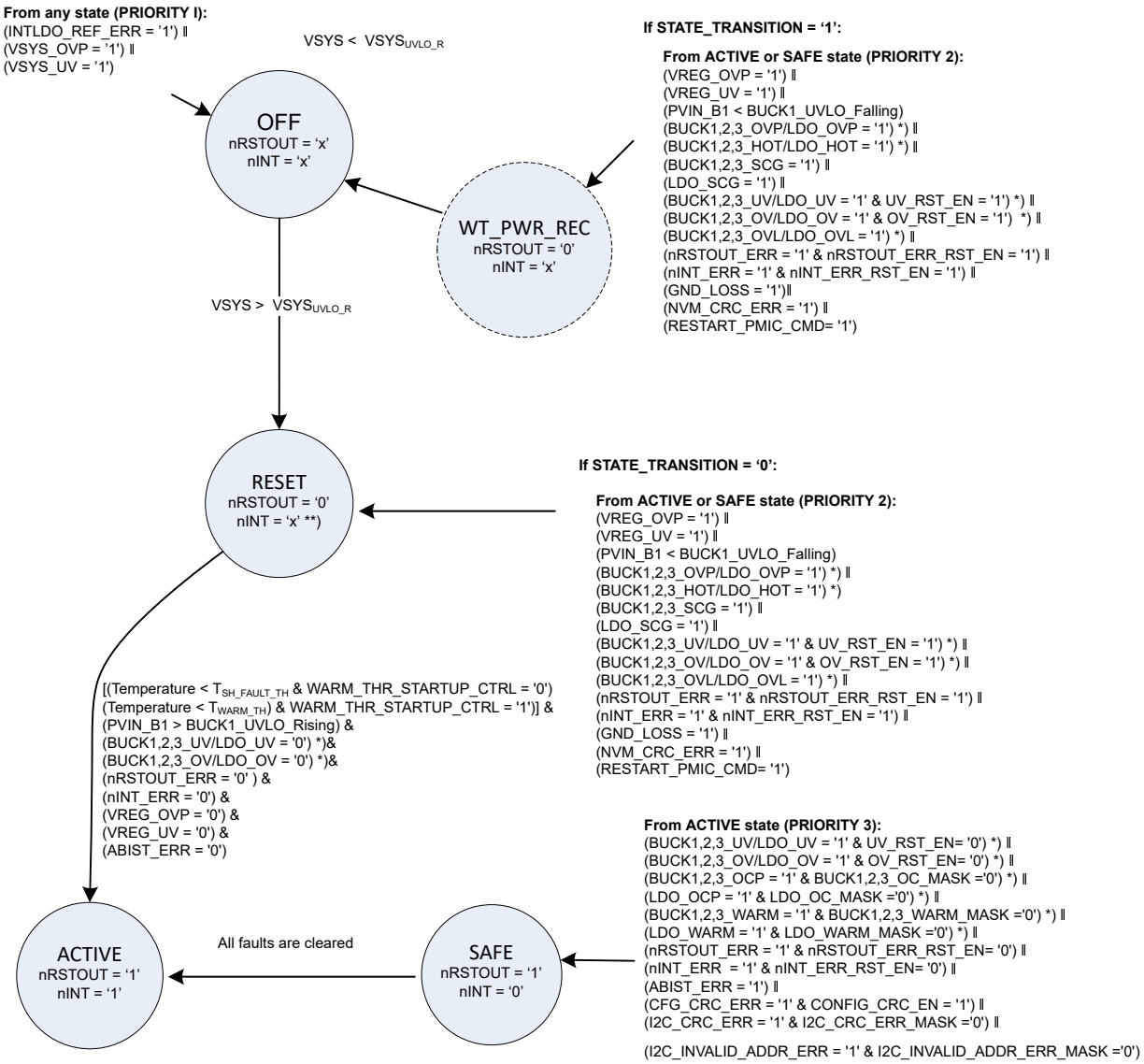
If all Priority 3 faults are cleared, the device transitions to the ACTIVE State. See state diagram for details.

If the fault detected is a Priority 2 fault and the STATE_TRANSITION bit is set to '0', the device transitions to the RESET State

WT_PWR_REC State:

- If a Priority 2 fault is detected and the STATE_TRANSITION bit is set to '1', the part enters the WT_PWR_REC state
- nRSTOUT is driven low
- All regulator outputs are disabled

In order to exit the WT_PWR_REC State, the voltage on VSYS and VSYS_S must go below the $VSYS_{UVLO\_THRESHOLD}$ so that the device can enter the OFF State.



NOTE:
Voltages on all rails must be less than the SCG threshold before the rail can be enabled. Exception is LDO, if LDO_PREBIAS_CTRL = '0'
*) applicable to enabled rails only
**) the state of the nINT-pin is dependent on fault-conditions and VIO-supply
1. All rails are turend off under OVP, HOT, or SCG Condition, regardless of which state the device is in. It cannot be enabled until the faulty condition no longer exists.
2. In SAFE state, the MCU may have access to I2C of the TPS65033x
4. For following faults if the mask is being set, the . FSM won't change state and nINT pin won't be pulled low but the status bit is set:
   BUCK1,2,3_OC/LDO_OC , BUCK1,2,3_WARM/ LDO_WARM, I2C-errors
5. ABIST_ERR is a superset of (OR-combination) of ABIST_LDO_ACK, ABIST_BUCK3_ACK, ABIST_BUCK2_ACK, ABIST_BUCK1_ACK and SYSTEM_ERR_ACK.

Figure 7-6. The TPS650332-Q1 device state diagram

7.4.1.3 Voltage Monitoring (VMON)

7.4.1.3.1 Input Supply Voltage and Internal Reference Monitoring

The device includes two separate power domains — one for regulation circuitry and the other for monitoring circuitry in order to ensure that voltage monitors are not affected by the voltage regulators. All internal regulators and references for regulation circuitry and monitoring circuitry are powered from a supply at VSYS pin and VSYS_S pin, respectively.

The input supply voltage is monitored for undervoltage and overvoltage events. If an overvoltage or undervoltage is detected on VSYS and VSYS_S or both, the device turns off all voltage regulators (including the internal regulators and references) and goes into the OFF state.

Critical internal regulators and references such as VREG and V1P8_INT are monitored at all times. Proper operation of the device relies on these internal regulators and references to be within their defined range.

If the V1P8_INT internal reference is outside its defined range, an internal reference error is detected and transitions the state machine to the OFF state.

The V1P8_INT and VREG rails require adequate decoupling capacitance for proper operation. Missing decoupling capacitance may cause the rails to not regulate properly. In case of the V1P8_INT, the device may not be able to set status bits and may enter an undefined state. To mitigate the effect in case of a failure on the decoupling capacitor, the system integrator may add an additional capacitor on both of these rails.

7.4.1.3.2 Regulator Output Voltage Monitoring

The output of the three switched-mode regulators and the linear regulator are monitored for undervoltage, overvoltage, and an overvoltage protection event as described in Figure 7-7.

If the output voltage exceeds the configurable OV-threshold with respect to the configured output voltage and if OV_RST_EN='1', then the device enters either the REST State or the WT_PWR_REC State (depending on the setting of the STATE_TRANSITION bit), and forces the nRSTOUT and nINT pins to be pulled low.

If the output voltage exceeds the configurable OV-threshold with respect to the configured output voltage and if OV_RST_EN='0' , the device enters the SAFE State and forces the nINT pin to be pulled low.

The MCU must clear the bit by writing a '1' to the respective _OV_ACK-error-bit.

If the output voltage falls below the configurable UV threshold with respect to the configured output voltage and if UV_RST_EN='1', then the device enters either the REST State or the WT_PWR_REC State (depending on the setting of the STATE_TRANSITION bit), and forces the nRSTOUT and nINT pins to be pulled low.

If the output voltage falls below the configurable UV threshold with respect to the configured output voltage and if UV_RST_EN='0', the device enters the SAFE State, forcing the nINT pin to be pulled low.

The MCU must clear the bit by writing a '1' to the respective _UV_ACK-error-bit.

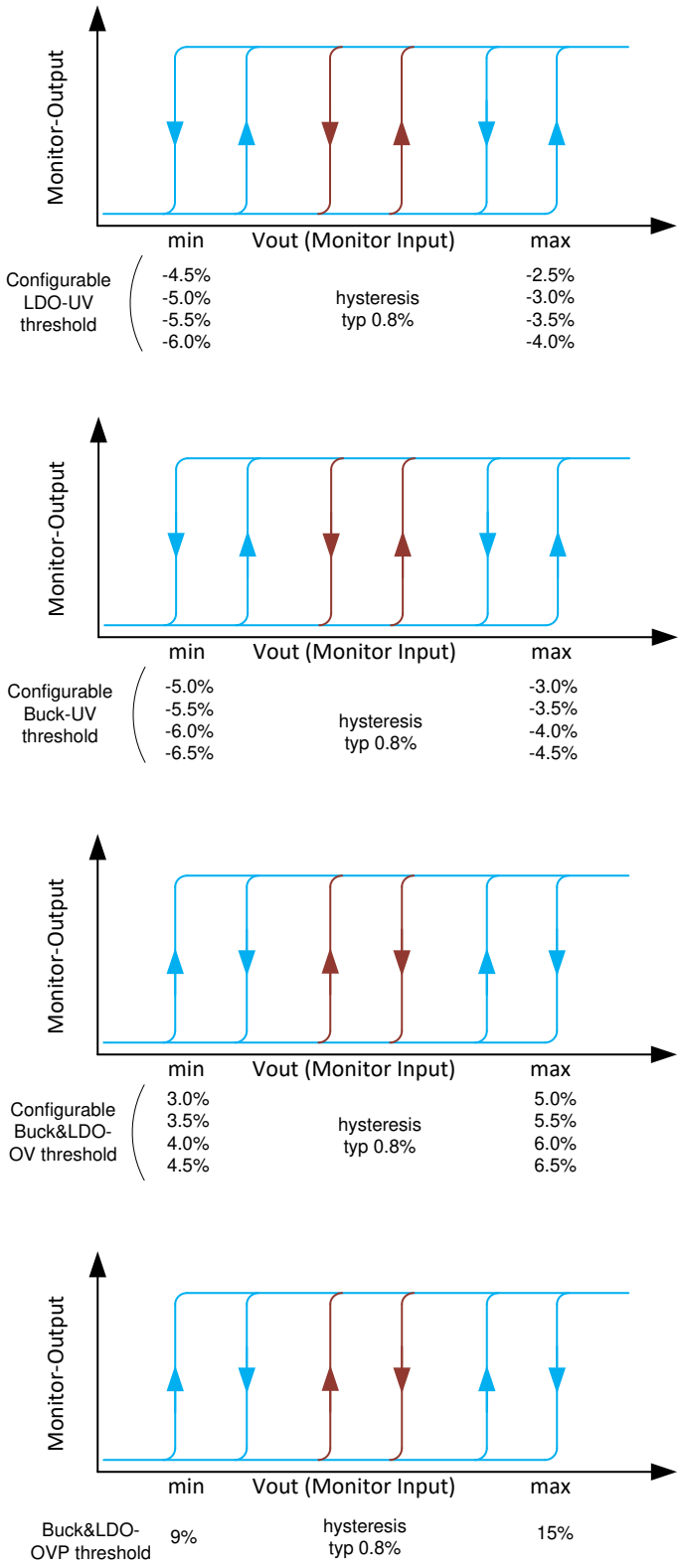


Figure 7-7. Voltage monitoring scheme for regulator output

7.4.1.4 Regulator current limit

All regulators include a current-limit circuit to protect the internal power MOSFETs from an over-current event. Each current-limit circuit limits the output current of the respective regulator when an over-current event occurs and the corresponding status bit (BUCKx_OCP_ACK or LDO_OCP_ACK) is set. If the corresponding _OCP_MASK bit is set to 0 (not masked), the device transitions to the SAFE State and pulls down the nINT pin. The MCU must clear the bit by writing a '1' to the respective _OCP_ACK bit.

The combination of an over-current and an undervoltage is considered an over-load-condition. If this condition occurs, the device sets a corresponding status bit (BUCKx_OVL_STATUS or LDO_OVL_STATUS) and the device transitions to either the REST State or the WT_PWR_REC State (depending on the setting of the STATE_TRANSITION bit), and forces the nRSTOUT and nINT pins to be pulled low.

If the fault is no longer present, the MCU can clear the bit by writing a '1' to the respective error-bit.

7.4.1.5 Short Circuit to Ground (SCG) detection

All regulators include a short circuit to ground detection. If the output voltage falls below the threshold voltage defined by VBUCKx_SCG or LDO_SCG, the corresponding status bit (BUCKx_SCG_STATUS or LDO_SCG_STATUS) is set and the device transitions to either the REST State or the WT_PWR_REC State (depending on the setting of the STATE_TRANSITION bit), and forces the nRSTOUT and nINT pins to be pulled low.

If the fault is no longer present, the MCU can clear the bit by writing a '1' to the respective error-bit.

7.4.1.6 Overload Fault Detection

The short circuit current limit value for each voltage regulator sets the threshold for the over current protection fault. The undervoltage threshold discussed in the Voltage Monitoring section sets the threshold for the undervoltage fault. In the event that both an overcurrent fault and an undervoltage fault are detected, an overload protection fault is generated. The overload protection fault detects an overload condition that does not trigger the short to ground fault.

7.4.1.7 Loss-of-ground monitoring

The loss-of-ground detection circuit monitors the voltage difference between the ground for the analog circuitry (V_{AGND}) and the ground for the digital circuitry (V_{DGND}). If the difference is outside the defined range, i.e., $| V_{AGND} - V_{DGND}| \geq [V_{LOG\_TH}]$ for a duration longer than the deglitch time t_{LOG_DEG}, the device shuts down all regulators and goes into the REST State or the WT_PWR_REC State (depending on the setting of the STATE_TRANSITION bit), and forces the nRSTOUT and nINT pins to be pulled low.

If the fault is no longer present, the MCU can clear the bit by writing a '1' to the GND_LOSS_ERR_STATUS bit.

7.4.1.8 Temperature Monitoring and Regulator Current Limit

The device has temperature monitors near all regulators. Each monitor has a warning threshold and a hot threshold with separate status bits assigned.

The BUCK1_WARM_ACK, BUCK2_WARM_ACK, BUCK3_WARM_ACK, or LDO_WARM_ACK status bit is set to 1 when the temperature rises above a defined level, T_{WARM_TH}. The BUCKx_WARM_MASK and LDO_WARM_MASK bit determines the device behavior during an over-temperature event in the regulators. If the corresponding _WARM_MASK bit is set to '0', the device pulls down the nINT pin to alert the external MCU and transitions into the SAFE State .

The MCU must clear the bit by writing a '1' to the corresponding _WARM_ACK bit.

When the temperature rises above the critical level defined by $T_{SD\_FAULT\_TH}$, the device disables the affected regulator and sets the BUCK1_HOT_STATUS, BUCK2_HOT_STATUS, BUCK3_HOT_STATUS, or LDO_HOT_STATUS bit. An over-temperature condition in any step-down regulator triggers a device transition to either the RESET State or the WT_PWR_REC State (depending on the setting of the STATE_TRANSITION bit) and forces the nRSTOUT and nINT pins to be pulled low .

If the fault is no longer present, the MCU can clear the bit by writing a '1' to the corresponding _HOT_STATUS bit.

7.4.1.9 Output Error Monitor on nRSTOUT pin

The error detection circuit for nRSTOUT pin compares the actual logic level on the nRSTOUT pin against the intended logic level. The following occurs if a mismatch is detected between the two levels:

If nRSTOUT_ERR_RST_EN= ’0' then nRSTOUT_ERR_ACK is set and the device enters the SAFE state.

The MCU must clear the bit by writing a '1' to the corresponding nRSTOUT_ERR_ACK bit.

If nRSTOUT_ERR_RST_EN= ’1' then nRSTOUT_ERR_STATUS is set and the device enters either the RESET State or the WT_PWR_REC State.

If the fault is no longer present, the MCU can clear the bit by writing a '1' to the nRSTOUT_ERR_STATUS bit.

A deglitch time ($t_{DEGLITCH\_READBACK}$) allows for the output to settle, before being analyzed.

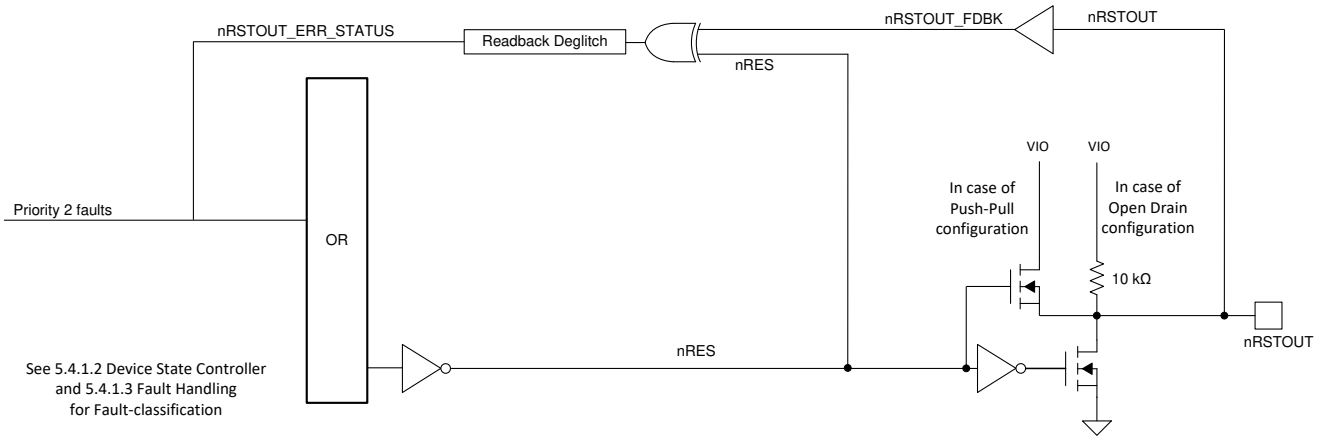


Figure 7-8. nRSTOUT Diagram

7.4.1.10 Output Error Monitor on nINT pin

The error detection circuit for nINT pin compares the actual logic level on the nINT pin against the intended logic level. The following occurs if a mismatch between the two levels is detected:

If nINT_ERR_RST_EN= ’0' then nINT_ERR_ACK is set and the device enters the SAFE state.

The MCU must clear the bit by writing a '1' to the corresponding nINT_ERR_ACK bit.

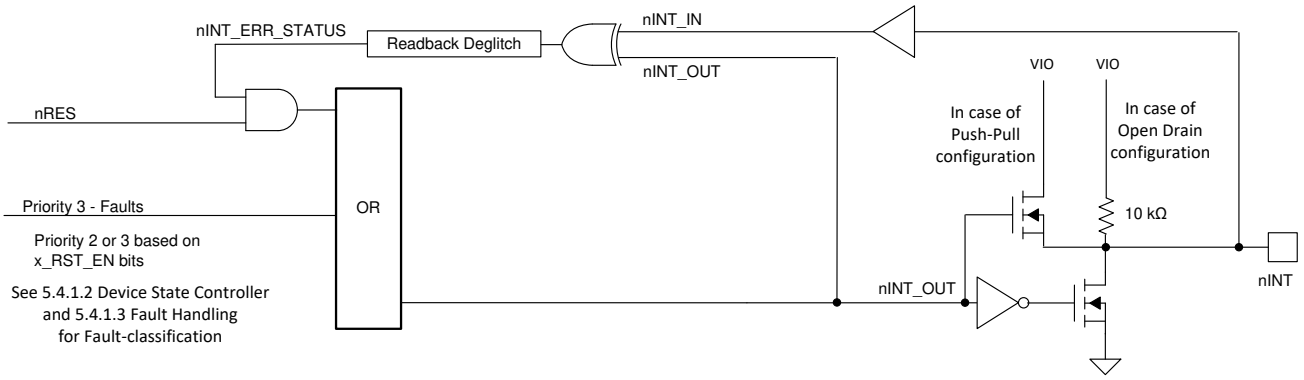
If nINT_ERR_RST_EN= ’1' then nINT_ERR_STATUS is set, nRSTOUT pin is pulled low and the device enters either the RESET State or the WT_PWR_REC State.

If the fault is no longer present, the MCU can clear the bit by writing a '1' to the nINT_ERR_STATUS bit.

A deglitch time ($t_{DEGLITCH\_READBACK}$) allows for the output to settle, before being analyzed.

Note

If a short on the nINT pin keeps the pin from going low, the MCU or device reading this pin is not able to detect that a fault has occurred. Therefore, it is recommended that the MCU periodically poll the register with the nINT_ERR_STATUS bit so that action can be taken if a mismatch occurs.



7.4.1.11 Restart PMIC Command

Writing to the RESTART_CMD register re-starts the device by transitioning the device to the RESET state. After the reset, the RESTART_CMD_STATUS bit is set, indicating the previous shutdown was due to restart command from the MCU.

The MCU can clear this bit by writing a '1' to the RESTART_CMD_STATUS bit.

7.4.1.12 Device Control Registers

Changes to the BUCK_LDO_CTRL and the GPIO_CTRL registers are protected by the CONTROL_LOCK Register. Before changes can be made to these registers, the CONTROL_ACCESS_CMD of 0xDD must be written to the CONTROL_LOCK Register to unlock the control registers. Once changes are complete, the CONTROL_ACCESS_CMD of 0x00 must be written to the CONTROL_LOCK Register to lock the control registers.

Note

Changes to these registers do not impact the Configuration CRC value stored in the CFG_REG_CRC Register.

7.4.1.13 Device Configuration Register Access Control

Write access to the device configuration registers is restricted via the CONFIG_LOCK register to avoid inadvertent writes to the device configuration registers. By default, the CONFIG_ACCESS_CMD is set to the write-access lock. The MCU must clear the lock before changing any device configuration registers. After the device configuration registers have been set to their desired values, set the CONFIG_ACCESS_CMD to the lock state to prevent changes to the configuration registers.

7.4.1.14 CRC on Device Configuration Registers

The device configuration registers are protected by CRC. The CRC controller in this device performs a CRC to verify the integrity of the configuration registers. If the MCU reconfigures the device configurations by changing the configuration registers, the MCU must calculate expected checksum value and write it to the CFG_REG_CRC register. The CRC controller calculates checksum value of the device that represents the actual content of the configuration registers. The CRC controller then compares this checksum value against what was written to the CFG_REG_CRC register by the MCU.

The CRC-protection is enabled by default. Prior to editing the configuration, the MCU must clear the CONFIG_CRC_EN bit. To re-enable the CRC check, the MCU must set the CONFIG_CRC_EN control bit. When enabled, the CRC controller continuously performs the CRC. The CRC controller detects a checksum error when the internally calculated checksum value of the device is not equal to the checksum-value in the CFG_REG_CRC register. If the CRC controller detects a checksum error, the devices sets the CFG_REG_CRC_ERR_ACK bit and goes into the SAFE State .

When the CFG_REG_CRC_ERR_ACK flag is set to 1, it remains so, even after the MCU disables the configuration CRC and reads out the CFG_REG_CRC_ERR_ACK flag. To exit the SAFE State . the MCU must clear the bit by writing a '1' to the CFG_REG_CRC_ERR_ACK bit.

The CRC controller uses a standard CRC-8 polynomial to calculate checksum-value, which is $X^8 + X^2 + X^1 + 1$. The CRC controller checks the CRC of these registers in a 8-bit string. The protected registers are as follows:

Table 7-1. CFG_CRC Register List

Register	Relevant bits	Byte #
LDO_GPIO_CFG	6:0	1
BUCK1_VOUT	4:0	2
BUCK1_UVLO	7:0	3
BUCK2_VOUT	4:0	4
BUCK3_VOUT	4:0	5
LDO_VOUT	4:0	6
DISCHARGE_SETTING	7:0	7
SEQ_TRIG_BUCK1	5:0	8
SEQ_TRIG_BUCK2	5:0	9
SEQ_TRIG_BUCK3	5:0	10
SEQ_TRIG_LDO	5:0	11
SEQ_TRIG_nRSTOUT	6:0	12
SEQ_TRIG_GPIO	6:0	13
BUCK1_SEQ_DLY	7:0	14
BUCK2_SEQ_DLY	7:0	15
BUCK3_SEQ_DLY	7:0	16
LDO_SEQ_DLY	7:0	17
nRSTOUT_SEQ_DLY	7:0	18
GPIO_SEQ_DLY	7:0	19
INT_MASK_BUCKx_LDO	7:0	20
VMON_BUCK1_CFG	3:0	21
VMON_BUCK2_CFG	3:0	22
VMON_BUCK3_CFG	3:0	23
VMON_LDO_CFG	3:0	24
ERR_BUCKx_LDO_CFG	7:0	25
INT_MASK_SAFETY	1:0	26
PIN_MON_ERR_CFG	1:0	27

Irrelevant bits are padded with zeros.

7.4.1.15 CRC on Device NVM Contents

The device NVM registers are protected by CRC. The expected checksum value is stored in the device NVM. The CRC controller in this device performs a CRC to verify the integrity of the NVM registers. The CRC controller calculates checksum value of the device that represents the actual content of the NVM registers, and then compares this checksum value against the stored checksum value in the device NVM.

The CRC controller detects a checksum error when the internally calculated checksum value of the device is not equal to the checksum-value stored in the device NVM. If the CRC controller detects a checksum error, the devices sets the NVM_CRC_ERR_STATUS bit and goes into the RESET State, which also forces the nRSTOUT and nINT pins to be pulled low, or WT_PWR_REC State.

The MCU can clear the bit by writing a '1' to the NVM_CRC_ERR_STATUS bit.

7.4.1.16 I²C Serial Interface

The interface adds flexibility to the power-supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and status bits to be monitored. Register contents remain intact as long as the VSYS voltage remains above the UVLO threshold. An internal oscillator runs the I²C interface and is automatically enabled after an access to the interface.

The 7-bit device address for the PMIC is 110 0000b.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

Note

Since the voltage source for the SDA and SCL pull-up resistors can come from either an external voltage source or from one of the PMIC voltage rails, it is recommended that a STOP command be sent to the PMIC before actual transactions are generated. This will ensure that if by chance a false start command was registered by the PMIC, that it be terminated before an actual command is issued. If supplied by an external source, the external source must be present on or before the application of VSYS in order to avoid a floating node on the SDA and SCL lines.

7.4.1.17 CRC on I²C Interface

The I²C-compatible synchronous serial interface provides access to the configurable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a controller or a target depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. The device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode plus (1 MHz) when VIO is 3.3 V or 1.8 V, and high-speed mode (3.4 MHz) only when VIO is 1.8 V.

7.4.1.17.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

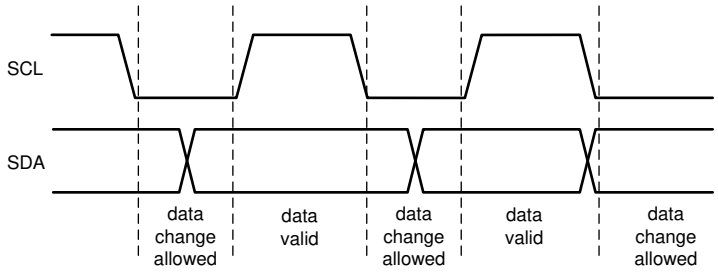


Figure 7-9. Data Validity Diagram

7.4.1.17.2 Start and Stop Conditions

The device is controlled through an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as the SDA signal going from HIGH to LOW while the SCL signal is HIGH. A STOP condition is defined as the SDA signal going from LOW to HIGH while the SCL signal is HIGH. The I²C controller device device always generates the START and STOP conditions.

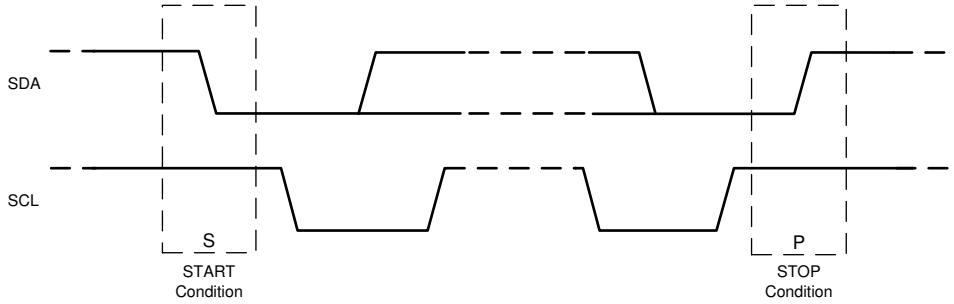


Figure 7-10. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. The I²C controller device can generate repeated START conditions during data transmission. A START and a repeated START condition are equivalent function-wise. Figure 7-11 shows the SDA and SCL signal timing for the I²C-compatible bus. For timing values, see the *Specification* section.

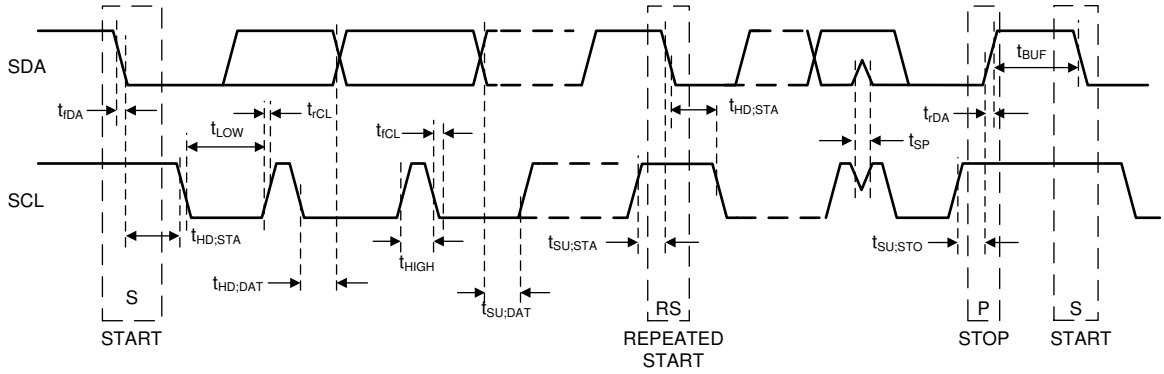


Figure 7-11. I²C-Compatible Timing

7.4.1.17.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the controller device. The controller device releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the controller device is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the target device. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the controller device), but the SDA line is not pulled down.

After the START condition, the bus controller device sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register. Figure 7-12 shows an example bit format of device address 110000-Bin = 60Hex.

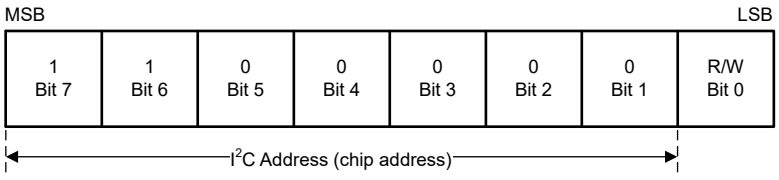


Figure 7-12. Example Device Address

In case the MCU attempts to write to a register-address that does not exist, the device sets the I2C_INVALID_ADDR_ACK bit and pulls the nINT pin low, unless the I2C_INVALID_ADDR_MASK bit is set. The MCU must clear this bit by writing a '1' to the I2C_INVALID_ADDR_ACK bit. In case the I2C_INVALID_ADDR_ACK bit is set, an address error still sets the I2C_INVALID_ADDR_ACK bit, but does not pull the nINT pin low and the part remains in its current state.

For safety applications, the device supports read and write protocols with embedded CRC data fields. In a write cycle, the I^2C controller device (i.e. the MCU) must provide the 8-bit CRC value after sending the write data bits and receiving the ACK from the target (i.e. the TPS650332-Q1 PMIC). The CRC value must be calculated from every bit included in the write protocol except the ACK bits from the target. See CRC Calculation for I2C and SPI Interface Protocols. In a read cycle, the I^2C target must provide the 8-bit CRC value after sending the read data bits and the ACK bit, and expect to receive the NACK from the controller at the end of the protocol. The CRC value must be calculated from every bit included in the read protocol except the ACK and NACK bits. See CRC Calculation for I2C and SPI Interface Protocols.

Note

If I2C CRC is enabled in the device and an I2C write without R_CRC bits is done, the device does not process the write request. The device does not set any interrupt bit and does not pull the nINT pin low.

The embedded CRC field can be enabled or disabled from the protocol by setting the I2C_CRC_EN register bit to '1' - enabled, '0' - disabled. The default of this bit is configurable through the NVM.

In case the calculated CRC-value does not match the received CRC-check-sum, an I^2C-CRC-error is detected, the I2C_CRC_ERR_ACK bit is set and pulls the nINT pin low, unless it is masked by the I2C_CRC_ERR_MASK bit. The MCU must clear this bit by writing a '1' to the I2C_CRC_ERR_ACK bit. In case the I2C_CRC_ERR_MASK bit is set, the I2C_CRC_ERR_ACK bit is still set, but does not pull down the nINT pin and the device remains in its current state.

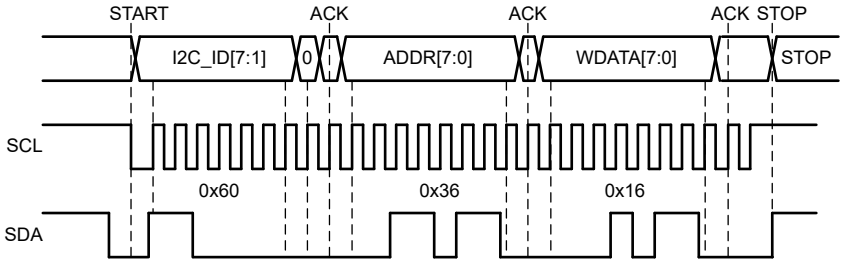
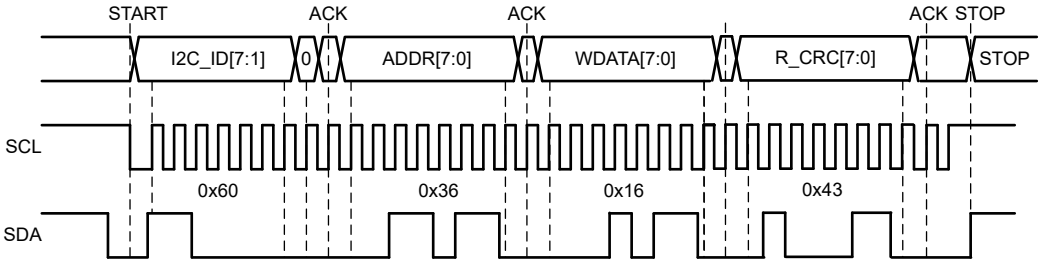
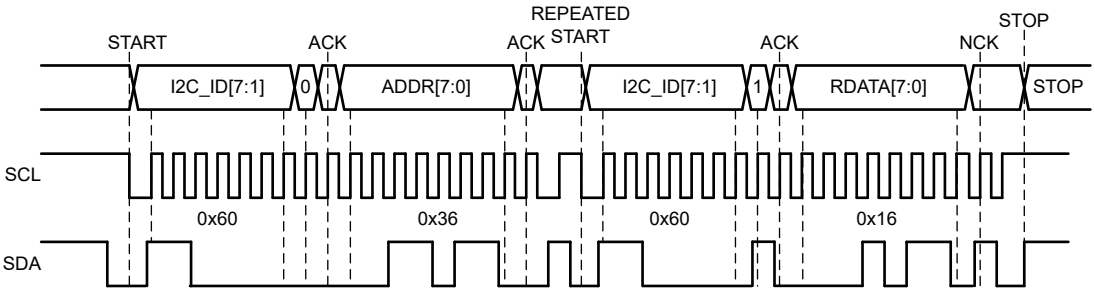


Figure 7-13. I^2C Write Cycle without CRC



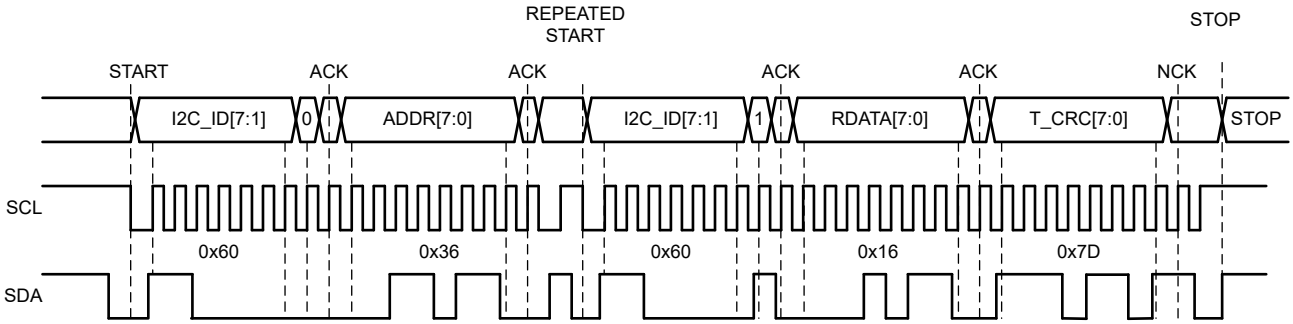
The I^2C controller device device (i.e. the MCU) provides R_CRC[7:0], which is calculated from the I2C_ID, R/W, ADDR, and the WDATA bits (24 bits). See CRC Calculation for I2C and SPI Interface Protocols.

Figure 7-14. I^2C Write Cycle with CRC



When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 7-15. I²C Read Cycle without CRC



The I²C target device (i.e. the TPS650332-Q1) provides T_CRC[7:0], which is calculated from the I2C_ID, R/W, ADDR, I2C_ID, R/W, and the RDATA bits (32 bits). See CRC Calculation for I2C and SPI Interface Protocols.

Figure 7-16. I²C READ Cycle with CRC

7.4.1.17.4 Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the device, the internal address index counter is incremented by one and the next register is written. Table 7-2 lists the writing sequence to two consecutive registers. Note that auto increment feature does not support CRC protocol.

Table 7-2. Auto-Increment Example

ACTION	START	DEVICE ADDRESS = 0x60	WRITE		REGISTER ADDRESS		DATA		DATA		STOP
PMIC device				ACK		ACK		ACK		ACK	

7.4.1.18 I²C CRC Calculations

7.4.1.18.1 CRC Calculation for the I²C Protocol

For safety applications, the TPS650332-Q1device supports read and write protocols with embedded CRC data fields. Both the master and slave devices use a standard CRC-8 polynomial to calculate the checksum value: $X^8 + X^2 + X + 1$.The CRC algorithm details are as follows:

- Initial value for the remainder is all 1s.
- Big-endian bit stream order
- Result inversion is enabled.

The TPS650332-Q1 device uses this polynomial to calculate the checksum value on every bit except the ACK and NACK bits it receives from the MCU during a write protocol. The device compares this calculated checksum with the MCRC checksum value which the device receives from the MCU. The device also uses this polynomial to calculate the SCRC checksum value based on every bit except the ACK and NACK bits which the device transmits to the MCU during a read protocol. The master device (MCU) must use this same polynomial to calculate the checksum value based on the bits which the MCU receives from the device. The MCU must compare this calculated checksum with the SCRC checksum value which it receives from the device.

Figure 7-17 and Figure 7-18 show the calculation of a 4-bit MCRC and the SCRC (respectively).

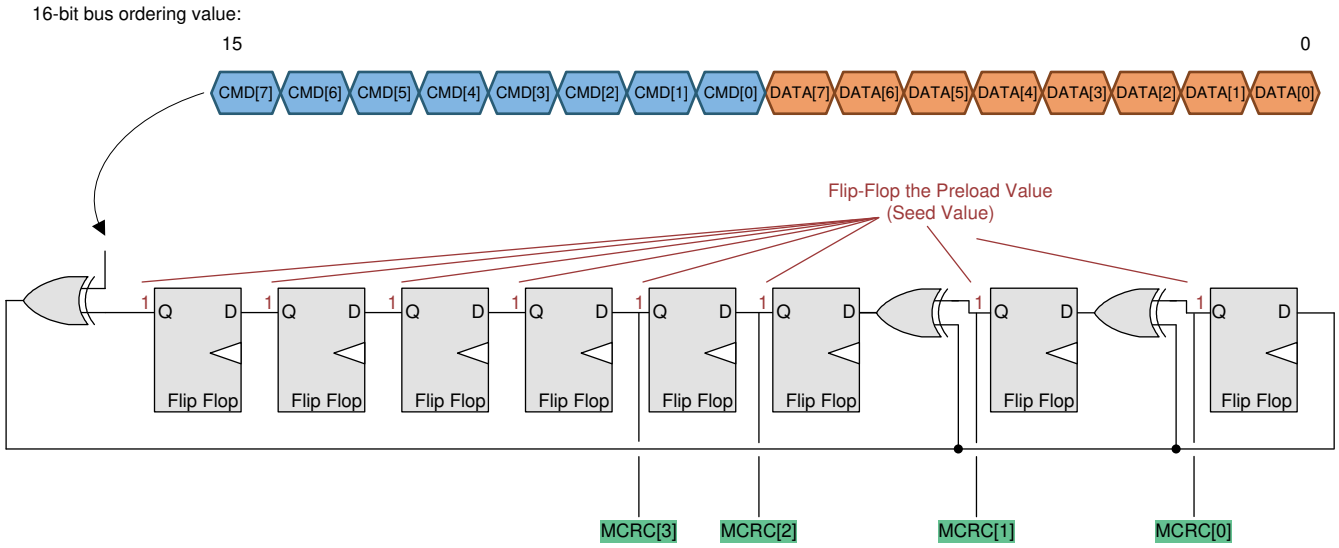


Figure 7-17. Calculation of 4-Bit Master CRC (MCRC) Output

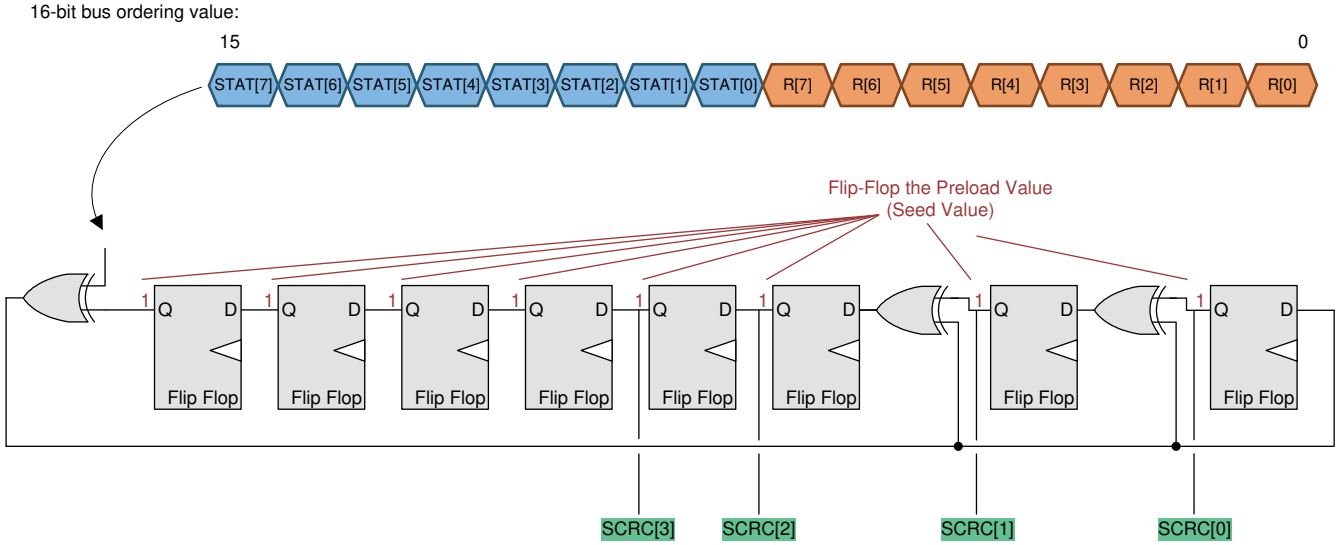


Figure 7-18. Calculation of 4-Bit Slave CRC (SCRC) Input

7.5 Device Functional Modes

Consult the Technical Reference Manual (TRM) for the specific part number to see the device configuration and Power Sequence Diagram.

7.5.1 Power-Up Sequence

The power-up sequence is controlled by the configuration of the Sequence Trigger registers and the Sequence Delay registers.

7.5.2 Power-Down Sequence

To ensure that all rails discharge, the device waits until the outputs discharge below 0.3 V before a new power-up sequence can be initiated.

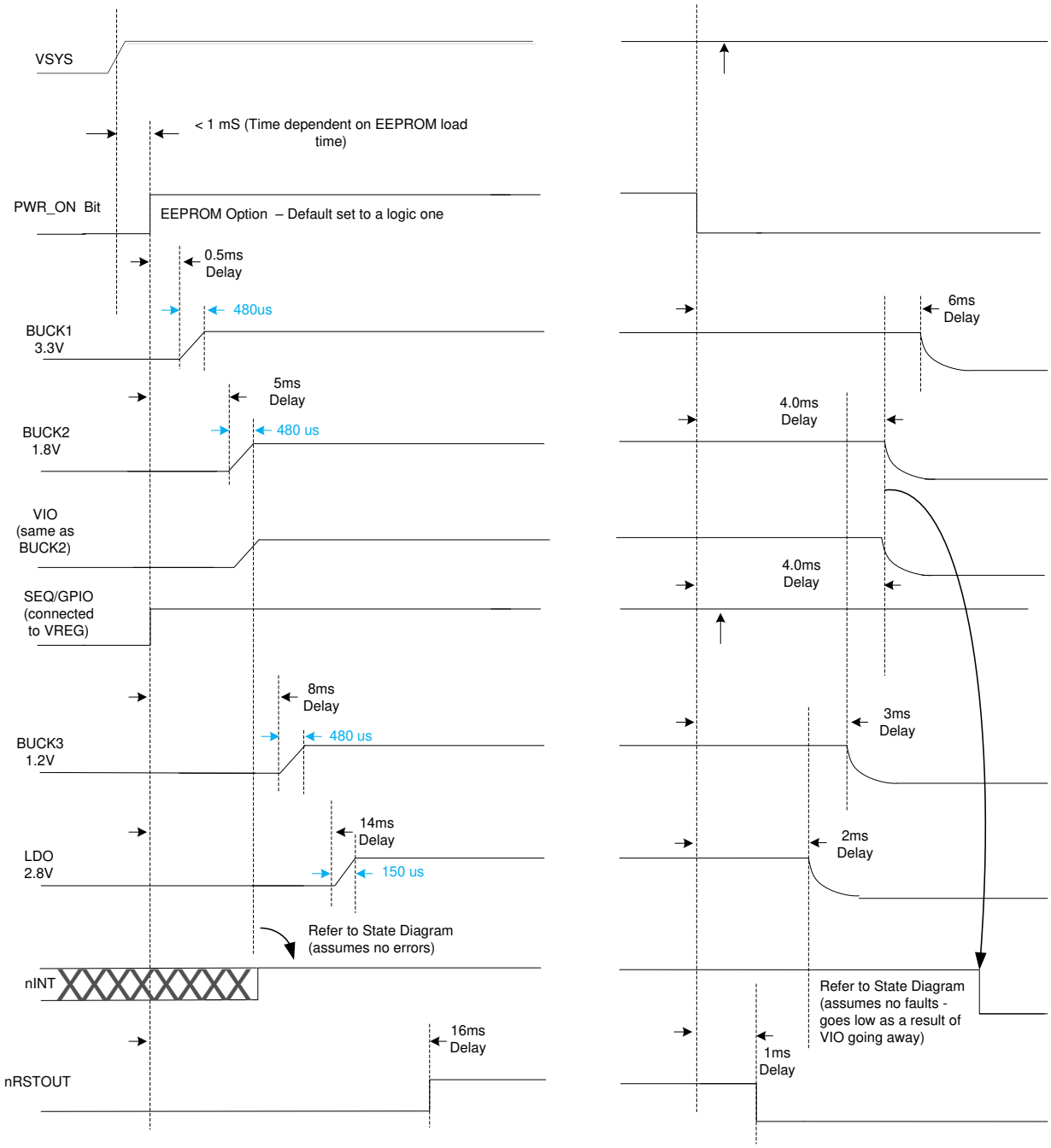
7.5.3 Power Sequence Diagram

The Power Sequence Diagram shown below is for the default setting of the device populated on the TI EVM. This default setting matches the settings shown in the Register Map section of this document. Consult the Technical Reference Manual (TRM) for a particular part number to see the specific settings and Power Sequence Diagram for that particular part number.

Note

The times shown in the timing diagrams reflect the time programmed in the xxx_SEQ_DLY registers. The programmed times have a ±10% tolerance. When measured in the application, the Start Time (t_{START}) for the BUCKs and the LDO are added to the programmed sequence delay times. The time it takes to run ABIST also adds to the measured sequence delay times. Running ABIST takes approximately 100us to 300us per voltage rail.

Automatic Power Up Sequence/PWR_ON Bit Power Down Sequence



NOTE: Power Up sequence is based on SEQ and/or GPIO

NOTE: Power Down sequence is the reverse order of the Power Up sequence.

Figure 7-19. Power Sequence

7.6 Register Map

7.6.1 User Registers

Note

The Reset value that is shown for one or more register bits in the Register Map does not necessarily reflect the value programmed at the factory. Consult the TRM (Technical Reference Manual) for the specific device part number to see the actual default settings programmed at the factory.

7.6.1.1 TPS650332_Map Registers

Table 7-3 lists the memory-mapped registers for the TPS650332_Map registers. All register offset addresses not listed in Table 7-3 should be considered as reserved locations and the register contents should not be modified.

Table 7-3. TPS650332_MAP Registers

Address	Acronym	Register Name	Section
0h	PID	Product ID	Go
1h	RID	Revision ID	Go
2h	CONTROL_LOCK	Control Lock/Unlock Command Register	Go
3h	BUCK_LDO_CTRL	Enable Register	Go
4h	GPIO_CTRL	GPIO Settings	Go
5h	CONFIG_LOCK	Configuration Lock/Unlock Command Register	Go
6h	LDO_GPIO_CFG	LDO Control Register	Go
7h	BUCK1_VOUT	BUCK1 Output Voltage Settings	Go
8h	BUCK1_UVLO	BUCK1 Input Voltage UVLO	Go
9h	BUCK2_VOUT	BUCK2 Output Voltage Settings	Go
Ah	BUCK3_VOUT	BUCK3 Output Voltage Settings	Go
Bh	LDO_VOUT	LDO Output Voltage Settings	Go
Ch	DISCHARGE_SETTING	Discharge Setting Control Register	Go
Dh	SEQ_TRIG_BUCK1	BUCK1 Sequencer Assignments	Go
Eh	SEQ_TRIG_BUCK2	BUCK2 Sequencer Assignments	Go
Fh	SEQ_TRIG_BUCK3	BUCK3 Sequencer Assignments	Go
10h	SEQ_TRIG_LDO	LDO Sequencer Assignments	Go
11h	SEQ_TRIG_nRSTOUT	BUCK1 and BUCK2 Sequencer Assignments	Go
12h	SEQ_TRIG_GPIO	BUCK1 and BUCK2 Sequencer Assignments	Go
13h	BUCK1_SEQ_DLY	BUCK1 Sequence Delay	Go
14h	BUCK2_SEQ_DLY	BUCK2 Sequence Delay	Go
15h	BUCK3_SEQ_DLY	BUCK3 Sequence Delay	Go
16h	LDO_SEQ_DLY	LDO Sequence Delay	Go
17h	nRSTOUT_SEQ_DLY	nRSTOUT Sequence Delay	Go
18h	GPIO_SEQ_DLY	GPIO Sequence Delay	Go
19h	INT_ACK	Interrupt Acknowledge Global Register	Go
1Ah	INT_ACK_BUCK1	Interrupt Acknowledge BUCK1 Register	Go
1Bh	INT_ACK_BUCK2	Interrupt Acknowledge BUCK2 Register	Go
1Ch	INT_ACK_BUCK3	Interrupt Acknowledge BUCK3 Register	Go
1Dh	INT_ACK_LDO	Interrupt Acknowledge LDO Register	Go
1Eh	INT_MASK_BUCKx_LDO	BUCK1 Mask Register to Enable or Disable Interrupt Sources	Go
1Fh	FAULT_STATUS_BUCK1	BUCK1 Fault Status Register	Go
20h	FAULT_STATUS_BUCK2	BUCK2 Fault Status Register	Go
21h	FAULT_STATUS_BUCK3	BUCK3 Fault Status Register	Go
22h	FAULT_STATUS_LDO	LDO Fault Status Register	Go
23h	VMON_BUCK1_CFG	BUCK1 Voltage Monitor Configuration Register	Go
24h	VMON_BUCK2_CFG	BUCK2 Voltage Monitor Configuration Register	Go
25h	VMON_BUCK3_CFG	BUCK3 Voltage Monitor Configuration Register	Go

Table 7-3. TPS650332_MAP Registers (continued)

Address	Acronym	Register Name	Section
26h	VMON_LDO_CFG	LDO Voltage Monitor Configuration Register	Go
27h	ERR_BUCKx_LDO_CFG	BUCK1 Mask Register to Enable or Disable Interrupt Sources	Go
28h	RESTART_CMD	Re-Start Command Register	Go
29h	CFG_REG_CRC	Configuration Register for CRC	Go
2Ah	DEV_STAT	Device Status Register 1	Go
2Bh	DEV_ERR_ACK_1	Device Error Acknowledge_ 1 Register	Go
2Ch	DEV_ERR_ACK_2	System Error Acknowledge Register	Go
2Dh	DEV_FAULT_STATUS_1	Internal Supply Acknowledge Register	Go
2Eh	DEV_FAULT_STATUS_2	Internal Supply Acknowledge Register	Go
2Fh	INT_MASK_SAFETY	Interrupt Mask Safety	Go
30h	PIN_MON_ERR_CFG	BUCK1 Mask Register to Enable or Disable Interrupt Sources	Go
31h	ABIST_GROUP_DONE	ABIST Status Register	Go
32h	ABIST_BUCK1_2_ACK	ABIST BUCK1 and BUCK2 Error Acknowledge Register	Go
33h	ABIST_LDO_BUCK3_ACK	ABIST BUCK3 and LDO Error Acknowledge Register	Go
34h	ABIST_SYSTEM_ACK	ABIST System Error Acknowledge Register	Go
35h	ABIST_RUN_CMD	EEPROM Program Command Register	Go
36h	POWER_GOOD_STATUS	Voltage Regulator Power Good Status	Go
4Ah	EEPROM_PROG_CMD	EEPROM Program Command Register	Go

Complex bit access types are encoded to fit into small table cells. Table 7-4 shows the codes that are used for access types in this section.

Table 7-4. TPS650332_Map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WSelfClrF	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1.1 PID Register (Address = 0h) [Reset = D0h]

Return to the Summary Table.

Initialization source: POR

Figure 7-20. PID Register

7	6	5	4	3	2	1	0
PID							
R-D0h							

Table 7-5. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PID	R	D0h	Product ID: TPS65033200 (0xD0)

7.6.1.1.2 RID Register (Address = 1h) [Reset = 09h]

Return to the Summary Table.

Initialization source: POR

Figure 7-21. RID Register

7	6	5	4	3	2	1	0
NVM_Version				Die_Revision			
R/W-0h				R-9h			

Table 7-6. RID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	NVM_Version	R/W	0h	NVM Revision 0h = A 1h = B 2h = C 3h = D
3-0	Die_Revision	R	9h	Die Revision (PG X.Y where X = major revision and Y = minor revision) 4h = PG 1.0 5h = PG 1.1 8h = PG 2.0 9h = PG 2.1

7.6.1.1.3 CONTROL_LOCK Register (Address = 2h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-22. CONTROL_LOCK Register

7	6	5	4	3	2	1	0
CONTROL_ACCESS_CMD							
R-0h							

Table 7-7. CONTROL_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONTROL_ACCESS_CMD	R	0h	Write to this register to either lock or unlock the control registers. A readback of this register results in '0x00'. 0h = Locks the Control Registers DDh = Unlocks the Control Registers

7.6.1.1.4 BUCK_LDO_CTRL Register (Address = 3h) [Reset = 1Fh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access: CTRL_LOCK

Figure 7-23. BUCK_LDO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			ENABLE_SPREAD_SPECTRUM	ENABLE_BUCK3	ENABLE_BUCK2	ENABLE_BUCK1	ENABLE_LDO
R-0h			R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 7-8. BUCK_LDO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	ENABLE_SPREAD_SPECTRUM	R/W	1h	Spread Spectrum Enable 0h = Disabled 1h = Enabled
3	ENABLE_BUCK3	R/W	1h	BUCK3 enable bit 0h = Disabled 1h = Enabled
2	ENABLE_BUCK2	R/W	1h	BUCK2 enable bit 0h = Disabled 1h = Enabled
1	ENABLE_BUCK1	R/W	1h	BUCK1 enable bit 0h = Disabled 1h = Enabled
0	ENABLE_LDO	R/W	1h	LDO enable bit 0h = Disabled 1h = Enabled

7.6.1.1.5 GPIO_CTRL Register (Address = 4h) [Reset = 1Fh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access: CTRL_LOCK

Figure 7-24. GPIO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			LDO_PREBIAS_CTRL	WARM_THR_STARTUP_CTRL	CONFIG_CRC_EN	PWR_ON	GPIO_STATE
R-0h			R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 7-9. GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	LDO_PREBIAS_CTRL	R/W	1h	LDO Pre Bias Control 0h = Allows the device to power up even if the voltage on the LDO output is above the Short Circuit to Ground threshold. All other outputs must still be below the Short Circuit to Ground threshold. 1h = The device remains in the RESET state until the voltage on all outputs are below the Short Circuit to Ground threshold.
3	WARM_THR_STARTUP_CTRL	R/W	1h	WARM_THR_STARTUP_CTRL 0h = Device powers up if temperature is above the Warm Threshold setting but below the Over Temperature setting 1h = Device does not power up until the temperature is below the Warm Threshold setting
2	CONFIG_CRC_EN	R/W	1h	Config CRC Enable 0h = Disabled 1h = Enabled
1	PWR_ON	R/W	1h	Power up/down control 0h = Device powers off 1h = Device powers on
0	GPIO_STATE	R/W	1h	If configured as an output, this bit enables the GPIO function and also controls the state of the GPIO pin. 0h = The GPIO function is disabled. The output state is 'low'. 1h = The GPIO function is enabled. The output state is 'high'.

7.6.1.1.6 CONFIG_LOCK Register (Address = 5h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-25. CONFIG_LOCK Register

7	6	5	4	3	2	1	0
CONFIG_ACCESS_CMD							
R-0h							

Table 7-10. CONFIG_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONFIG_ACCESS_CMD	R	0h	Write to this register to either lock or unlock the configuration registers. A readback of this register results in '0x00'. 0h = Locks the Configuration Registers AAh = Unlocks the Configuration Registers

7.6.1.1.7 LDO_GPIO_CFG Register (Address = 6h) [Reset = 1Dh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access: CFG_LOCK
CFG_CRC : YES

Figure 7-26. LDO_GPIO_CFG Register

7	6	5	4	3	2	1	0
RESERVED	STATE_TRANSITION	TWARN_LEVEL	nRSTOUT_PIN_CONFIG	nINT_PIN_CONFIG	GPIO_DIR_CONFIG	LDO_BYP_EN	LDO_IOUT
R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-1h

Table 7-11. LDO_GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	STATE_TRANSITION	R/W	0h	State Transition for Priority 2 Faults 0h = Priority 2 Faults transition to the RESET state 1h = Priority 2 Faults transition to the WAIT_PWR_CYCLE state
5	TWARN_LEVEL	R/W	0h	Die Temperature Warning Level 0h = Temperature Warning Level is set to 120 deg C 1h = Temperature Warning Level is set to 130 deg C
4	nRSTOUT_PIN_CONFIG	R/W	1h	nRSTOUT PIN Configuration 0h = Open-Drain 1h = Push-Pull
3	nINT_PIN_CONFIG	R/W	1h	nINT PIN Configuration 0h = Open-Drain 1h = Push-Pull
2	GPIO_DIR_CONFIG	R/W	1h	GPIO Pin Configuration 0h = Configured as an output 1h = Configured as an input
1	LDO_BYP_EN	R/W	0h	LDO bypass enable bit: 0h = LDO operation 1h = Bypass Mode operation (Load Switch Operation)
0	LDO_IOUT	R/W	1h	LDO Current Limit: 0h = 200mA 1h = 400mA

7.6.1.1.8 BUCK1_VOUT Register (Address = 7h) [Reset = 10h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-27. BUCK1_VOUT Register

7	6	5	4	3	2	1	0
RESERVED			BUCK1_VOUT				
R-0h			R/W-10h				

Table 7-12. BUCK1_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	BUCK1_VOUT	R/W	10h	The output voltage range is from 2.5V to 4.0V in increments of 50mV: 0h = 2.50V 1h = 2.55V 2h = 2.60V 3h = 2.65V 4h = 2.70V 5h = 2.75V 6h = 2.80V 7h = 2.85V 8h = 2.90V 9h = 2.95V Ah = 3.00V Bh = 3.05V Ch = 3.10V Dh = 3.15V Eh = 3.20V Fh = 3.25V 10h = 3.30V 11h = 3.35V 12h = 3.40V 13h = 3.45V 14h = 3.50V 15h = 3.55V 16h = 3.60V 17h = 3.65V 18h = 3.70V 19h = 3.75V 1Ah = 3.80V 1Bh = 3.85V 1Ch = 3.90V 1Dh = 3.95V 1Eh = 4.00V 1Fh = 4.00V

7.6.1.1.9 BUCK1_UVLO Register (Address = 8h) [Reset = 12h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-28. BUCK1_UVLO Register

7	6	5	4	3	2	1	0
BUCK1_UVLO_Falling				BUCK1_UVLO_Rising			
R/W-1h				R/W-2h			

Table 7-13. BUCK1_UVLO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK1_UVLO_Falling	R/W	1h	The PVIN_B1 pin UVLO falling voltage setting is programmable based on the input voltage requirement (the values shown have a +/-10% tolerance): 0h = 3.5V 1h = 4.0V 2h = 4.5V 3h = 5.0V 4h = 5.5V 5h = 6.0V 6h = 6.5V 7h = 7.0V 8h = 7.5V 9h = 8.0V Ah = 8.5V Bh = 9.0V Ch = 9.0V Dh = 9.0V Eh = 9.0V Fh = 9.0V
3-0	BUCK1_UVLO_Rising	R/W	2h	The PVIN_B1 pin UVLO rising voltage setting is programmable based on the input voltage requirement (the values shown have a +/-10% tolerance): 0h = 3.64V 1h = 4.16V 2h = 4.68V 3h = 5.20V 4h = 5.72V 5h = 6.24V 6h = 6.76V 7h = 7.28V 8h = 7.80V 9h = 8.32V Ah = 8.84V Bh = 9.36V Ch = 9.36V Dh = 9.36V Eh = 9.36V Fh = 9.36V

7.6.1.1.10 BUCK2_VOUT Register (Address = 9h) [Reset = 1Dh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-29. BUCK2_VOUT Register

7	6	5	4	3	2	1	0
RESERVED			BUCK2_VOUT				
R-0h			R/W-1Dh				

Table 7-14. BUCK2_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	BUCK2_VOUT	R/W	1Dh	The output voltage range is from 0.9V to 1.9V: 0h = 0.9V 1h = 0.95V 2h = 1.000V 3h = 1.025V 4h = 1.050V 5h = 1.075V 6h = 1.100V 7h = 1.125V 8h = 1.150V 9h = 1.175V Ah = 1.200V Bh = 1.225V Ch = 1.250V Dh = 1.275V Eh = 1.300V Fh = 1.325V 10h = 1.350V 11h = 1.375V 12h = 1.400V 13h = 1.425V 14h = 1.450V 15h = 1.475V 16h = 1.500V 17h = 1.525V 18h = 1.550V 19h = 1.575V 1Ah = 1.600V 1Bh = 1.700V 1Ch = 1.750V 1Dh = 1.800V 1Eh = 1.850V 1Fh = 1.900V

7.6.1.1.11 BUCK3_VOUT Register (Address = Ah) [Reset = 0Ah]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-30. BUCK3_VOUT Register

7	6	5	4	3	2	1	0
RESERVED			BUCK3_VOUT				
R-0h			R/W-Ah				

Table 7-15. BUCK3_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	BUCK3_VOUT	R/W	Ah	The output voltage range is from 0.9V to 1.9V : 0h = 0.9V 1h = 0.95V 2h = 1.000V 3h = 1.025V 4h = 1.050V 5h = 1.075V 6h = 1.100V 7h = 1.125V 8h = 1.150V 9h = 1.175V Ah = 1.200V Bh = 1.225V Ch = 1.250V Dh = 1.275V Eh = 1.300V Fh = 1.325V 10h = 1.350V 11h = 1.375V 12h = 1.400V 13h = 1.425V 14h = 1.450V 15h = 1.475V 16h = 1.500V 17h = 1.525V 18h = 1.550V 19h = 1.575V 1Ah = 1.600V 1Bh = 1.700V 1Ch = 1.750V 1Dh = 1.800V 1Eh = 1.850V 1Fh = 1.900V

7.6.1.1.12 LDO_VOUT Register (Address = Bh) [Reset = 0Eh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-31. LDO_VOUT Register

7	6	5	4	3	2	1	0
RESERVED			LDO_VOUT				
R-0h			R/W-Eh				

Table 7-16. LDO_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	LDO_VOUT	R/W	Eh	The output voltage range is from 1.8V to 3.3V: 0h = 1.800V 1h = 1.825V 2h = 2.500V 3h = 2.525V 4h = 2.550V 5h = 2.575V 6h = 2.600V 7h = 2.625V 8h = 2.650V 9h = 2.675V Ah = 2.700V Bh = 2.725V Ch = 2.750V Dh = 2.775V Eh = 2.800V Fh = 2.825V 10h = 2.850V 11h = 2.875V 12h = 2.900V 13h = 2.925V 14h = 2.950V 15h = 2.975V 16h = 3.000V 17h = 3.025V 18h = 3.050V 19h = 3.075V 1Ah = 3.100V 1Bh = 3.125V 1Ch = 3.150V 1Dh = 3.175V 1Eh = 3.200V 1Fh = 3.300V

7.6.1.1.13 DISCHARGE_SETTING Register (Address = Ch) [Reset = 55h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-32. DISCHARGE_SETTING Register

7	6	5	4	3	2	1	0
BUCK3_Discharge_Control		BUCK2_Discharge_Control		BUCK1_Discharge_Control		LDO_Discharge_Control	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	

Table 7-17. DISCHARGE_SETTING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BUCK3_Discharge_Control	R/W	1h	BUCK3 Discharge Control 0h = No Discharge 1h = 125 Ω 2h = 250 Ω 3h = 500 Ω
5-4	BUCK2_Discharge_Control	R/W	1h	BUCK2 Discharge Control 0h = No Discharge 1h = 125 Ω 2h = 250 Ω 3h = 500 Ω
3-2	BUCK1_Discharge_Control	R/W	1h	BUCK1 Discharge Control 0h = No Discharge 1h = 125 Ω 2h = 250 Ω 3h = 500 Ω
1-0	LDO_Discharge_Control	R/W	1h	LDO Discharge Control 0h = 50K Ω 1h = 125 Ω 2h = 250 Ω 3h = 500 Ω

7.6.1.1.14 SEQ_TRIG_BUCK1 Register (Address = Dh) [Reset = 1Eh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-33. SEQ_TRIG_BUCK1 Register

7	6	5	4	3	2	1	0
RESERVED		PWR_ON_bit_BUCK1	LDO_PG_BUCK1	BUCK3_PG_BUCK1	BUCK2_PG_BUCK1	GPIO_PIN_BUCK1	SEQ_PIN_BUCK1
R-0h		R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h

Table 7-18. SEQ_TRIG_BUCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	PWR_ON_bit_BUCK1	R/W	0h	BUCK1 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
4	LDO_PG_BUCK1	R/W	1h	BUCK1 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
3	BUCK3_PG_BUCK1	R/W	1h	BUCK1 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
2	BUCK2_PG_BUCK1	R/W	1h	BUCK1 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
1	GPIO_PIN_BUCK1	R/W	1h	BUCK1 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
0	SEQ_PIN_BUCK1	R/W	0h	BUCK1 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic

7.6.1.1.15 SEQ_TRIG_BUCK2 Register (Address = Eh) [Reset = 1Eh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-34. SEQ_TRIG_BUCK2 Register

7	6	5	4	3	2	1	0
RESERVED		PWR_ON_bit_BUCK2	LDO_PG_BUCK2	BUCK3_PG_BUCK2	BUCK1_PG_BUCK2	GPIO_PIN_BUCK2	SEQ_PIN_BUCK2
R-0h		R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h

Table 7-19. SEQ_TRIG_BUCK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	PWR_ON_bit_BUCK2	R/W	0h	BUCK2 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
4	LDO_PG_BUCK2	R/W	1h	BUCK2 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
3	BUCK3_PG_BUCK2	R/W	1h	BUCK2 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
2	BUCK1_PG_BUCK2	R/W	1h	BUCK2 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
1	GPIO_PIN_BUCK2	R/W	1h	BUCK2 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
0	SEQ_PIN_BUCK2	R/W	0h	BUCK2 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic

7.6.1.1.16 SEQ_TRIG_BUCK3 Register (Address = Fh) [Reset = 1Ch]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-35. SEQ_TRIG_BUCK3 Register

7	6	5	4	3	2	1	0
RESERVED		PWR_ON_bit_BUCK3	LDO_PG_BUCK3	BUCK2_PG_BUCK3	BUCK1_PG_BUCK3	GPIO_PIN_BUCK3	SEQ_PIN_BUCK3
R-0h		R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

Table 7-20. SEQ_TRIG_BUCK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	PWR_ON_bit_BUCK3	R/W	0h	BUCK3 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
4	LDO_PG_BUCK3	R/W	1h	BUCK3 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
3	BUCK2_PG_BUCK3	R/W	1h	BUCK3 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
2	BUCK1_PG_BUCK3	R/W	1h	BUCK3 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
1	GPIO_PIN_BUCK3	R/W	0h	BUCK3 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
0	SEQ_PIN_BUCK3	R/W	0h	BUCK3 Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic

7.6.1.1.17 SEQ_TRIG_LDO Register (Address = 10h) [Reset = 1Ch]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-36. SEQ_TRIG_LDO Register

7	6	5	4	3	2	1	0
RESERVED		PWR_ON_bit_LDO	BUCK3_PG_LDO	BUCK2_PG_LDO	BUCK1_PG_LDO	GPIO_PIN_LDO	SEQ_PIN_LDO
R-0h		R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

Table 7-21. SEQ_TRIG_LDO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	PWR_ON_bit_LDO	R/W	0h	LDO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
4	BUCK3_PG_LDO	R/W	1h	LDO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
3	BUCK2_PG_LDO	R/W	1h	LDO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
2	BUCK1_PG_LDO	R/W	1h	LDO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
1	GPIO_PIN_LDO	R/W	0h	LDO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
0	SEQ_PIN_LDO	R/W	0h	LDO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic

7.6.1.1.18 SEQ_TRIG_nRSTOUT Register (Address = 11h) [Reset = 3Eh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-37. SEQ_TRIG_nRSTOUT Register

7	6	5	4	3	2	1	0
RESERVED	PWR_ON_bit_nRSTOUT	LDO_PG_nRSTOUT	BUCK3_PG_nRSTOUT	BUCK2_PG_nRSTOUT	BUCK1_PG_nRSTOUT	GPIO_PIN_nRSTOUT	SEQ_PIN_nRSTOUT
R-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h

Table 7-22. SEQ_TRIG_nRSTOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PWR_ON_bit_nRSTOUT	R/W	0h	nRSTOUT Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
5	LDO_PG_nRSTOUT	R/W	1h	Included as part of the power ON/OFF sequence logic 0h = Is part of power ON/OFF sequence 1h = Not included as part of the power ON/OFF sequence logic
4	BUCK3_PG_nRSTOUT	R/W	1h	nRSTOUT Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
3	BUCK2_PG_nRSTOUT	R/W	1h	nRSTOUT Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
2	BUCK1_PG_nRSTOUT	R/W	1h	nRSTOUT Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
1	GPIO_PIN_ nRSTOUT	R/W	1h	nRSTOUT Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
0	SEQ_PIN_ nRSTOUT	R/W	0h	nRSTOUT Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic

7.6.1.1.19 SEQ_TRIG_GPIO Register (Address = 12h) [Reset = 7Fh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-38. SEQ_TRIG_GPIO Register

7	6	5	4	3	2	1	0
RESERVED	PWR_ON_bit_GPIO	LDO_PG_GPIO	BUCK3_PG_GPIO	BUCK2_PG_GPIO	BUCK1_PG_GPIO	nRSTOUT_PIN_GPIO	SEQ_PIN_GPIO
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 7-23. SEQ_TRIG_GPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PWR_ON_bit_GPIO	R/W	1h	GPIO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
5	LDO_PG_GPIO	R/W	1h	GPIO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
4	BUCK3_PG_GPIO	R/W	1h	GPIO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
3	BUCK2_PG_GPIO	R/W	1h	GPIO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
2	BUCK1_PG_GPIO	R/W	1h	GPIO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
1	nRSTOUT_PIN_GPIO	R/W	1h	GPIO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic
0	SEQ_PIN_ GPIO	R/W	1h	GPIO Sequence Trigger On/Off 0h = Included as part of the power ON/OFF sequence logic 1h = Not included as part of the power ON/OFF sequence logic

7.6.1.1.20 BUCK1_SEQ_DLY Register (Address = 13h) [Reset = 71h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-39. BUCK1_SEQ_DLY Register

7	6	5	4	3	2	1	0
BUCK1_SEQ_DLY_OFF				BUCK1_SEQ_DLY_ON			
R/W-7h				R/W-1h			

Table 7-24. BUCK1_SEQ_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK1_SEQ_DLY_OFF	R/W	7h	BUCK1 Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms
3-0	BUCK1_SEQ_DLY_ON	R/W	1h	BUCK1 Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms

7.6.1.1.21 BUCK2_SEQ_DLY Register (Address = 14h) [Reset = 56h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-40. BUCK2_SEQ_DLY Register

7	6	5	4	3	2	1	0
BUCK2_SEQ_DLY_OFF				BUCK2_SEQ_DLY_ON			
R/W-5h				R/W-6h			

Table 7-25. BUCK2_SEQ_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK2_SEQ_DLY_OFF	R/W	5h	BUCK2 Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms
3-0	BUCK2_SEQ_DLY_ON	R/W	6h	BUCK2 Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms

7.6.1.1.22 BUCK3_SEQ_DLY Register (Address = 15h) [Reset = 49h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-41. BUCK3_SEQ_DLY Register

7	6	5	4	3	2	1	0
BUCK3_SEQ_DLY_OFF				BUCK3_SEQ_DLY_ON			
R/W-4h				R/W-9h			

Table 7-26. BUCK3_SEQ_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK3_SEQ_DLY_OFF	R/W	4h	BUCK3 Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms
3-0	BUCK3_SEQ_DLY_ON	R/W	9h	BUCK3 Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms

7.6.1.1.23 LDO_SEQ_DLY Register (Address = 16h) [Reset = 3Dh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-42. LDO_SEQ_DLY Register

7	6	5	4	3	2	1	0
LDO_SEQ_DLY_OFF				LDO_SEQ_DLY_ON			
R/W-3h				R/W-Dh			

Table 7-27. LDO_SEQ_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LDO_SEQ_DLY_OFF	R/W	3h	LDO Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms
3-0	LDO_SEQ_DLY_ON	R/W	Dh	LDO Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms

7.6.1.1.24 nRSTOUT_SEQ_DLY Register (Address = 17h) [Reset = 2Eh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-43. nRSTOUT_SEQ_DLY Register

7	6	5	4	3	2	1	0
nRSTOUT_SEQ_DLY_OFF				nRSTOUT_SEQ_DLY_ON			
R/W-2h				R/W-Eh			

Table 7-28. nRSTOUT_SEQ_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	nRSTOUT_SEQ_DLY_OFF	R/W	2h	nRSTOUT Power Down Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms
3-0	nRSTOUT_SEQ_DLY_ON	R/W	Eh	nRSTOUT Power Up Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms

7.6.1.1.25 GPIO_SEQ_DLY Register (Address = 18h) [Reset = BBh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-44. GPIO_SEQ_DLY Register

7	6	5	4	3	2	1	0
GPIO_SEQ_DLY_OFF				GPIO_SEQ_DLY_ON			
R/W-Bh				R/W-Bh			

Table 7-29. GPIO_SEQ_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO_SEQ_DLY_OFF	R/W	Bh	GPIO Power Down Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms
3-0	GPIO_SEQ_DLY_ON	R/W	Bh	GPIO Power Up Sequence Delay From Trigger Point 0h = 0ms 1h = 0.5ms 2h = 1ms 3h = 2ms 4h = 3ms 5h = 4ms 6h = 5ms 7h = 6ms 8h = 7ms 9h = 8ms Ah = 9ms Bh = 10ms Ch = 12ms Dh = 14ms Eh = 16ms Fh = 20ms

7.6.1.1.26 INT_ACK Register (Address = 19h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR

Figure 7-45. INT_ACK Register

7	6	5	4	3	2	1	0
RESERVED				BUCK3_ACK	BUCK2_ACK	BUCK1_ACK	LDO_ACK
R-0h				R-0h	R-0h	R-0h	R-0h

Table 7-30. INT_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	BUCK3_ACK	R	0h	Interrupt Acknowledge BUCK3 Register 0h = No interrupt 1h = Interrupt set
2	BUCK2_ACK	R	0h	Interrupt Acknowledge BUCK2 Register 0h = No interrupt 1h = Interrupt set
1	BUCK1_ACK	R	0h	Interrupt Acknowledge BUCK1 0h = No interrupt 1h = Interrupt set
0	LDO_ACK	R	0h	Interrupt Acknowledge LDO 0h = No interrupt 1h = Interrupt set

7.6.1.1.27 INT_ACK_BUCK1 Register (Address = 1Ah) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-46. INT_ACK_BUCK1 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK1_OV_ACK	BUCK1_UV_ACK	BUCK1_OCP_ACK	BUCK1_WARM_ACK
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-31. INT_ACK_BUCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	BUCK1_OV_ACK	R/W1C	0h	BUCK1 Overvoltage Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
2	BUCK1_UV_ACK	R/W1C	0h	BUCK1 Undervoltage Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
1	BUCK1_OCP_ACK	R/W1C	0h	BUCK1 Overcurrent Protection Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
0	BUCK1_WARM_ACK	R/W1C	0h	BUCK1 Over Temperature Warning Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set

7.6.1.1.28 INT_ACK_BUCK2 Register (Address = 1Bh) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-47. INT_ACK_BUCK2 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK2_OV_ACK	BUCK2_UV_ACK	BUCK2_OCP_ACK	BUCK2_WARM_ACK
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-32. INT_ACK_BUCK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	BUCK2_OV_ACK	R/W1C	0h	BUCK2 Overvoltage Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
2	BUCK2_UV_ACK	R/W1C	0h	BUCK2 Undervoltage Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
1	BUCK2_OCP_ACK	R/W1C	0h	BUCK2 Overcurrent Protection Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
0	BUCK2_WARM_ACK	R/W1C	0h	BUCK2 Over Temperature Warning Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set

7.6.1.1.29 INT_ACK_BUCK3 Register (Address = 1Ch) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-48. INT_ACK_BUCK3 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK3_OV_ACK	BUCK3_UV_ACK	BUCK3_OCP_ACK	BUCK3_WARM_ACK
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-33. INT_ACK_BUCK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	BUCK3_OV_ACK	R/W1C	0h	BUCK3 Overvoltage Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
2	BUCK3_UV_ACK	R/W1C	0h	BUCK3 Undervoltage Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
1	BUCK3_OCP_ACK	R/W1C	0h	BUCK3 Overcurrent Protection Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
0	BUCK3_WARM_ACK	R/W1C	0h	BUCK3 Over Temperature Warning Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set

7.6.1.1.30 INT_ACK_LDO Register (Address = 1Dh) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-49. INT_ACK_LDO Register

7	6	5	4	3	2	1	0
RESERVED				LDO_OV_ACK	LDO_UV_ACK	LDO_OCP_ACK	LDO_WARM_ACK
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-34. INT_ACK_LDO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	LDO_OV_ACK	R/W1C	0h	LDO Overvoltage Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
2	LDO_UV_ACK	R/W1C	0h	LDO Undervoltage Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
1	LDO_OCP_ACK	R/W1C	0h	LDO Overcurrent Protection Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set
0	LDO_WARM_ACK	R/W1C	0h	LDO Over Temperature Warning Interrupt Acknowledge 0h = No interrupt 1h = Interrupt set

7.6.1.1.31 INT_MASK_BUCKx_LDO Register (Address = 1Eh) [Reset = FFh]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-50. INT_MASK_BUCKx_LDO Register

7	6	5	4	3	2	1	0
BUCK3_OCP_MASK	BUCK3_WARM_MASK	BUCK2_OCP_MASK	BUCK2_WARM_MASK	BUCK1_OCP_MASK	BUCK1_WARM_MASK	LDO_OCP_MASK	LDO_WARM_MASK
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 7-35. INT_MASK_BUCKx_LDO Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK3_OCP_MASK	R/W	1h	BUCK3 Overcurrent Protection Interrupt Mask 0h = Not Masked 1h = Masked
6	BUCK3_WARM_MASK	R/W	1h	BUCK3 Over Temperature Warning Interrupt Mask 0h = Not Masked 1h = Masked
5	BUCK2_OCP_MASK	R/W	1h	BUCK2 Overcurrent Protection Interrupt Mask 0h = Not Masked 1h = Masked
4	BUCK2_WARM_MASK	R/W	1h	BUCK2 Over Temperature Warning Interrupt Mask 0h = Not Masked 1h = Masked
3	BUCK1_OCP_MASK	R/W	1h	BUCK1 Overcurrent Protection Interrupt Mask 0h = Not Masked 1h = Masked
2	BUCK1_WARM_MASK	R/W	1h	BUCK1 Over Temperature Warning Interrupt Mask 0h = Not Masked 1h = Masked
1	LDO_OCP_MASK	R/W	1h	LDO Overcurrent Protection Interrupt Mask 0h = Not Masked 1h = Masked
0	LDO_WARM_MASK	R/W	1h	LDO Over Temperature Warning Interrupt Mask 0h = Not Masked 1h = Masked

7.6.1.1.32 FAULT_STATUS_BUCK1 Register (Address = 1Fh) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR

Figure 7-51. FAULT_STATUS_BUCK1 Register

7	6	5	4	3	2	1	0
RESERVED	PVIN_UVLO_STATUS	BUCK1_OV_STATUS	BUCK1_HOT_STATUS	BUCK1_OVP_STATUS	BUCK1_SCG_STATUS	BUCK1_OVL_STATUS	BUCK1_UV_STATUS
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-36. FAULT_STATUS_BUCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PVIN_UVLO_STATUS	R/W1C	0h	BUCK1 PVIN Under Voltage Status 0h = No Fault detected 1h = Fault detected
5	BUCK1_OV_STATUS	R/W1C	0h	BUCK1 Overvoltage Status 0h = No Fault detected 1h = Fault detected
4	BUCK1_HOT_STATUS	R/W1C	0h	BUCK1 Over Temperature Shutdown Status 0h = No Fault detected 1h = Fault detected
3	BUCK1_OVP_STATUS	R/W1C	0h	BUCK1 Overvoltage Protection Status 0h = No Fault detected 1h = Fault detected
2	BUCK1_SCG_STATUS	R/W1C	0h	BUCK1 Short Circuit to Ground Status 0h = No Fault detected 1h = Fault detected
1	BUCK1_OVL_STATUS	R/W1C	0h	BUCK1 Over-Load Protection Status 0h = No Fault detected 1h = Fault detected
0	BUCK1_UV_STATUS	R/W1C	0h	BUCK1 Undervoltage Status 0h = No Fault detected 1h = Fault detected

7.6.1.1.33 FAULT_STATUS_BUCK2 Register (Address = 20h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR

Figure 7-52. FAULT_STATUS_BUCK2 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK2_OV_STATUS	BUCK2_HOT_STATUS	BUCK2_OVP_STATUS	BUCK2_SCG_STATUS	BUCK2_OVL_STATUS	BUCK2_UV_STATUS
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-37. FAULT_STATUS_BUCK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	BUCK2_OV_STATUS	R/W1C	0h	BUCK2 Overvoltage Status 0h = No Fault detected 1h = Fault detected
4	BUCK2_HOT_STATUS	R/W1C	0h	BUCK2 Over Temperature Shutdown Status 0h = No Fault detected 1h = Fault detected
3	BUCK2_OVP_STATUS	R/W1C	0h	BUCK2 Overvoltage Protection Status 0h = No Fault detected 1h = Fault detected
2	BUCK2_SCG_STATUS	R/W1C	0h	BUCK2 Short Circuit to Ground Status 0h = No Fault detected 1h = Fault detected
1	BUCK2_OVL_STATUS	R/W1C	0h	BUCK2 Over-Load Protection Status 0h = No Fault detected 1h = Fault detected
0	BUCK2_UV_STATUS	R/W1C	0h	BUCK2 Undervoltage Status 0h = No Fault detected 1h = Fault detected

7.6.1.1.34 FAULT_STATUS_BUCK3 Register (Address = 21h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR

Figure 7-53. FAULT_STATUS_BUCK3 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK3_OV_STATUS	BUCK3_HOT_STATUS	BUCK3_OVP_STATUS	BUCK3_SCG_STATUS	BUCK3_OVL_STATUS	BUCK3_UV_STATUS
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-38. FAULT_STATUS_BUCK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	BUCK3_OV_STATUS	R/W1C	0h	BUCK3 Overvoltage Status 0h = No Fault detected 1h = Fault detected
4	BUCK3_HOT_STATUS	R/W1C	0h	BUCK3 Over Temperature Shutdown Status 0h = No Fault detected 1h = Fault detected
3	BUCK3_OVP_STATUS	R/W1C	0h	BUCK3 Overvoltage Protection Status 0h = No Fault detected 1h = Fault detected
2	BUCK3_SCG_STATUS	R/W1C	0h	BUCK3 Short Circuit to Ground Status 0h = No Fault detected 1h = Fault detected
1	BUCK3_OVL_STATUS	R/W1C	0h	BUCK3 Over-Load Protection Status 0h = No Fault detected 1h = Fault detected
0	BUCK3_UV_STATUS	R/W1C	0h	BUCK3 Undervoltage Status 0h = No Fault detected 1h = Fault detected

7.6.1.1.35 FAULT_STATUS_LDO Register (Address = 22h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR

Figure 7-54. FAULT_STATUS_LDO Register

7	6	5	4	3	2	1	0
RESERVED		LDO_OV_STATUS	LDO_HOT_STATUS	LDO_OVP_STATUS	LDO_SCG_STATUS	LDO_OVL_STATUS	LDO_UV_STATUS
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-39. FAULT_STATUS_LDO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	LDO_OV_STATUS	R/W1C	0h	LDO Overvoltage Status 0h = No Fault detected 1h = Fault detected
4	LDO_HOT_STATUS	R/W1C	0h	LDO Over Temperature Shutdown Status 0h = No Fault detected 1h = Fault detected
3	LDO_OVP_STATUS	R/W1C	0h	LDO Overvoltage Protection Status 0h = No Fault detected 1h = Fault detected
2	LDO_SCG_STATUS	R/W1C	0h	LDO Short Circuit to Ground Status 0h = No Fault detected 1h = Fault detected
1	LDO_OVL_STATUS	R/W1C	0h	LDO Over-Load Protection Status 0h = No Fault detected 1h = Fault detected
0	LDO_UV_STATUS	R/W1C	0h	LDO Undervoltage Status 0h = No Fault detected 1h = Fault detected

7.6.1.1.36 VMON_BUCK1_CFG Register (Address = 23h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-55. VMON_BUCK1_CFG Register

7	6	5	4	3	2	1	0
RESERVED				BUCK1_OV_SET		BUCK1_UV_SET	
R-0h				R/W-0h		R/W-0h	

Table 7-40. VMON_BUCK1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-2	BUCK1_OV_SET	R/W	0h	BUCK1 OV detection threshold with respect to target voltage setting: 0h = 104% 1h = 104.5% 2h = 105% 3h = 105.5%
1-0	BUCK1_UV_SET	R/W	0h	BUCK1 UV detection threshold with respect to target voltage setting: 0h = 96% 1h = 95.5% 2h = 95% 3h = 94.5%

7.6.1.1.37 VMON_BUCK2_CFG Register (Address = 24h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-56. VMON_BUCK2_CFG Register

7	6	5	4	3	2	1	0
RESERVED				BUCK2_OV_SET		BUCK2_UV_SET	
R-0h				R/W-0h		R/W-0h	

Table 7-41. VMON_BUCK2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-2	BUCK2_OV_SET	R/W	0h	BUCK2 OV detection threshold with respect to target voltage setting: 0h = 104% 1h = 104.5% 2h = 105% 3h = 105.5%
1-0	BUCK2_UV_SET	R/W	0h	BUCK2 UV detection threshold with respect to target voltage setting: 0h = 96% 1h = 95.5% 2h = 95% 3h = 94.5%

7.6.1.1.38 VMON_BUCK3_CFG Register (Address = 25h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-57. VMON_BUCK3_CFG Register

7	6	5	4	3	2	1	0
RESERVED				BUCK3_OV_SET		BUCK3_UV_SET	
R-0h				R/W-0h		R/W-0h	

Table 7-42. VMON_BUCK3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-2	BUCK3_OV_SET	R/W	0h	BUCK3 OV detection threshold with respect to target voltage setting: 0h = 104% 1h = 104.5% 2h = 105% 3h = 105.5%
1-0	BUCK3_UV_SET	R/W	0h	BUCK3 UV detection threshold with respect to target voltage setting: 0h = 96% 1h = 95.5% 2h = 95% 3h = 94.5%

7.6.1.1.39 VMON_LDO_CFG Register (Address = 26h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-58. VMON_LDO_CFG Register

7	6	5	4	3	2	1	0
RESERVED				LDO_OV_SET		LDO_UV_SET	
R-0h				R/W-0h		R/W-0h	

Table 7-43. VMON_LDO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-2	LDO_OV_SET	R/W	0h	LDO OV detection threshold with respect to target voltage setting: 0h = 104% 1h = 104.5% 2h = 105% 3h = 105.5%
1-0	LDO_UV_SET	R/W	0h	LDO UV detection threshold with respect to target voltage setting: 0h = 96.5% 1h = 96% 2h = 95.5% 3h = 95%

7.6.1.1.40 ERR_BUCKx_LDO_CFG Register (Address = 27h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-59. ERR_BUCKx_LDO_CFG Register

7	6	5	4	3	2	1	0
BUCK3_OV_RST_EN	BUCK3_UV_RST_EN	BUCK2_OV_RST_EN	BUCK2_UV_RST_EN	BUCK1_OV_RST_EN	BUCK1_UV_RST_EN	LDO_OV_RST_EN	LDO_UV_RST_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-44. ERR_BUCKx_LDO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK3_OV_RST_EN	R/W	0h	BUCK3 Over Voltage Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the State Transition bit
6	BUCK3_UV_RST_EN	R/W	0h	BUCK3 Under Voltage Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the State Transition bit
5	BUCK2_OV_RST_EN	R/W	0h	BUCK2 Over Voltage Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the State Transition bit
4	BUCK2_UV_RST_EN	R/W	0h	BUCK2 Under Voltage Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the State Transition bit
3	BUCK1_OV_RST_EN	R/W	0h	BUCK1 Over Voltage Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the State Transition bit
2	BUCK1_UV_RST_EN	R/W	0h	BUCK1 Under Voltage Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the State Transition bit
1	LDO_OV_RST_EN	R/W	0h	LDO Over Voltage Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the State Transition bit
0	LDO_UV_RST_EN	R/W	0h	LDO Under Voltage Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the State Transition bit

7.6.1.1.41 RESTART_CMD Register (Address = 28h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR

Figure 7-60. RESTART_CMD Register

7	6	5	4	3	2	1	0
PMIC_RESTART_CMD							
R-0h							

Table 7-45. RESTART_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PMIC_RESTART_CMD	R	0h	Write to this register to re-start the device. A readback of this register results in '0x00'. DDh = Re-start the device

7.6.1.1.42 CFG_REG_CRC Register (Address = 29h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK

Figure 7-61. CFG_REG_CRC Register

7	6	5	4	3	2	1	0
DEV_CFG_CRC							
R/W-0h							

Table 7-46. CFG_REG_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEV_CFG_CRC	R/W	0h	Expected CRC8 value for device configuration registers

7.6.1.1.43 DEV_STAT Register (Address = 2Ah) [Reset = 0Ch]

Return to the Summary Table.

Initialization source: POR

Figure 7-62. DEV_STAT Register

7	6	5	4	3	2	1	0
RESERVED				CTRL_LOCK	CFG_LOCK	DEV_STATE	
R-0h				R-1h	R-1h	R-0h	

Table 7-47. DEV_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	CTRL_LOCK	R	1h	Control Lock Status 0h = Write access allowed based on CONTROL_LOCK Register 1h = Write access not allowed based on CONTROL_LOCK Register
2	CFG_LOCK	R	1h	Configuration Lock Status 0h = Write access allowed based on CONFIG_LOCK Register 1h = Write access not allowed based on CONFIG_LOCK Register
1-0	DEV_STATE	R	0h	Device State 0h = Any State other than the ACTIVE, RESET or SAFE State 1h = ACTIVE State 2h = RESET State 3h = SAFE State

7.6.1.1.44 DEV_ERR_ACK_1 Register (Address = 2Bh) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-63. DEV_ERR_ACK_1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	SYSTEM_ERR_ACK	ABIST_LDO_ACK	ABIST_BUCK3_ACK	ABIST_BUCK2_ACK	ABIST_BUCK1_ACK
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-48. DEV_ERR_ACK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	SYSTEM_ERR_ACK	R	0h	System Error Acknowledge 0h = No error detected 1h = Error detected
3	ABIST_LDO_ACK	R	0h	ABIST LDO Error Acknowledge 0h = Not detected 1h = Detected
2	ABIST_BUCK3_ACK	R	0h	ABIST BUCK3 Error Acknowledge 0h = Not detected 1h = Detected
1	ABIST_BUCK2_ACK	R	0h	ABIST BUCK2 Error Acknowledge 0h = Not detected 1h = Detected
0	ABIST_BUCK1_ACK	R	0h	ABIST BUCK1 Error Acknowledge 0h = Not detected 1h = Detected

7.6.1.1.45 DEV_ERR_ACK_2 Register (Address = 2Ch) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-64. DEV_ERR_ACK_2 Register

7	6	5	4	3	2	1	0
RESERVED			CFG_REG_CRC_ERR_ACK	nINT_ERR_ACK	nRSTOUT_ERR_ACK	I2C_INVALID_ADDR_ERR_ACK	I2C_CRC_ERR_ACK
R-0h			R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-49. DEV_ERR_ACK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	CFG_REG_CRC_ERR_ACK	R/W1C	0h	CFG Register CRC Error Acknowledge 0h = No error detected 1h = Error detected
3	nINT_ERR_ACK	R/W1C	0h	nINT Error Acknowledge 0h = No error detected 1h = Error detected
2	nRSTOUT_ERR_ACK	R/W1C	0h	nRSTOUT Error Acknowledge 0h = No error detected 1h = Error detected
1	I2C_INVALID_ADDR_ERR_ACK	R/W1C	0h	I2C Invalid Address Error Acknowledge 0h = No error detected 1h = Error detected
0	I2C_CRC_ERR_ACK	R/W1C	0h	I2C CRC Error Acknowledge 0h = No error detected 1h = Error detected

7.6.1.1.46 DEV_FAULT_STATUS_1 Register (Address = 2Dh) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR

Figure 7-65. DEV_FAULT_STATUS_1 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESERVED	RESERVED	RESTART_CMD_STATUS	VREG_OVP_STATUS	VREG_UV_STATUS
R-0h		R-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-50. DEV_FAULT_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESTART_CMD_STATUS	R/W1C	0h	The previous shutdown was due to a Restart Command from the MCU 0h = Not detected 1h = Detected
1	VREG_OVP_STATUS	R/W1C	0h	VREG over voltage protection error status 0h = Not detected 1h = Detected
0	VREG_UV_STATUS	R/W1C	0h	VREG under voltage detection error status 0h = Not detected 1h = Detected

7.6.1.1.47 DEV_FAULT_STATUS_2 Register (Address = 2Eh) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR

Figure 7-66. DEV_FAULT_STATUS_2 Register

7	6	5	4	3	2	1	0
RESERVED			nINT_ERR_STATUS	nRSTOUT_ERR_STATUS	NVM_CRC_ERR_STATUS	RESERVED	GND_LOSS_ERR_STATUS
R-0h			R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h

Table 7-51. DEV_FAULT_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	nINT_ERR_STATUS	R/W1C	0h	nINT pin monitor detection error status 0h = Not detected 1h = Detected
3	nRSTOUT_ERR_STATUS	R/W1C	0h	nRSTOUT pin monitor detection error status 0h = Not detected 1h = Detected
2	NVM_CRC_ERR_STATUS	R/W1C	0h	NVM CRC detection error status 0h = Not detected 1h = Detected
1	RESERVED	R	0h	Reserved
0	GND_LOSS_ERR_STATUS	R/W1C	0h	Ground Loss detection error status 0h = Not detected 1h = Detected

7.6.1.1.48 INT_MASK_SAFETY Register (Address = 2Fh) [Reset = 03h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-67. INT_MASK_SAFETY Register

7	6	5	4	3	2	1	0
RESERVED						I2C_INVALID_ADDR_MASK	I2C_CRC_ERR_MASK
R-0h						R/W-1h	R/W-1h

Table 7-52. INT_MASK_SAFETY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	I2C_INVALID_ADDR_MASK	R/W	1h	I2C Invalid Address Interrupt Mask 0h = Not Masked 1h = Masked
0	I2C_CRC_ERR_MASK	R/W	1h	I2C CRC Error Interrupt Mask 0h = Not Masked 1h = Masked

7.6.1.1.49 PIN_MON_ERR_CFG Register (Address = 30h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE
Protection Access : CFG_LOCK
CFG_CRC : YES

Figure 7-68. PIN_MON_ERR_CFG Register

7	6	5	4	3	2	1	0
RESERVED						nINT_ERR_RST_EN	nRSTOUT_ERR_RST_EN
R-0h						R/W-0h	R/W-0h

Table 7-53. PIN_MON_ERR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	nINT_ERR_RST_EN	R/W	0h	nINT_ERR Pin Monitor Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET state
0	nRSTOUT_ERR_RST_EN	R/W	0h	nRSTOUT_ERR Pin Monitor Fault Configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET state

7.6.1.1.50 ABIST_GROUP_DONE Register (Address = 31h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-69. ABIST_GROUP_DONE Register

7	6	5	4	3	2	1	0
RESERVED			ABIST_SYS	ABIST_LDO	ABIST_BUCK3	ABIST_BUCK2	ABIST_BUCK1
R-0h			R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-54. ABIST_GROUP_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	ABIST_SYS	R/W1C	0h	ABIST System is done. 0h = Not done 1h = Done
3	ABIST_LDO	R/W1C	0h	ABIST LDO is done. 0h = Not done 1h = Done
2	ABIST_BUCK3	R/W1C	0h	ABIST BUCK3 is done. 0h = Not done 1h = Done
1	ABIST_BUCK2	R/W1C	0h	ABIST BUCK2 is done. 0h = Not done 1h = Done
0	ABIST_BUCK1	R/W1C	0h	ABIST BUCK1 is done. 0h = Not done 1h = Done

7.6.1.1.51 ABIST_BUCK1_2_ACK Register (Address = 32h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-70. ABIST_BUCK1_2_ACK Register

7	6	5	4	3	2	1	0
RESERVED	ABIST_BUCK2_OVP_ACK	ABIST_BUCK2_OV_ACK	ABIST_BUCK2_UV_ACK	RESERVED	ABIST_BUCK1_OVP_ACK	ABIST_BUCK1_OV_ACK	ABIST_BUCK1_UV_ACK
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-55. ABIST_BUCK1_2_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	ABIST_BUCK2_OVP_ACK	R/W1C	0h	ABIST BUCK2 Over Voltage Protection Error Acknowledge 0h = Not detected 1h = Detected
5	ABIST_BUCK2_OV_ACK	R/W1C	0h	ABIST BUCK2 Over Voltage Error Acknowledge 0h = Not detected 1h = Detected
4	ABIST_BUCK2_UV_ACK	R/W1C	0h	ABIST BUCK2 Under Voltage Error Acknowledge 0h = Not detected 1h = Detected
3	RESERVED	R	0h	
2	ABIST_BUCK1_OVP_ACK	R/W1C	0h	ABIST BUCK1 Over Voltage Protection Error Acknowledge 0h = Not detected 1h = Detected
1	ABIST_BUCK1_OV_ACK	R/W1C	0h	ABIST BUCK1 Over Voltage Error Acknowledge 0h = Not detected 1h = Detected
0	ABIST_BUCK1_UV_ACK	R/W1C	0h	ABIST BUCK1 Under Voltage Error Acknowledge 0h = Not detected 1h = Detected

7.6.1.1.52 ABIST_LDO_BUCK3_ACK Register (Address = 33h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-71. ABIST_LDO_BUCK3_ACK Register

7	6	5	4	3	2	1	0
RESERVED	ABIST_LDO_OVP_ACK	ABIST_LDO_OV_ACK	ABIST_LDO_UV_ACK	RESERVED	ABIST_BUCK3_OVP_ACK	ABIST_BUCK3_OV_ACK	ABIST_BUCK3_UV_ACK
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 7-56. ABIST_LDO_BUCK3_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	ABIST_LDO_OVP_ACK	R/W1C	0h	ABIST LDO Over Voltage Protection Error Acknowledge 0h = Not detected 1h = Detected
5	ABIST_LDO_OV_ACK	R/W1C	0h	ABIST LDO Over Voltage Error Acknowledge 0h = Not detected 1h = Detected
4	ABIST_LDO_UV_ACK	R/W1C	0h	ABIST LDO Under Voltage Error Acknowledge 0h = Not detected 1h = Detected
3	RESERVED	R	0h	
2	ABIST_BUCK3_OVP_ACK	R/W1C	0h	ABIST BUCK3 Over Voltage Protection Error Acknowledge 0h = Not detected 1h = Detected
1	ABIST_BUCK3_OV_ACK	R/W1C	0h	ABIST BUCK3 Over Voltage Error Acknowledge 0h = Not detected 1h = Detected
0	ABIST_BUCK3_UV_ACK	R/W1C	0h	ABIST BUCK3 Under Voltage Error Acknowledge 0h = Not detected 1h = Detected

7.6.1.1.53 ABIST_SYSTEM_ACK Register (Address = 34h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR, RESET STATE

Figure 7-72. ABIST_SYSTEM_ACK Register

7	6	5	4	3	2	1	0
RESERVED					ABIST_SYSTEM_TSHUT_ACK	RESERVED	ABIST_GNDLOSS_ERR_ACK
R-0h					R/W1C-0h	R-0h	R/W1C-0h

Table 7-57. ABIST_SYSTEM_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	ABIST_SYSTEM_TSHUT_ACK	R/W1C	0h	ABIST thermal shutdown Error Acknowledge 0h = Not detected 1h = Detected
1	RESERVED	R	0h	Reserved
0	ABIST_GNDLOSS_ERR_ACK	R/W1C	0h	ABIST ground loss Error Acknowledge 0h = Not detected 1h = Detected

7.6.1.1.54 ABIST_RUN_CMD Register (Address = 35h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR
Protection Access : Factory programming controlled

Figure 7-73. ABIST_RUN_CMD Register

7	6	5	4	3	2	1	0
ABIST_CONTROL							
R-0h							

Table 7-58. ABIST_RUN_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ABIST_CONTROL	R	0h	Write to this register to run ABIST. A readback of this register results in '0x00'. DAh = Run ABIST real time

7.6.1.1.55 POWER_GOOD_STATUS Register (Address = 36h) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR

Figure 7-74. POWER_GOOD_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	nRSTOUT_STATUS	GPIO_STATUS	SEQ_STATUS	LDO_PG_STATUS	BUCK3_PG_STATUS	BUCK2_PG_STATUS	BUCK1_PG_STATUS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-59. POWER_GOOD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	nRSTOUT_STATUS	R	0h	nRSTOUT Pin Logic Level Status 0h = nRSTOUT pin is at a low level 1h = nRSTOUT pin is at a high level
5	GPIO_STATUS	R	0h	GPIO Pin Logic Level Status (for both input and output) 0h = GPIO pin is at a low level 1h = GPIO pin is at a high level
4	SEQ_STATUS	R	0h	SEQ Pin Logic Level Status 0h = SEQ pin is at a low level 1h = SEQ pin is at a high level
3	LDO_PG_STATUS	R	0h	LDO Power Good Status 0h = Voltage rail is not within regulation limits 1h = Voltage rail is within regulation limits
2	BUCK3_PG_STATUS	R	0h	BUCK3 Power Good Status 0h = Voltage rail is not within regulation limits 1h = Voltage rail is within regulation limits
1	BUCK2_PG_STATUS	R	0h	BUCK2 Power Good Status 0h = Voltage rail is not within regulation limits 1h = Voltage rail is within regulation limits
0	BUCK1_PG_STATUS	R	0h	BUCK1 Power Good Status 0h = Voltage rail is not within regulation limits 1h = Voltage rail is within regulation limits

7.6.1.1.56 EEPROM_PROG_CMD Register (Address = 4Ah) [Reset = 00h]

Return to the Summary Table.

Initialization source: POR
Protection Access : Factory programming controlled
(Note: This register is only active when the Factory setting of User Programmability is enabled)

Figure 7-75. EEPROM_PROG_CMD Register

7	6	5	4	3	2	1	0
PROG_ACCESS_CMD							
R-0h							

Table 7-60. EEPROM_PROG_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PROG_ACCESS_CMD	R	0h	Write to this register to enable the NVM LDO and program the EEPROM. A readback of this register results in '0x00'. 2Dh = Enable NVM LDO and program eeprom.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Texas Instruments TPS650332-Q1 device is designed for automotive camera modules.

8.2 Typical Application

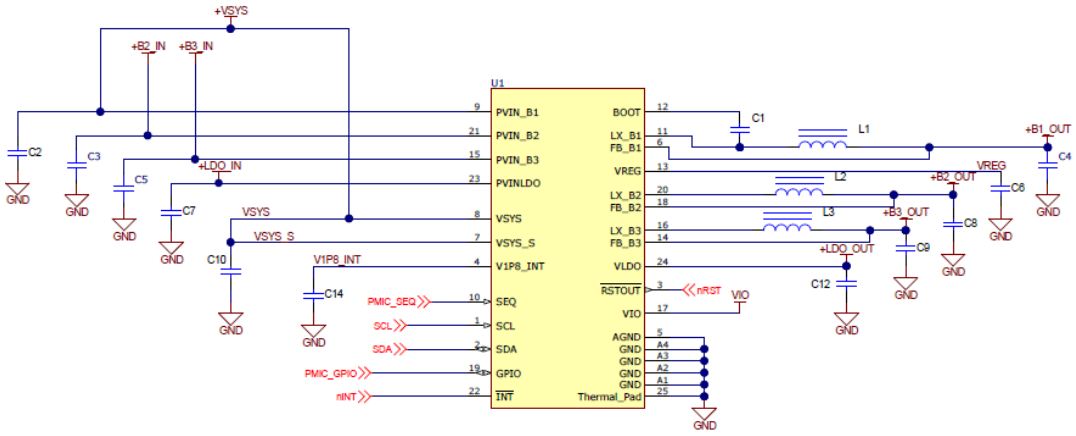


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Use the parameters listed in Table 8-1 for this design example.

Table 8-1. Design Parameters

RESOURCES	VOLTAGE
BUCK1	3.3 V
BUCK2	1.8 V
BUCK3	1.2 V
VLDO	2.8 V

8.2.2 Detailed Design Procedure

8.2.2.1 BUCK1 Output Filter Design (Inductor and Output Capacitor)

8.2.2.1.1 BUCK1 Inductor Selection

The typical value for the converter output inductor is 1.5 µH. The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductance influences the efficiency of the converter directly. An inductor with the lowest DC resistance must be selected for highest efficiency. Refer to the *Choosing Inductors and Capacitors for DC/DC Converters* application report for more information on inductor selection.

Use Equation 1 to calculate the maximum inductor current under static load conditions (ΔI_L). Select an inductor with a saturation current higher than the maximum inductor current as calculated with Equation 2 because, the inductor current rises above the calculated value during heavy load transients.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (1)$$

where

- f is the switching frequency (2.3 MHz typical).
- L is the inductor value.
- ΔI_L is the peak-to-peak inductor ripple current.

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- I_{Lmax} is the maximum inductor current

The highest inductor current occurs at the maximum input voltage (V_{IN}).

Table 8-2 shows the recommended inductor.

Table 8-2. Recommended Inductors

INDUCTOR	INDUCTANCE (µH)	SUPPLIER	MAX DIMENSIONS (mm)
TFM201610ALMA1R5MTAA	1.5	TDK	2.0 × 1.6 × 1.0

8.2.2.1.2 BUCK1 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the converter allows the use of small ceramic capacitors with a typical value of 10 µF without large output voltage undershoots and overshoots during heavy load transients. TI recommends using ceramic capacitors with low ESR values because they result in the lowest output-voltage ripple. Table 8-3 lists the recommended capacitors.

If ceramic output capacitors are used, the RMS ripple-current rating of the capacitor always meets the application requirements. Use Equation 3 to calculate the RMS ripple current ($I_{RMSCout}$).

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (3)$$

The device operates in PWM mode. The overall output-voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor. Use Equation 4 to calculate the ΔV_{OUT} value.

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (4)$$

The highest output-voltage ripple occurs at the highest input voltage.

8.2.2.1.3 BUCK1 Input Capacitor Selection

DC-DC converters have pulsating input currents that can create high-input voltage spikes, which interfere with other circuits. A low-ESR input capacitor provides the best input voltage filtering to minimize these voltage spikes. Place the input capacitor as close to the PVIN_Bx pin as possible with a clean ground connection. Do the same for the output capacitor and the inductor. The converters require a ceramic input capacitor of 10 µF. The input capacitor can increase without any limit for better input voltage filtering.

Table 8-3. BUCK1 Recommended Capacitors

CAPACITANCE	SUPPLIER	TYPE
10 µF (input)	Kemet C1206C106J3RACAUTO	Ceramic
10 µF (output)	TDK CGA4J3X7S1A106K125AE	Ceramic

8.2.2.2 BUCK2/BUCK3 Output Filter Design (Inductor and Output Capacitor)

8.2.2.2.1 BUCK2/BUCK3 Inductor Selection

The typical value for the converter output inductor is 1.0 µH. The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductance influences the efficiency of the converter directly. An inductor with the lowest DC resistance must be selected for highest efficiency. Refer to the *Choosing Inductors and Capacitors for DC/DC Converters* application report for more information on inductor selection.

Use Equation 1 to calculate the maximum inductor current under static load conditions (ΔI_L). Select an inductor with a saturation current higher than the maximum inductor current as calculated with Equation 2 because, the inductor current rises above the calculated value during heavy load transients.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \tag{5}$$

where

- f is the switching frequency (2.3 MHz typical).
- L is the inductor value.
- ΔI_L is the peak-to-peak inductor ripple current.

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \tag{6}$$

where

- I_{Lmax} is the maximum inductor current

The highest inductor current occurs at the maximum input voltage (V_{IN}).

Table 8-2 shows the recommended inductor.

Table 8-4. Recommended Inductors

INDUCTOR TYPE	INDUCTANCE (µH)	SUPPLIER	MAX DIMENSIONS (mm)
TFM201610ALMA1R0MTAA	1.0	TDK	2.0 × 1.6 × 1.0

8.2.2.2.2 BUCK2 and BUCK3 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the converter allows the use of small ceramic capacitors with a typical value of 10 µF without large output voltage undershoots and overshoots during heavy load transients. TI recommends using ceramic capacitors with low ESR values because they result in the lowest output-voltage ripple. Table 8-3 lists the recommended capacitors.

If ceramic output capacitors are used, the RMS ripple-current rating of the capacitor always meets the application requirements. Use Equation 3 to calculate the RMS ripple current ($I_{RMSCout}$).

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (7)$$

The device operates in PWM mode. The overall output-voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor. Use Equation 4 to calculate the ΔV_{OUT} value.

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (8)$$

The highest output-voltage ripple occurs at the highest input voltage.

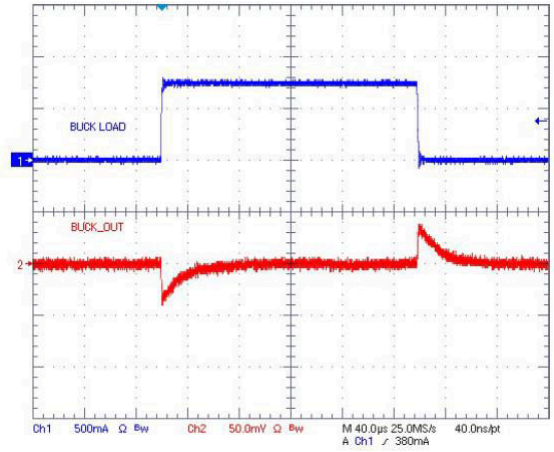
8.2.2.2.3 BUCK2 and BUCK3 Input Capacitor Selection

DC-DC converters have pulsating input currents that can create high-input voltage spikes, which interfere with other circuits. A low-ESR input capacitor provides the best input voltage filtering to minimize these voltage spikes. Place the input capacitor as close to the PVIN_Bx pin as possible with a clean ground connection. Do the same for the output capacitor and the inductor. The converters require a ceramic input capacitor of 10 µF. The input capacitor can increase without any limit for better input voltage filtering.

Table 8-5. BUCK2/BUCK3 Recommended Capacitors

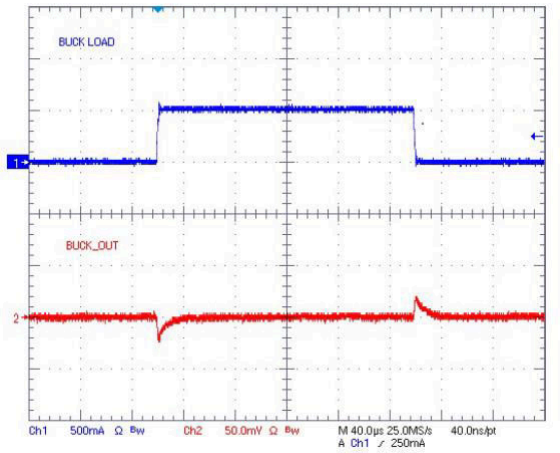
CAPACITANCE	SUPPLIER	TYPE
10 µF (input)	TDK CGA4J3X7S1A106K125AE	Ceramic
10 µF (output)	Taiyo Yuden JMJ212CB7106KGHT	Ceramic

8.2.3 Application Curves



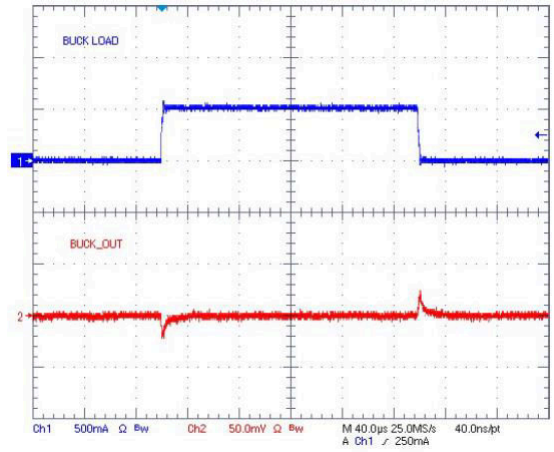
V_{PVIN_B1} = 12 V T_A = 25°C
V_{OUT} = 3.3 V 1 mA ≤ I_{LOAD} ≤ 750 mA

Figure 8-2. BUCK1 Load Transient Response



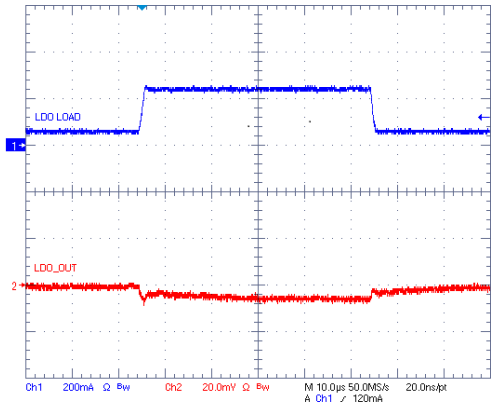
V_{PVIN_B2} = 3.3 V T_A = 25°C
V_{OUT} = 1.8 V 1 mA ≤ I_{LOAD} ≤ 600 mA

Figure 8-3. BUCK2 Load Transient Response



V_{PVIN_B3} = 3.3 V T_A = 25°C
V_{OUT} = 1.2 V 1 mA ≤ I_{LOAD} ≤ 600 mA

Figure 8-4. BUCK3 Load Transient Response



V_{PVIN_LDO} = 3.3 V T_A = 25°C
V_{OUT} = 2.8 V 60 mA ≤ $I_{LOAD(LDOx)}$ ≤ 240 mA

Figure 8-5. LDO Load Transient Response

9 Power Supply Recommendations

The device is designed to operate with an input voltage supply range from 4.0 V to 18.3 V. This input supply comes from a conditioned power source for automotive applications.

10 Layout

10.1 Layout Guidelines

Follow these general component placement guidelines for good printed circuit board (PCB) design:

- The PVIN_B1, PVIN_B2, PVIN_B3, and VINLDO pins must each be bypassed to ground with a low-ESR ceramic bypass capacitor. TI recommends using the typical bypass capacitance of 10 µF for the DC-DC converters and 2.2 µF for the LDO with a X7R dielectric. Ensure capacitor meets minimum capacitance under all operating conditions.
- The optimum capacitor placement is closest to the PVIN_Bx and VINLDO pins of the device. Minimize the loop area formed by the bypass capacitor connection from the PVIN_Bx and the thermal pad of the device. Minimize the loop area formed by the bypass capacitor connection from the VINLDO and the AGND pin of the device.
- The thermal pad must be tied to the PCB ground plane with multiple vias.
- Isolate AGND from Thermal Pad on shared layer. Separately connect AGND and Thermal Pad to GND plane using vias.
- The PVIN_Bx feedback traces must be routed away from any potential noise source to avoid coupling.
- The optimum placement of the VREG and V1P8_INT output capacitors is directly at their respective pins.
- Excessive distances of input and output capacitors for regulator pins may cause poor converter performance.
- Minimize loop area of bootstrap capacitor from LX_B1 to BOOT pin.

Note

Placement of the bootstrap capacitor is critical. Minimize the parasitic inductance introduced by the traces between the bootstrap capacitor and the pins of the device to less than 1.5nH per trace.

- Connect VSYS to VSYS_S directly at device pins with a localized decoupling capacitor. Connect VSYS to PVIN_B1 before the VSYS decoupling capacitor. Dedicate one input decoupling capacitor to PVIN_B1.

10.2 Layout Example

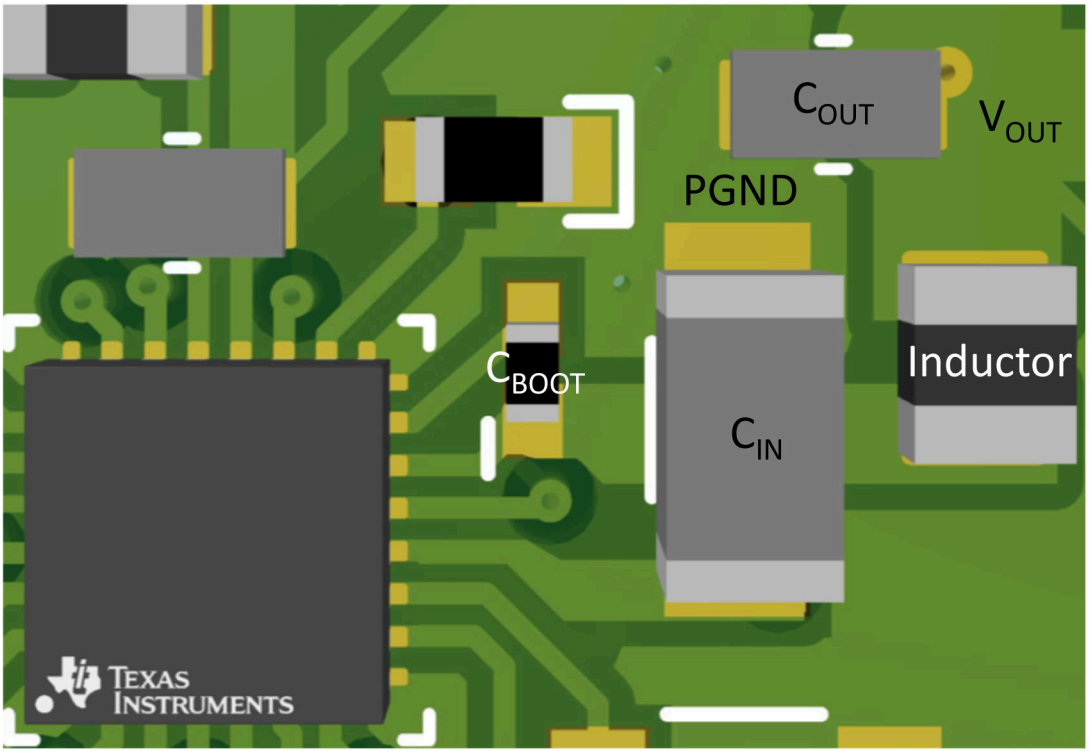


Figure 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

12.1 Package Option Addendum

Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TPS65033203RGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	SN	Level3-260C	-40ºC to 125ºC	TPS65033203-Q1
TPS65033207RGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	SN	Level3-260C	-40ºC to 125ºC	TPS65033207-Q1
TPS6503320DRGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	SN	Level3-260C	-40ºC to 125ºC	TPS6503320D-Q1
TPS6503320FRGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	SN	Level3-260C	-40ºC to 125ºC	TPS6503320F-Q1
TPS6503320GRGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	SN	Level3-260C	-40ºC to 125ºC	TPS6503320G-Q1
TPS6503320HARGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	SN	Level3-260C	-40ºC to 125ºC	TPS6503320HA-Q1

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

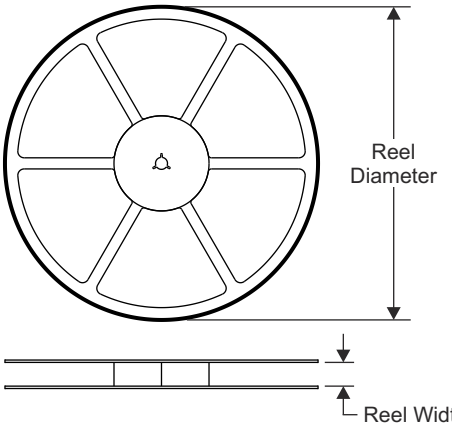
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

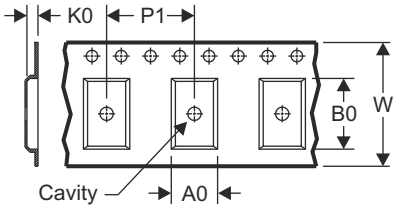
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

12.2 Tape and Reel Information

REEL DIMENSIONS

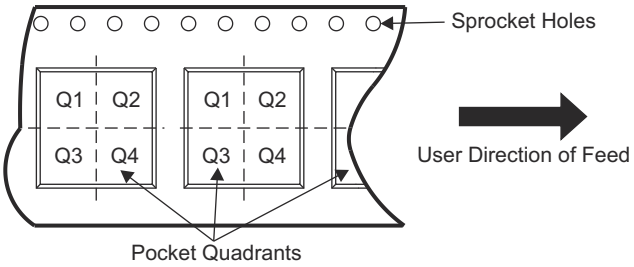


TAPE DIMENSIONS



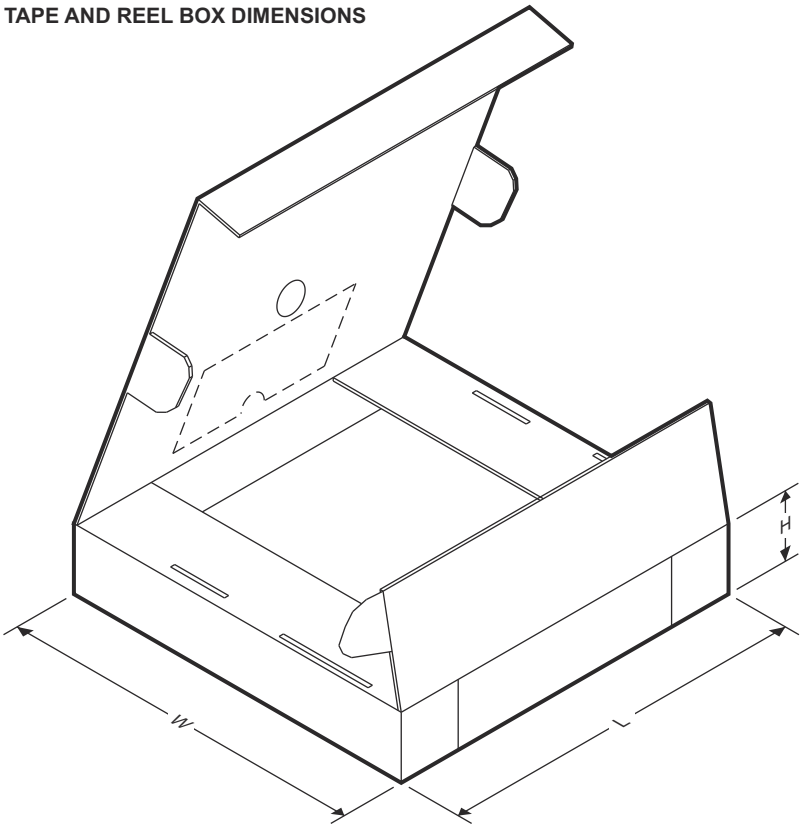
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65033203RGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2
TPS65033207RGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2
TPS6503320DRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2
TPS6503320FRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2
TPS6503320GRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2
TPS6503320HARGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



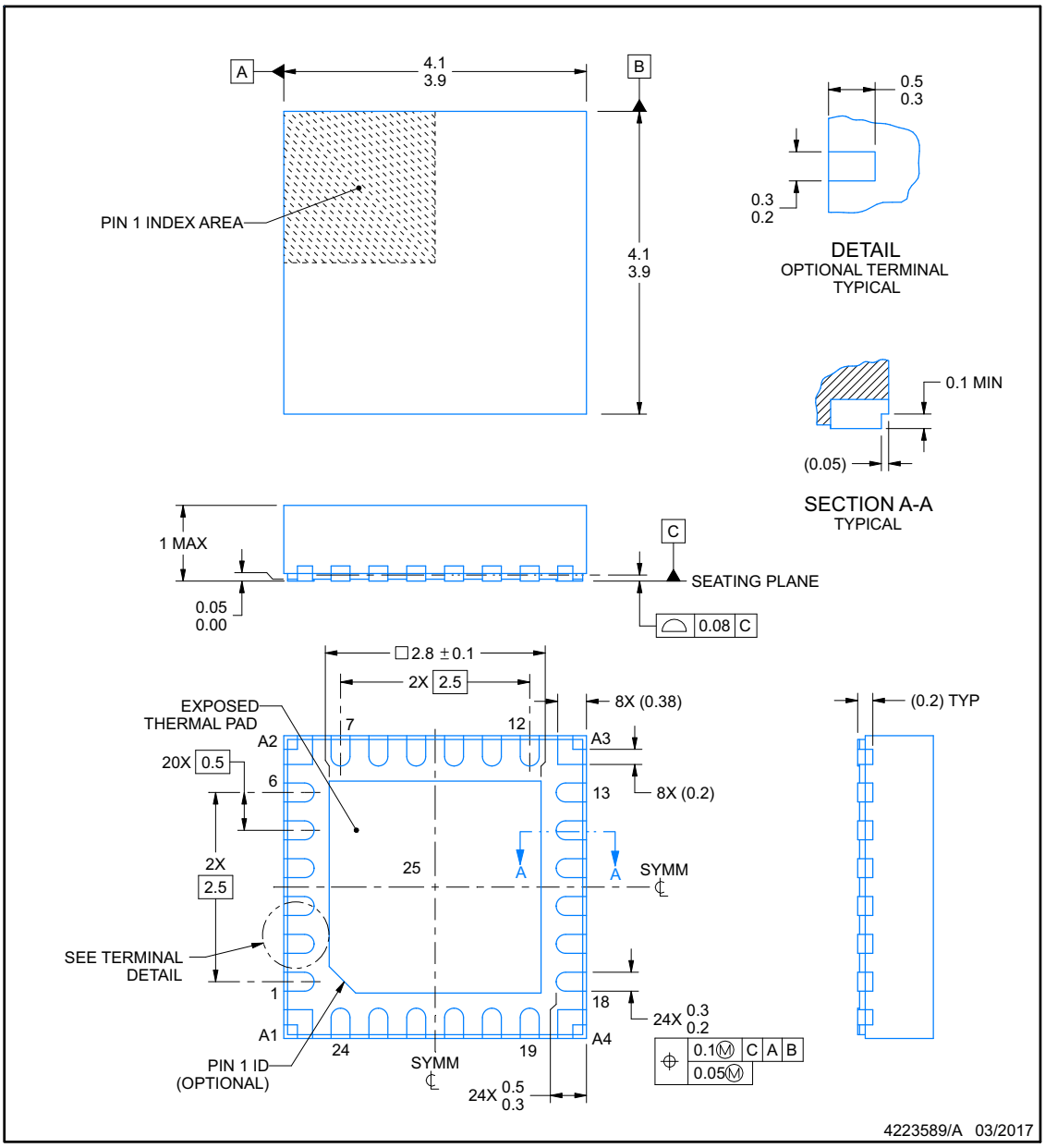
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65033203RGERQ1	VQFN	RGE	24	3000	213.0	191.0	35.0
TPS65033207RGERQ1	VQFN	RGE	24	3000	213.0	191.0	35.0
TPS6503320DRGERQ1	VQFN	RGE	24	3000	213.0	191.0	35.0
TPS6503320FRGERQ1	VQFN	RGE	24	3000	213.0	191.0	35.0
TPS6503320GRGERQ1	VQFN	RGE	24	3000	213.0	191.0	35.0
TPS6503320HARGERQ1	VQFN	RGE	24	3000	213.0	191.0	35.0

PACKAGE OUTLINE

RGE0024K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

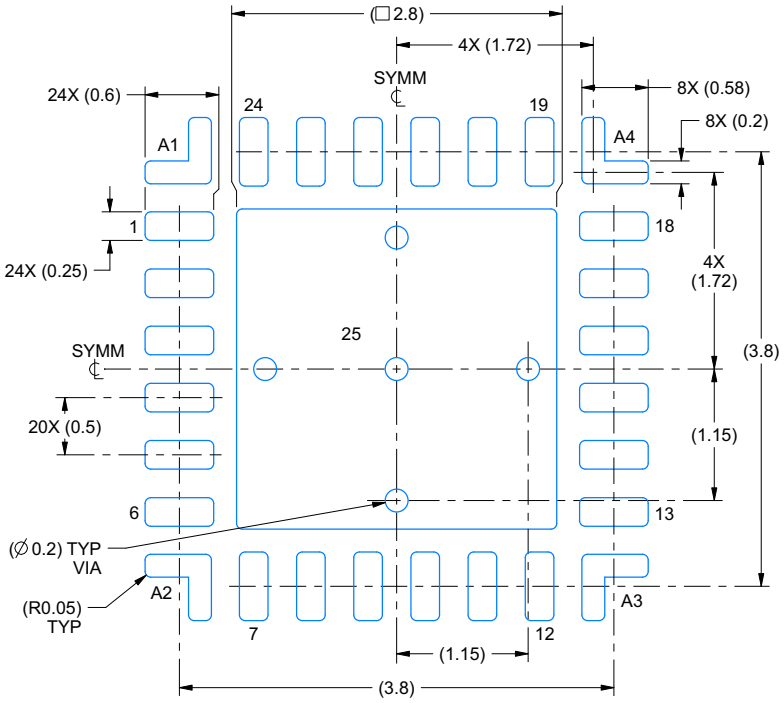
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

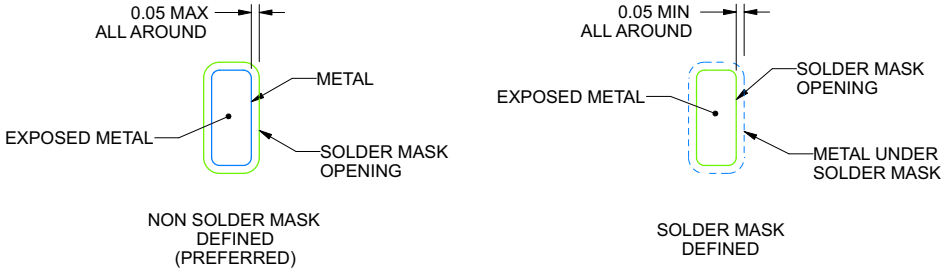
RGE0024K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

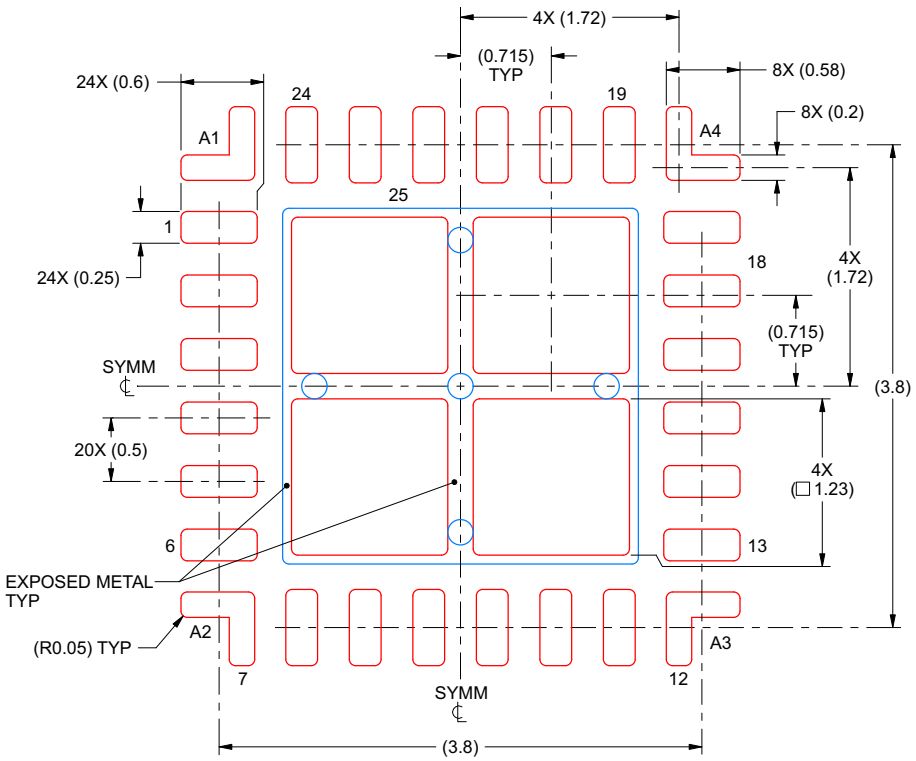
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 25:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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