9.6.3 Power Path Control Register (PPATH)

Figure 26. Power Path Control Register (PPATH)
Address – 0x01h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ACSINK	USBSINK	AC_EN	USB_EN	IAC[1:0]		IUSB[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	1	1	1	1	0	1

Table 2. Power Path Control Register (PPATH) Field Descriptions

Bit	Field	Type	Reset	Description
D7	ACSINK	R/W	0	AC current-sink control 0 – AC sink is enabled when USB is a valid supply and V_{AC} is below the detection threshold 1 – Set [ACSINK, USBSINK] = 11 to force both (AC and USB) current sinks OFF NOTE: [ACSINK, USBSINK] = 01b and 10b combinations are not recommended, as these may lead to unexpected enabling and disabling of the current sinks.
D6	USBSINK	R/W	1	USB current-sink control 0 – USB sink is enabled when AC is a valid supply and V_{USB} is below the detection threshold 1 – Set [ACSINK, USBSINK] = 11 to force both (AC and USB) current sinks OFF NOTE: [ACSINK, USBSINK] = 01b and 10b combinations are not recommended, as these may lead to unexpected enabling and disabling of the current sinks.
D5	AC_EN	R/W	1	AC power path enable 0 – AC power input is turned off. 1 – AC power input is turned on.
D4	USB_EN	R/W	1	USB power path enable 0 – USB power input is turned off (USB suspend mode). 1 – USB power input is turned on.
D3–D2	IAC[1:0]	R/W	1	AC input-current limit 00 – 100 mA 01 – 500 mA 10 – 1300 mA 11 – 2500 mA
D1–D0	IUSB[1:0]	R/W	1	USB input-current limit 00 – 100 mA 01 – 500 mA 10 – 1300 mA 11 – 1800 mA

Product Folder Links: *TPS65217*