

UCCx895 PSPICE/TINA Model Translation Report

Date: 27JUN2011

Revision: 1.2

Author: Veeresh Huggi

Simulator Names and Versions:

- PSPICE 16.0.0.p001
- TINA 9.0.10.194 SF

Description of Model: BiCMOS ADVANCED PHASE-SHIFT PWM CONTROLLER

Document Revision History:

REVISION NO.	DESCRIPTION	REVISION DATE	REMARKS
1.0	Initial Release	04OCT2010	
1.1	Post-QC review inputs incorporating and re-release of the component.	31DEC2010	
1.2	Re-releasing due to change in the lib file	27JUN2011	

Contents

1.	Model Modification.....	4
2.	Analysis Parameters	5
2.1.	PSPICE	5
2.2.	TINA.....	5
3.	TINA schematic v/s published (STARTUP) PSPICE schematic	6
3.1.	Transient Analysis.....	6
3.2.	Average Analysis	9
4.	Validation across EVM Corners.....	12
4.1	Transient Analysis.....	12
4.1.1	Condition 1 ($V_{IN_{MIN}} = 36V$, $I_{LOAD_{MIN}} = 0A$).....	12
4.1.2	Condition 2 ($V_{IN_{MIN}} = 36V$, $I_{LOAD_{MAX}} = 14A$)	14
4.1.3	Condition 3 ($V_{IN_{MAX}} = 72V$, $I_{LOAD_{MIN}} = 0A$)	16
4.1.4	Condition 4 ($V_{IN_{MAX}} = 72V$, $I_{LOAD_{MAX}} = 14A$)	18
4.2	Average Analysis	20
4.2.1	Condition 1 ($V_{IN_{MIN}} = 36V$, $I_{LOAD_{MIN}} = 0A$).....	20
4.2.2	Condition 2 ($V_{IN_{MIN}} = 36V$, $I_{LOAD_{MAX}} = 15A$)	22
4.2.3	Condition 3 ($V_{IN_{MAX}} = 72V$, $I_{LOAD_{MIN}} = 0A$)	24
4.2.4	Condition 4 ($V_{IN_{MAX}} = 72V$, $I_{LOAD_{MAX}} = 15A$)	26
5.	Validation Across Datasheet Corners	28
6.	Additional TINA Test-benches	29
6.1	UVLO	29
6.2	Line Transient	31
6.3	Load Transient	34
6.4	Oscillator Test	37
6.5	Steady State Analysis	40
6.6	Output Shutdown: CS	42

6.7	Output Shutdown: SS/DISB.....	45
6.8	Output Shutdown: REF.....	48
6.9	Error Amplifier	51
6.10	Adaptive Delay Set	53
6.11	Delay Programming	55
6.12	Output Source Capacity	58
6.13	Output Sink Capacity	60
7.	Encrypted Model Validation.....	62
7.1	Transient Analysis.....	62
7.2	Average Analysis	63
8	Published Test-bench Reference Schematic	64
8.1	Transient Analysis.....	64
8.2	Average Analysis	65

1. Model Modification

No model modifications.

2. Analysis Parameters

2.1. PSPICE

START UP
.OPTIONS ABSTOL = 1n
.OPTIONS CHGTOL = 0.01p
.OPTIONS ITL1 = 150
.OPTIONS ITL2 = 20
.OPTIONS ITL4 = 400
.OPTIONS RELTOL = 0.01
.OPTIONS VNTOL = 1u
Maximum step size = 4ns

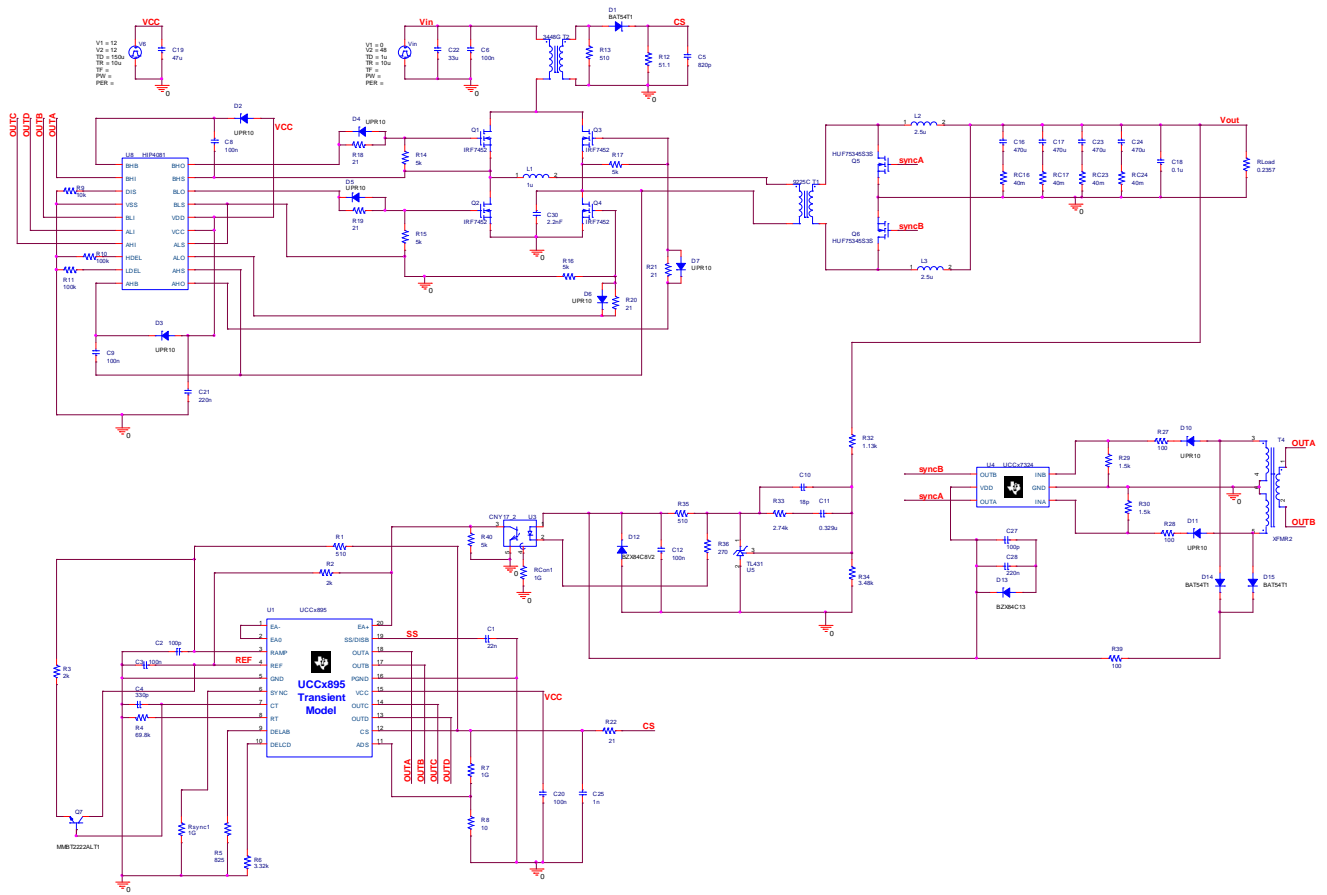
2.2. TINA

START UP
.OPTIONS ABSTOL = 1n
.OPTIONS CHGTOL = 10f
.OPTIONS ITL1 = 1000
.OPTIONS ITL2 = 40
.OPTIONS ITL4 = 20
.OPTIONS RELTOL = 10m
.OPTIONS VNTOL = 1u
TR maximum step size = 4ns

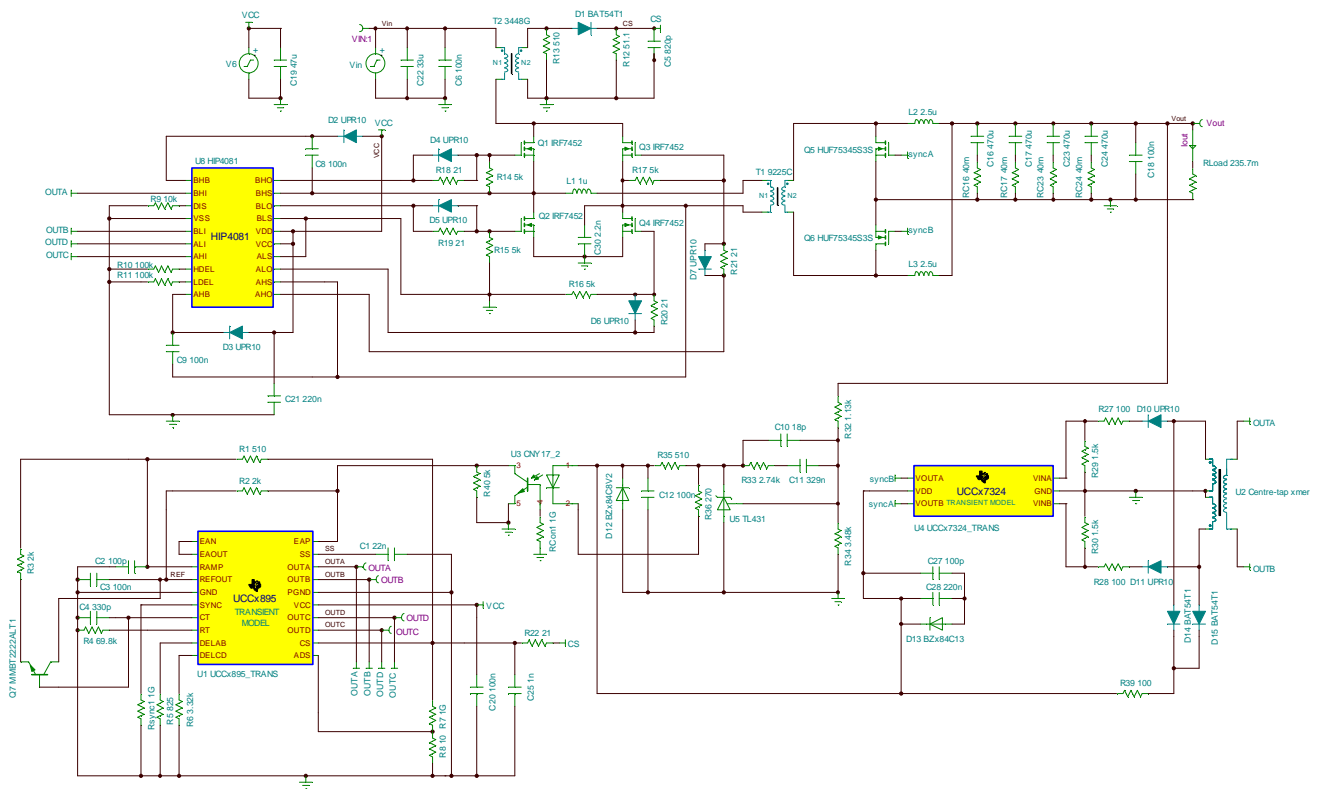
3. TINA schematic v/s published (STARTUP) PSPICE schematic

3.1. Transient Analysis

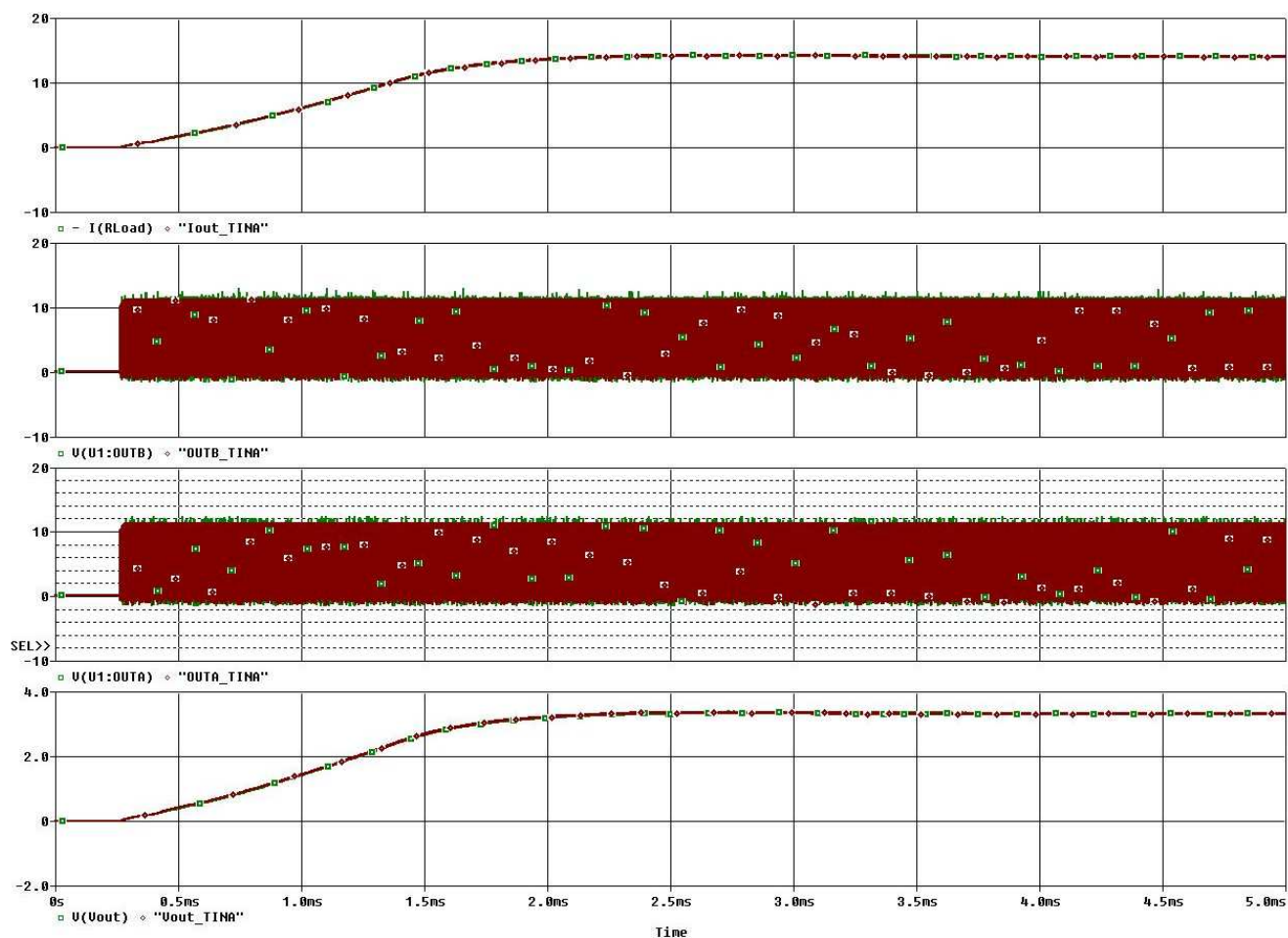
PSPICE Schematic:



TINA Schematic:



Overlaid Results:



Note: In the report TINA waveforms are with suffix “_TINA”. PSPICE waveforms do not have any suffix.

Tabulation of Results:

PARAMETER	PSPICE	TINA	EVM/DATASHEET	UNIT
VOUT*	3.316	3.315	3.3	V
V_{RIPPLE} !	54.51	49.244	-	mV
IOUT*	14.069	14.062	14	A
Switching Frequency	375.79	373.19	400	kHz

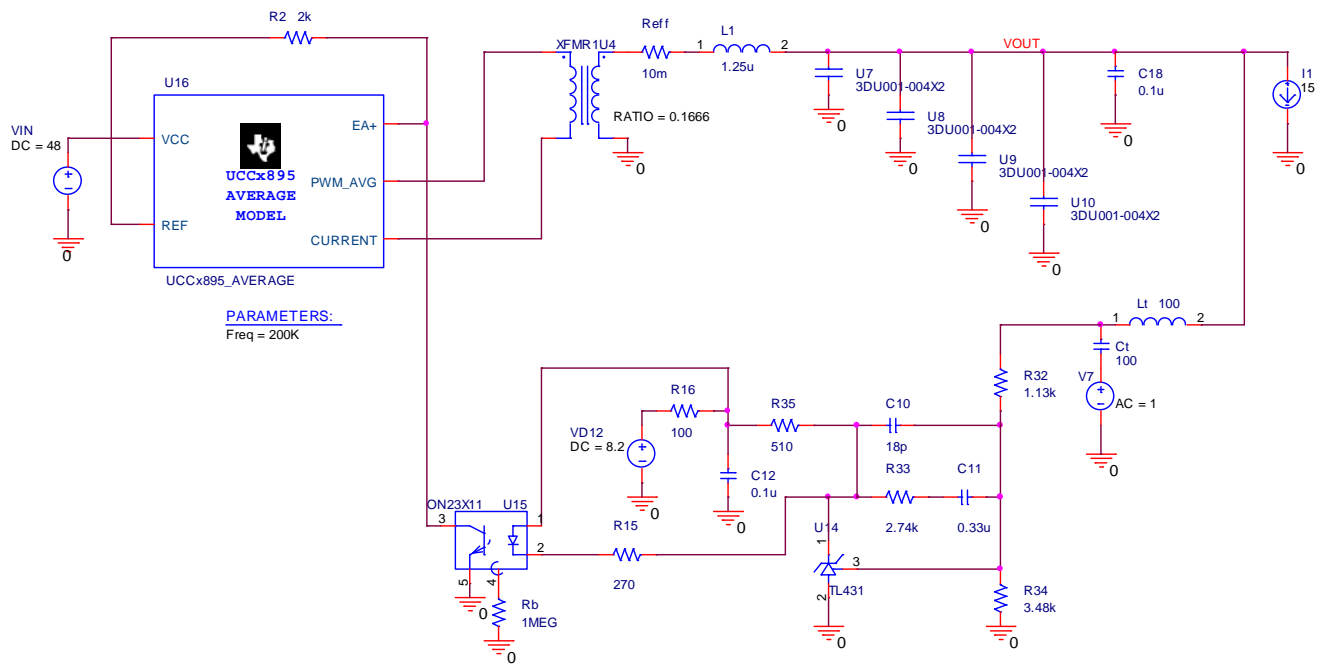
* VOUT and IOUT values are calculated as average over steady state range.

! Ripple values are calculated as peak to peak over steady state range.

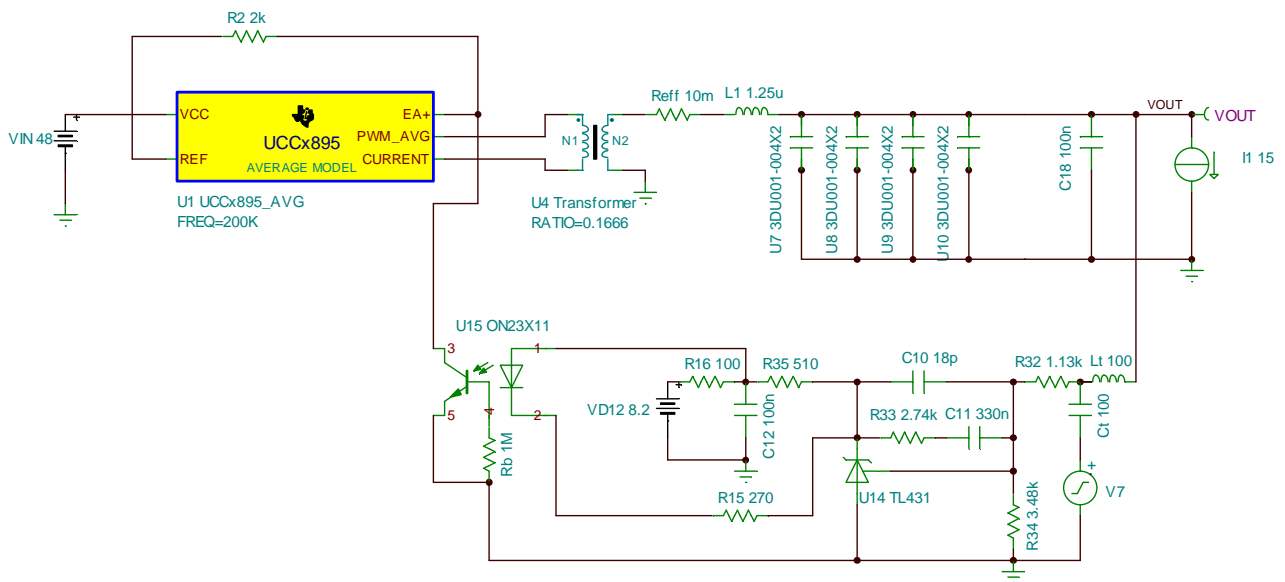
Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

3.2.Average Analysis

PSPICE Schematic:



TINA Schematic:



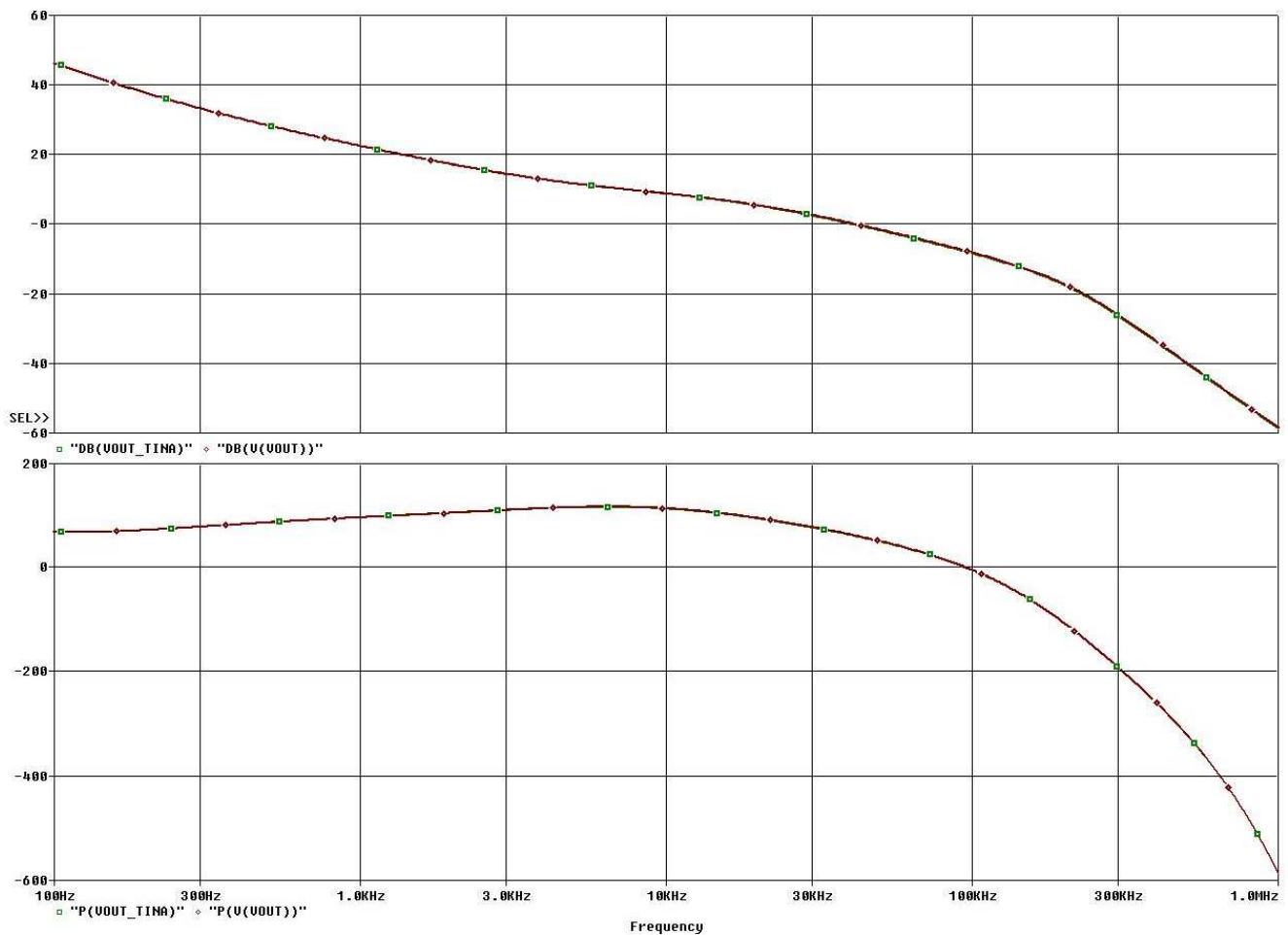
Description:

1. The AC Response for this model has been tested between an input voltage range of 36V - 72V and between an output current ranging from 100mA to 15A.
2. The output inductor used is 1.25uH instead of 2.5uH since the schematic shown here consists of only one side of the output stage.
3. PWM_AVG is not an actual pin on the IC but it represents the "Average PWM" signal used to control the MOSFET's in the bridge.
4. Similarly, CURRENT is not an actual pin on the IC but it represents the "Average Current" flowing through the MOSFET's.

Test Conditions and Additional Analysis Options (if any):

1. VIN = 48V
2. ILOAD = 15A constant current source

Overlaid Results:



Tabulation of Results:

PARAMETER	PSPICE	TINA	UNIT
Gain at 100Hz	46.07	46.07	dB
Zero Crossover Frequency	41.539	40.614	kHz
Phase at Zero Crossover	60.215	60.759	deg

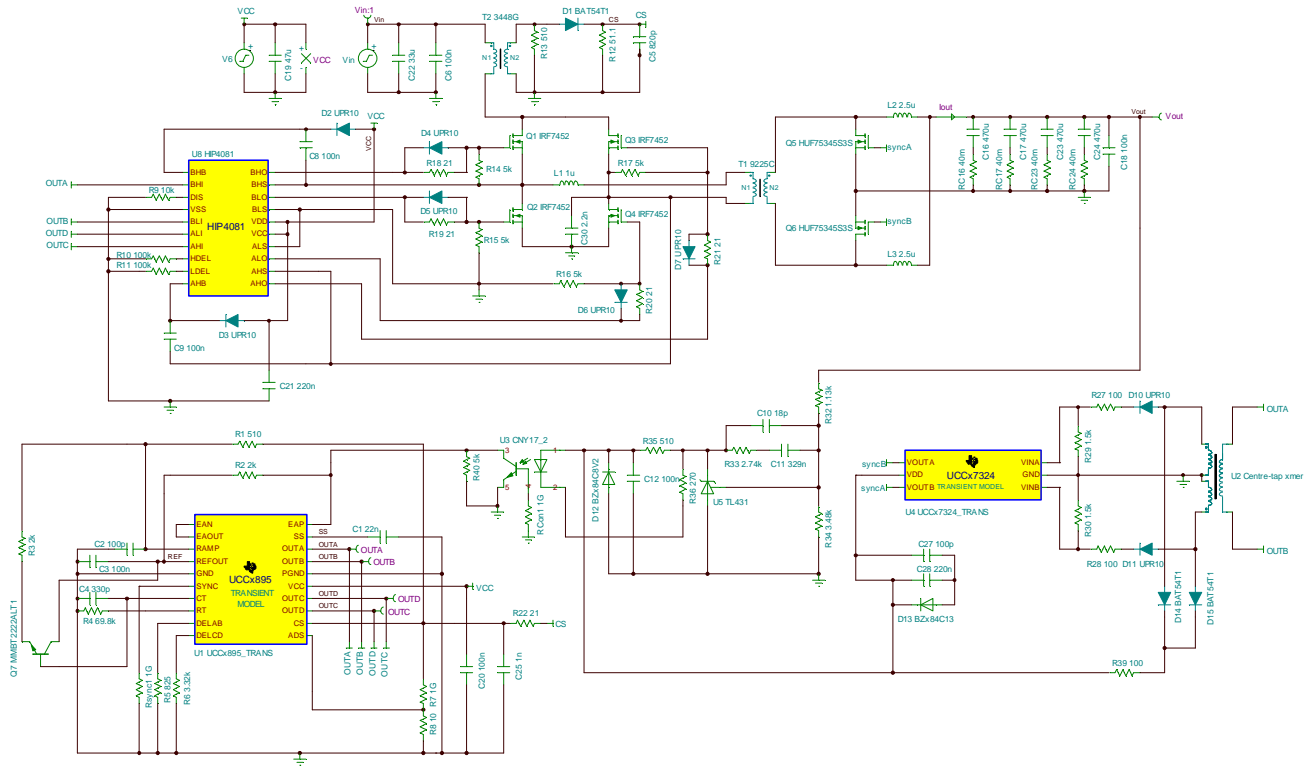
Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

4. Validation across EVM Corners

4.1 Transient Analysis

4.1.1 Condition 1 ($V_{IN_MIN} = 36V$, $I_{LOAD_MIN} = 0A$)

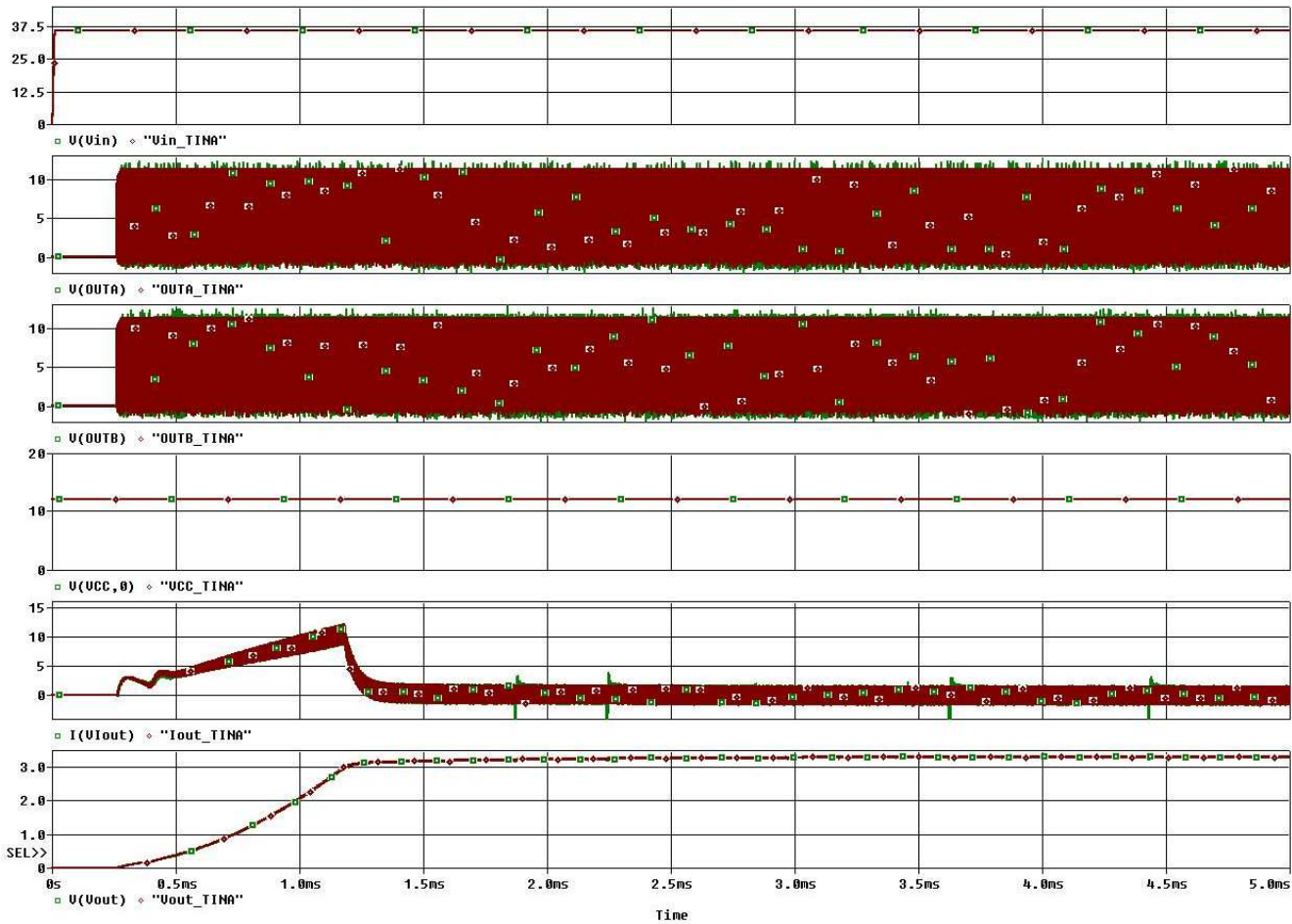
TINA Schematic:



Test Conditions and Additional Analysis Options (if any):

1. $VCC = 12V$
2. $VIN = 36V$
3. No load resistor connected at the output

Overlaid Results:



Tabulation of Results:

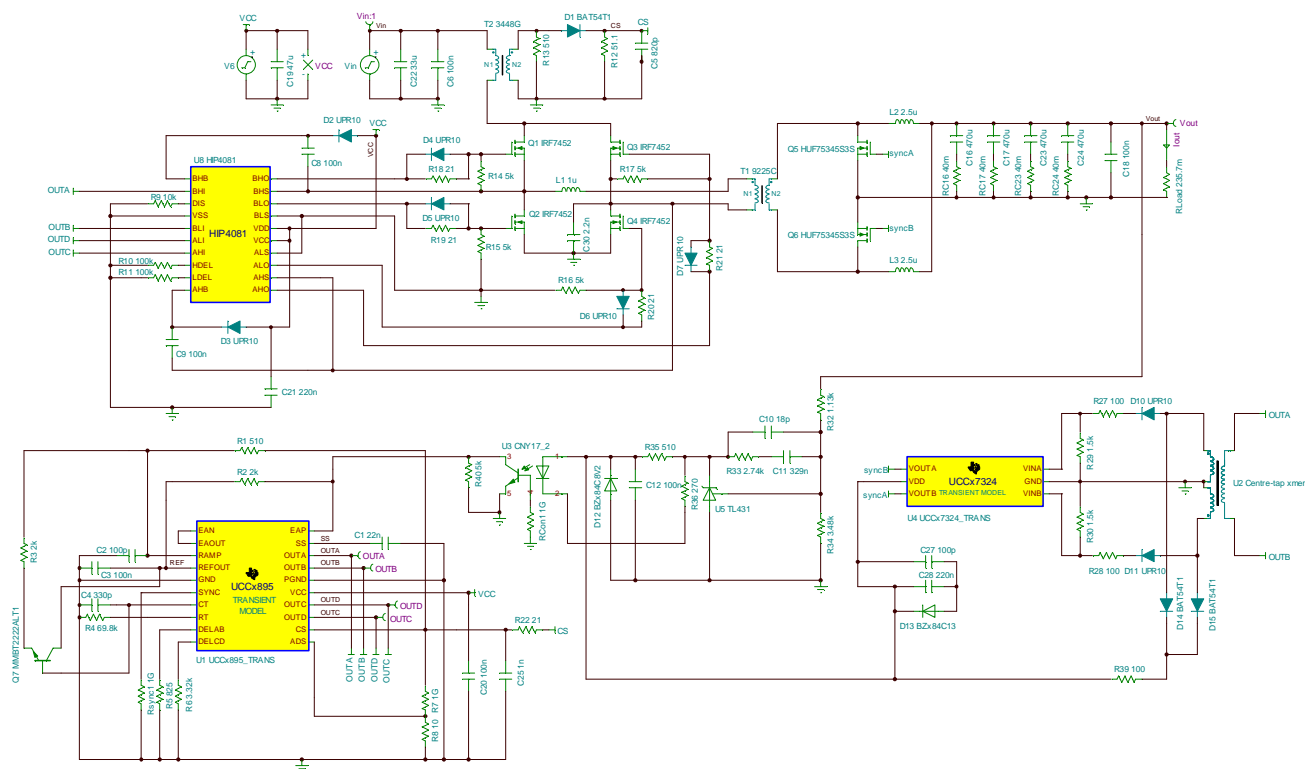
PARAMETER	PSPICE	TINA	EVM	UNIT
VOUT*	3.270	3.293	3.3	V
V _{ripple} !	29.463	29.924	-	mV
IOUT*	15.65	16.5	0	mA
Switching Frequency	180.22	182.17	200	kHz

* VOUT and IOUT values are calculated as average over steady state range.

! Ripple values are calculated as peak to peak over steady state range.

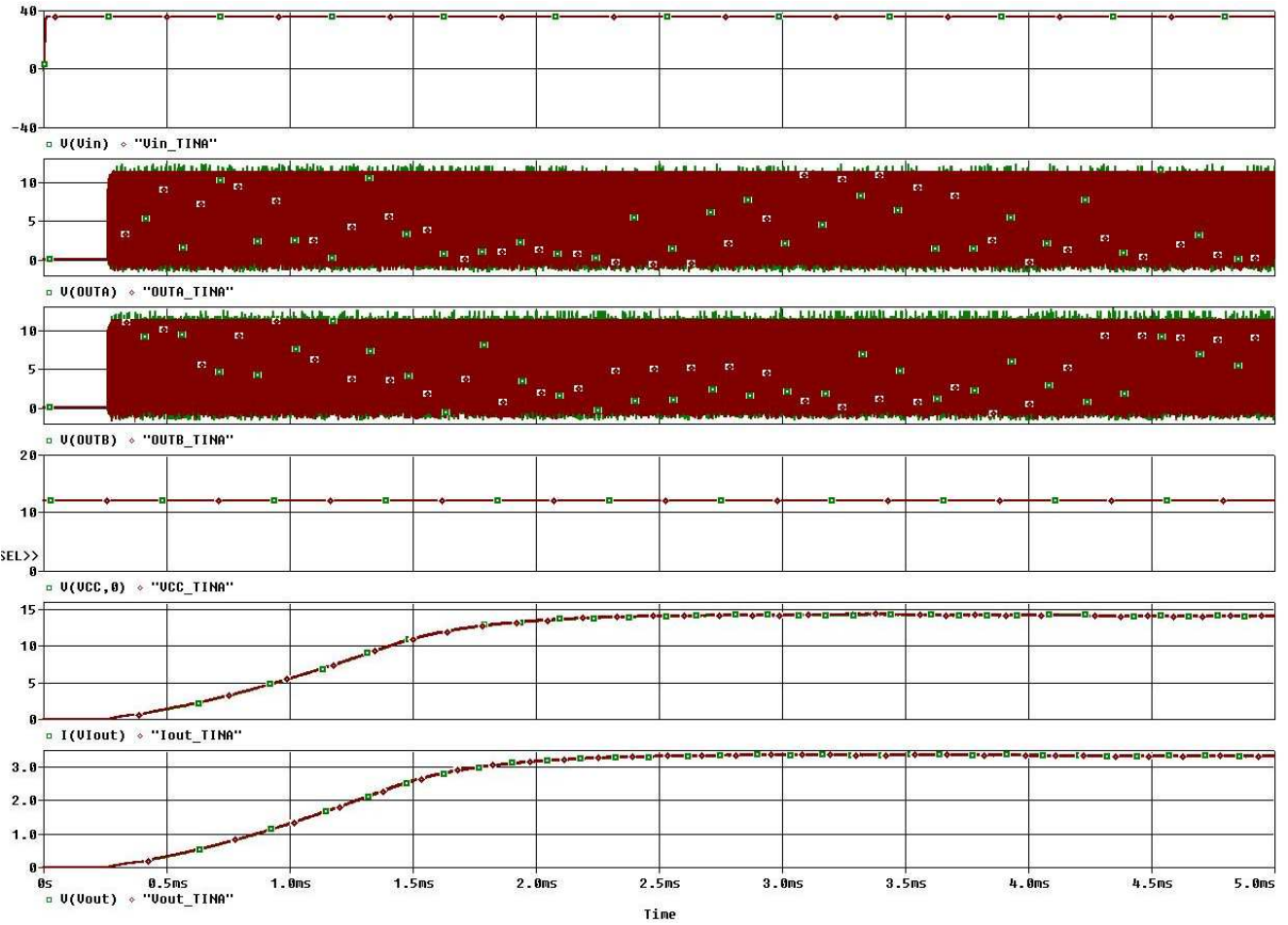
Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

TINA Schematic:



1. $V_{CC} = 12V$
2. $V_{IN} = 36V$
3. $R_{LOAD} = 235.7m\Omega$

Overlaid Result:



Tabulation of Results:

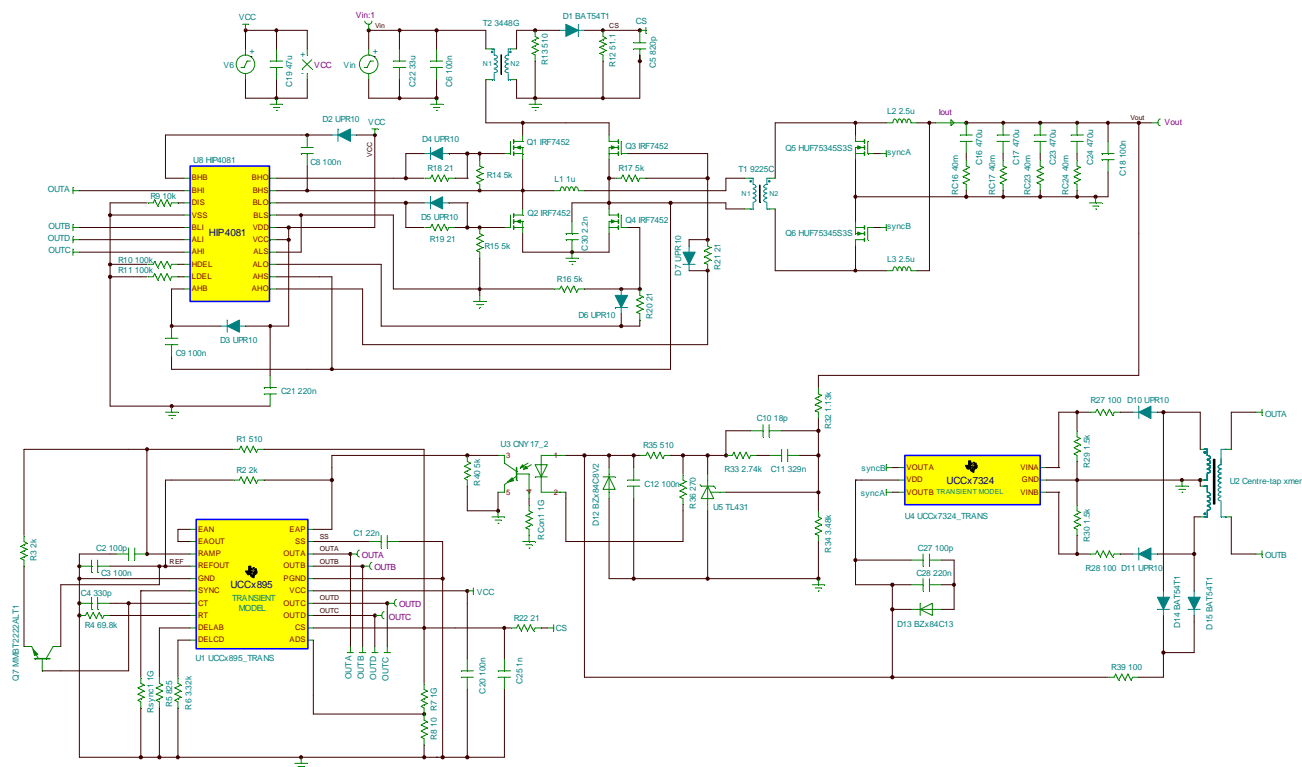
PARAMETER	PSPICE	TINA	EVM	UNIT
VOUT*	3.3449	3.347	3.3	V
V _{ripple} !	28.715	30.455	-	mV
IOUT*	14.191	14.200	14	A
Switching Frequency	182.87	182.98	200	kHz

* VOUT and IOUT values are calculated as average over steady state range.

! Ripple values are calculated as peak to peak over steady state range.

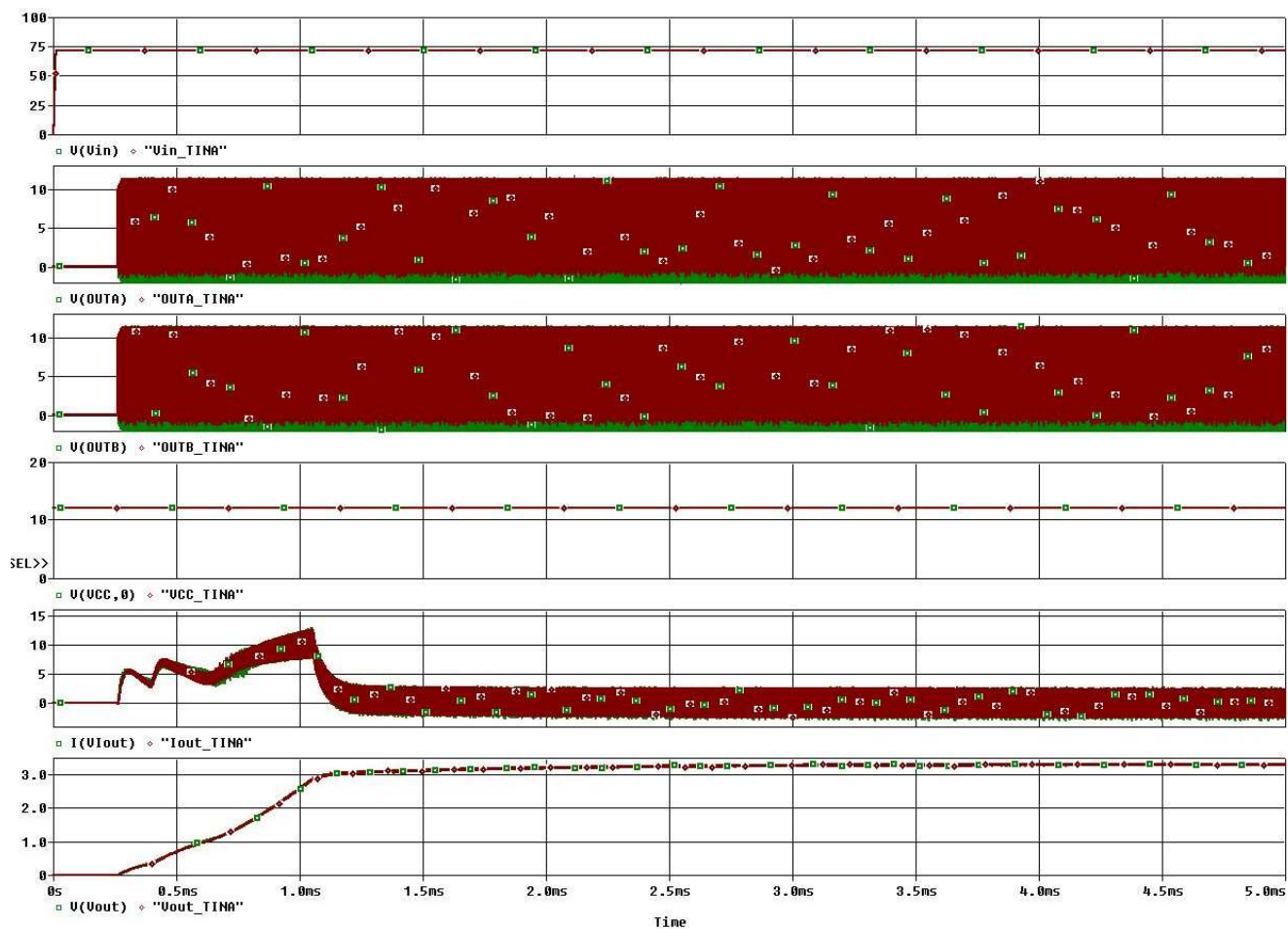
Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

TINA Schematic:



1. $V_{CC} = 12V$
2. $V_{IN} = 72V$
3. No load resistor connected at the output

Overlaid Results:



Tabulation of Results:

PARAMETER	PSPICE	TINA	EVM	UNIT
VOUT*	3.287	3.288	3.3	V
V _{RIPPLE} !	48.056	48.754	-	mV
IOUT*	0.474	0.128	0	A
Switching Frequency	184.88	182.265	200	kHz

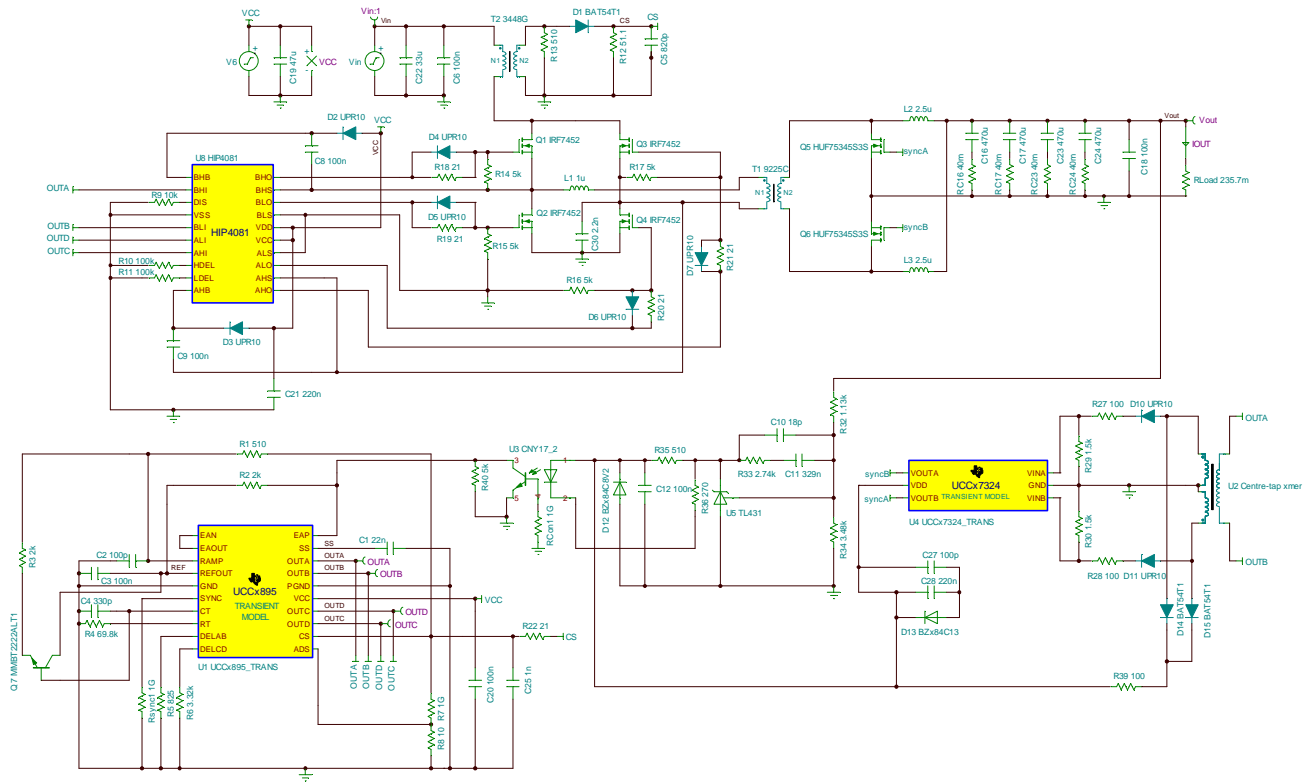
* VOUT and IOUT values are calculated as average over steady state range.

! Ripple values are calculated as peak to peak over steady state range.

Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

4.1.4 Condition 4 ($V_{IN_MAX}=72$, $I_{LOAD_MAX}=14A$)

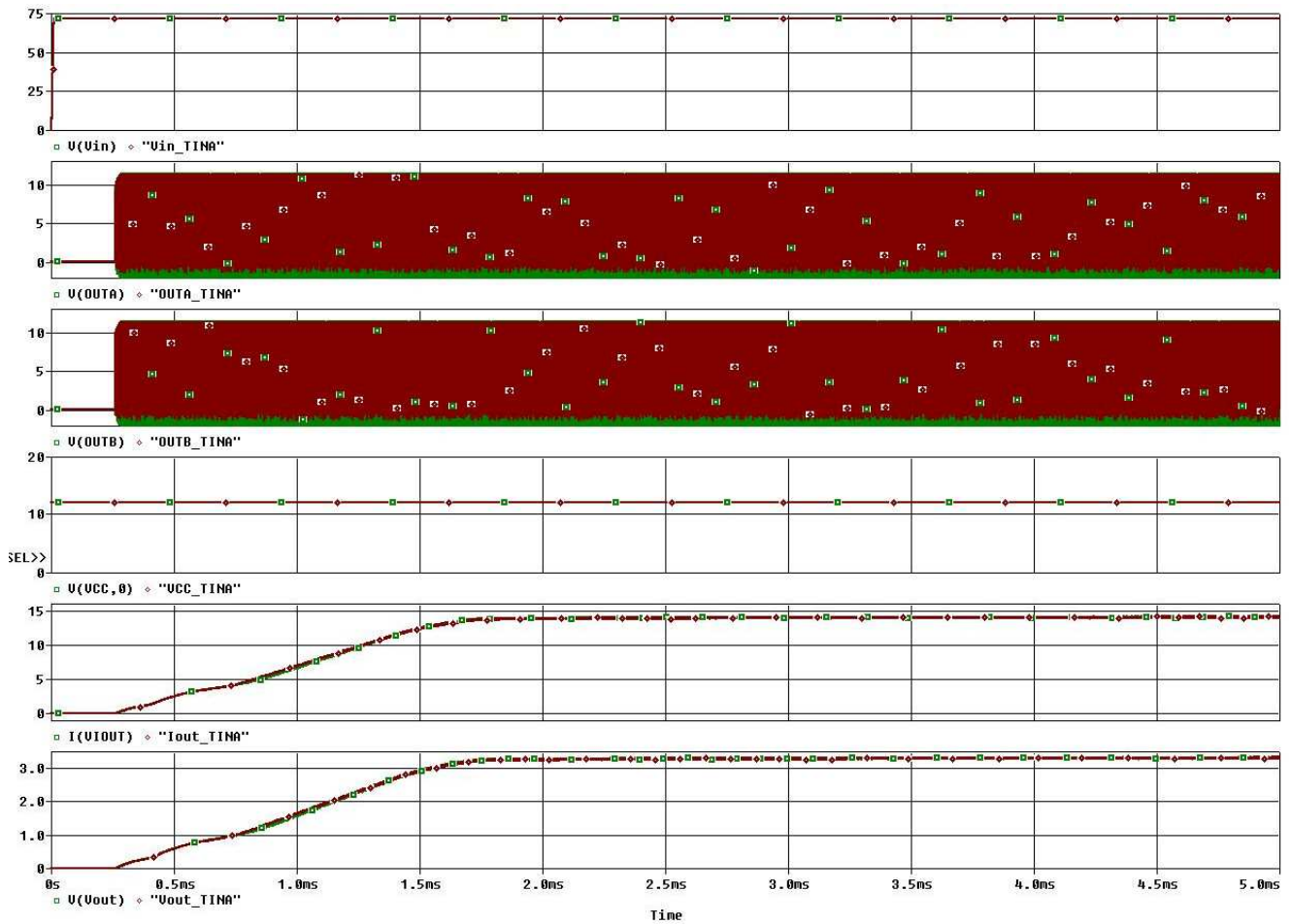
TINA Schematic:



Test Conditions and Additional Analysis Options (if any):

1. $VCC = 12V$
2. $VIN = 72V$
3. $R_{LOAD} = 235.7m\Omega$

Overlaid Graph:



Tabulation of Results:

PARAMETER	PSPICE	TINA	EVM	UNIT
VOUT*	3.2825	3.2819	3.3	V
V _{RIPPLE} !	48.507	50.710	-	mV
IOUT*	13.926	13.924	14	A
Switching Frequency	179.80	182.79	200	kHz

* VOUT and IOUT values are calculated as average over steady state range.

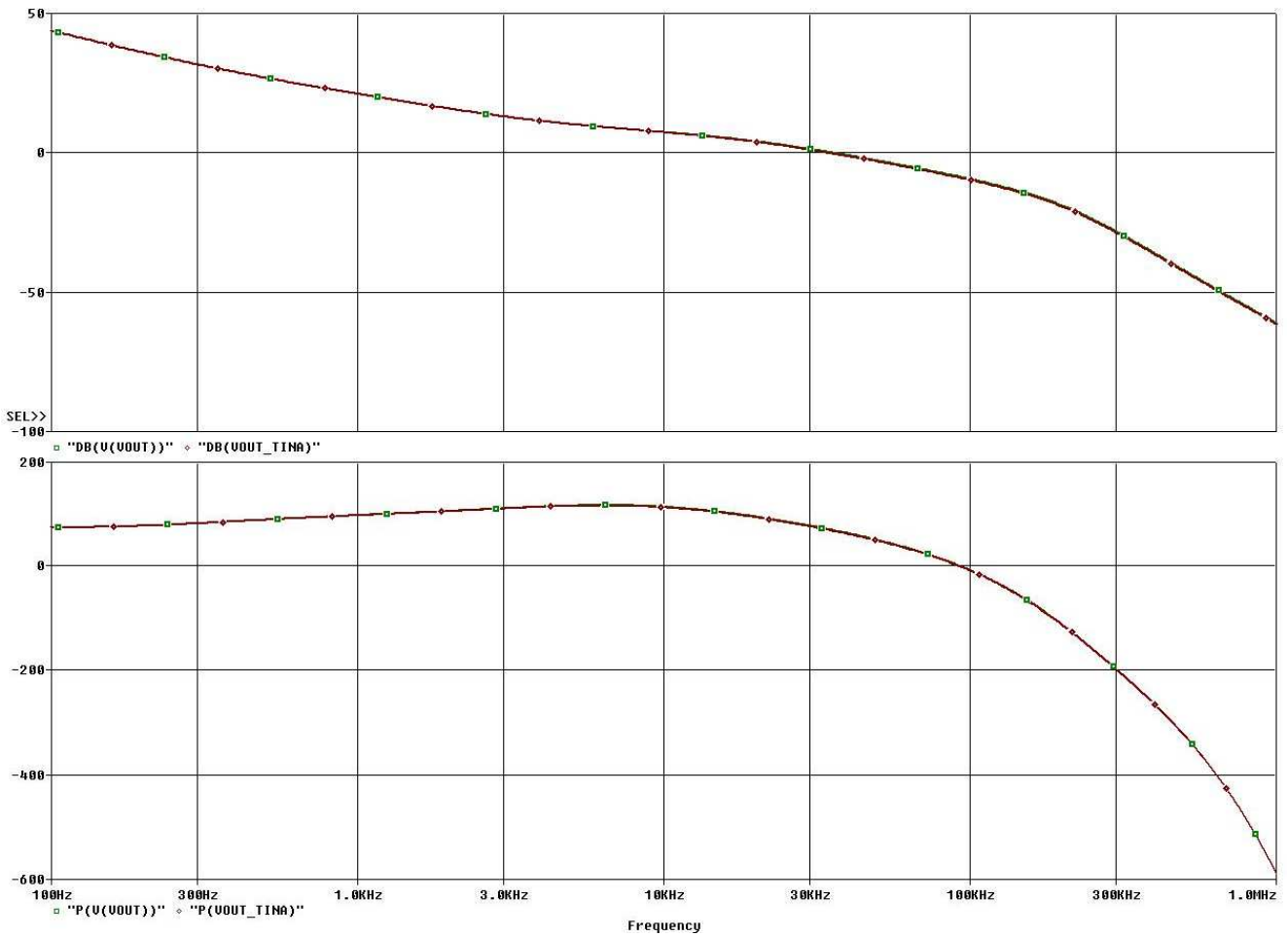
! Ripple values are calculated as peak to peak over steady state range.

Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

4.2.1 Condition 1 ($V_{IN_MIN} = 36V$, $I_{LOAD_MIN} = 0A$)

1. $V_{CC} = 12V$
2. $V_{IN} = 36V$
3. No load resistor connected at the output

Overlaid Results:



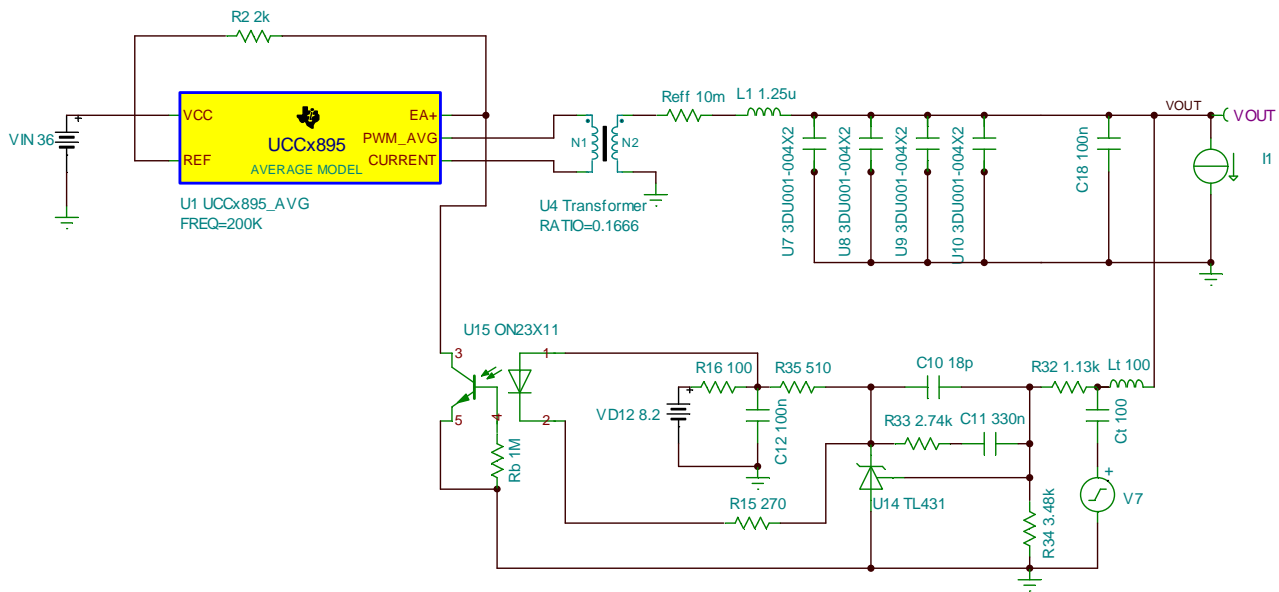
Tabulation of Results:

PARAMETER	PSPICE	TINA	UNIT
Gain at 100Hz	43.701	43.704	dB
Zero Crossover Frequency	35.469	34.332	kHz
Phase at Zero Crossover	68.205	68.799	deg

Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

4.2.2 Condition 2 ($V_{IN_MIN} = 36V$, $I_{LOAD_MAX} = 15A$)

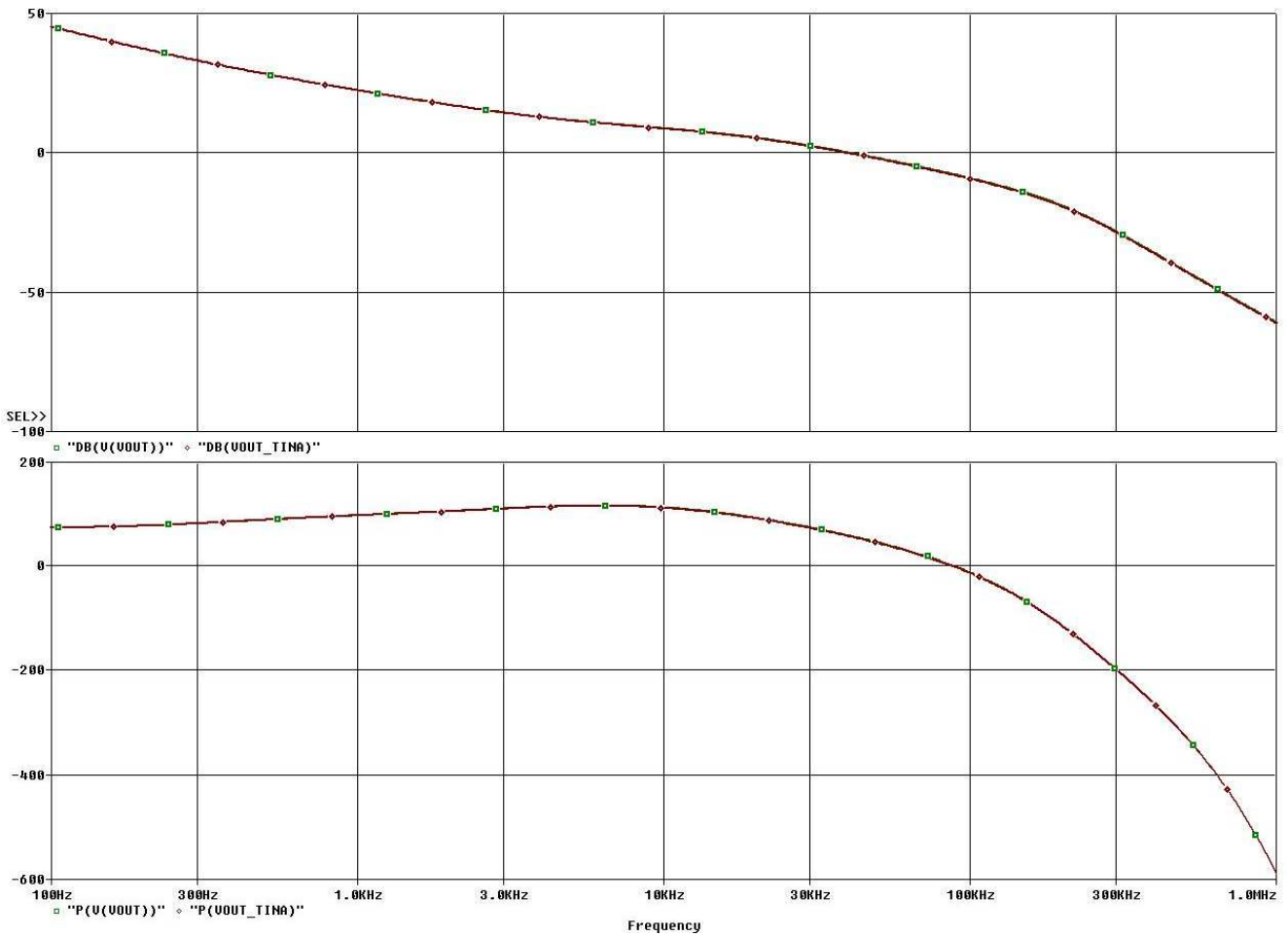
TINA Schematic:



Test Conditions and Additional Analysis Options (if any):

1. $V_{CC} = 12V$
2. $V_{IN} = 36V$
3. $R_{LOAD} = 235.7m\Omega$

Overlaid Results:

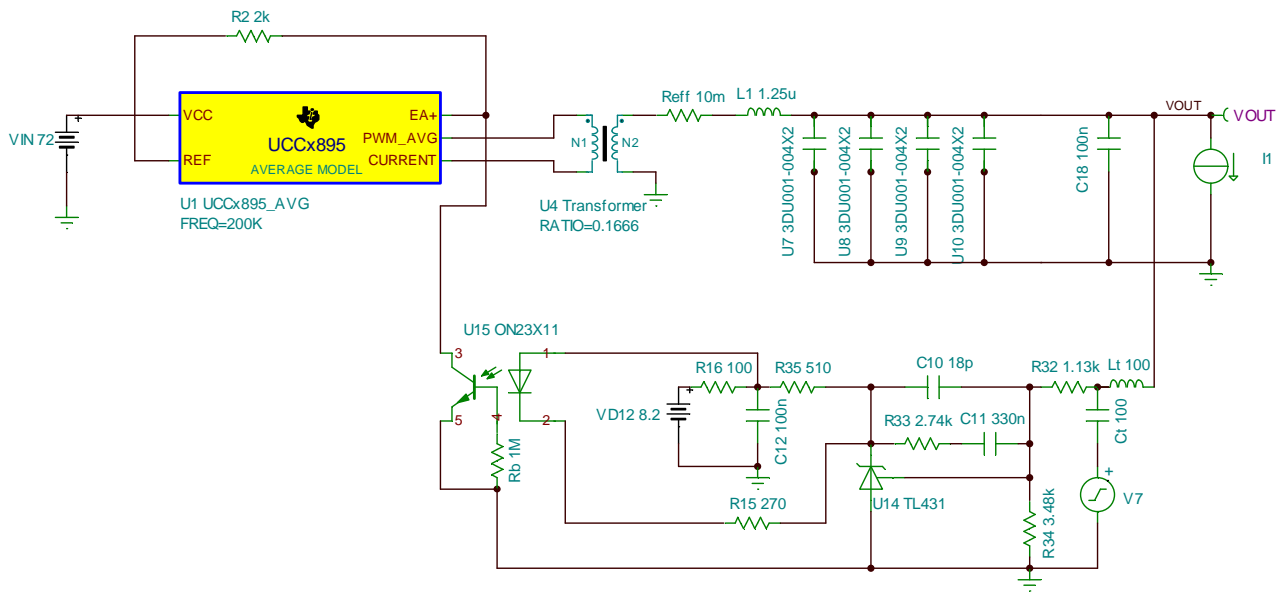


Tabulation of Results:

PARAMETER	PSPICE	TINA	UNIT
Gain at 100Hz	45.057	45.057	dB
Zero Crossover Frequency	40.289	39.45	kHz
Phase at Zero Crossover	57.363	57.894	deg

Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

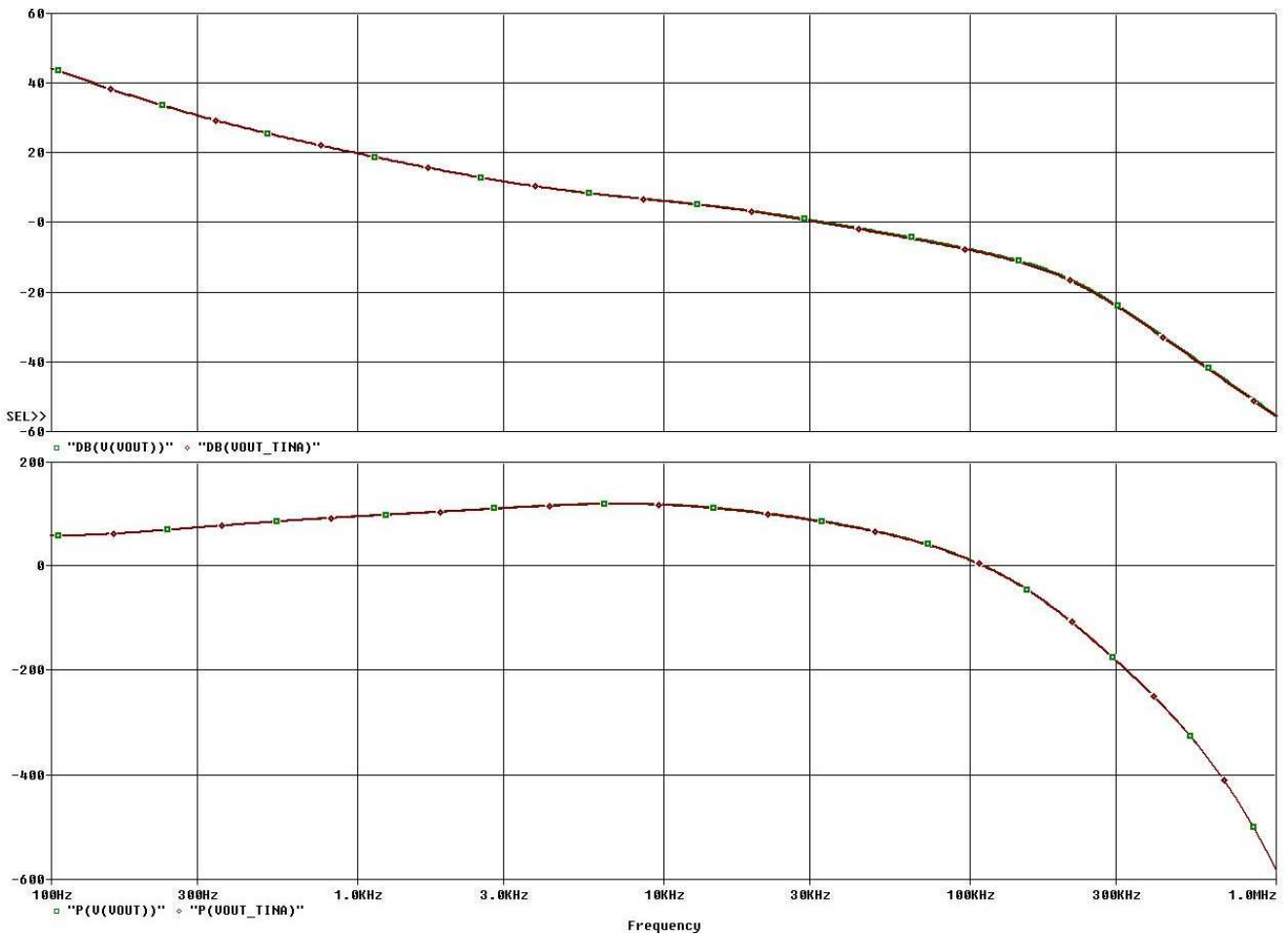
TINA Schematic:



Test Conditions and Additional Analysis Options (if any):

1. $V_{CC} = 12V$
2. $V_{IN} = 72V$
3. No load resistor connected at the output

Overlaid Results:



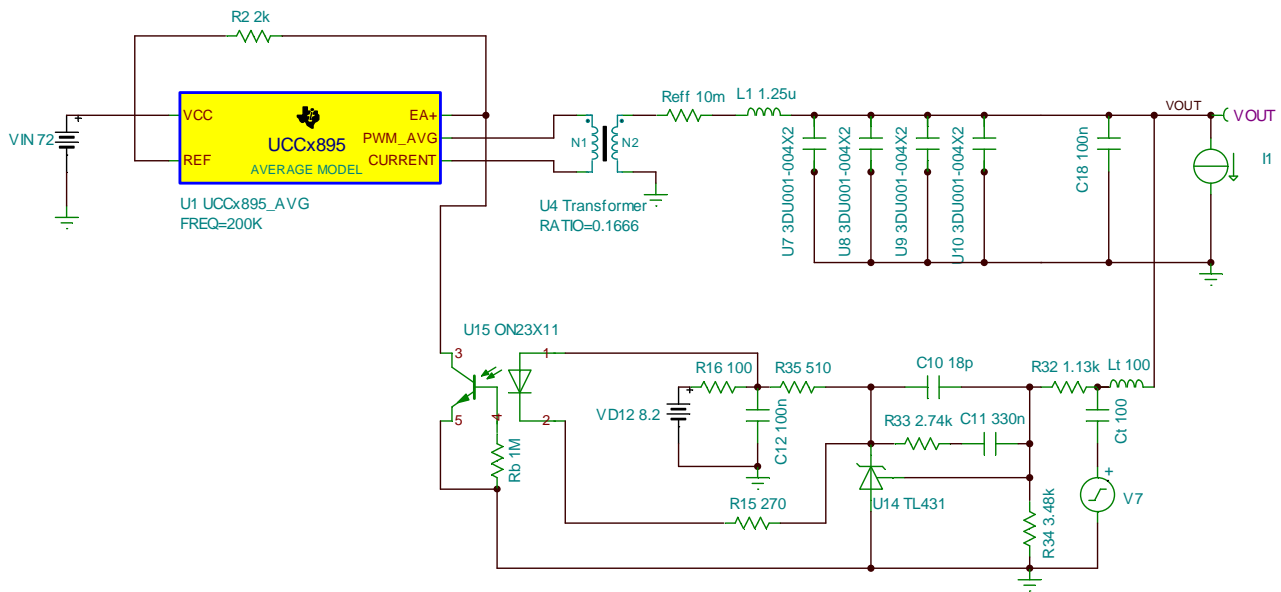
Tabulation of Results:

PARAMETER	PSPICE	TINA	UNIT
Gain at 100Hz	44.226	44.226	dB
Zero Crossover Frequency	33.621	32.207	kHz
Phase at Zero Crossover	84.061	84.551	deg

Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

4.2.4 Condition 4 ($V_{IN_MAX} = 72V$, $I_{LOAD_MAX} = 15A$)

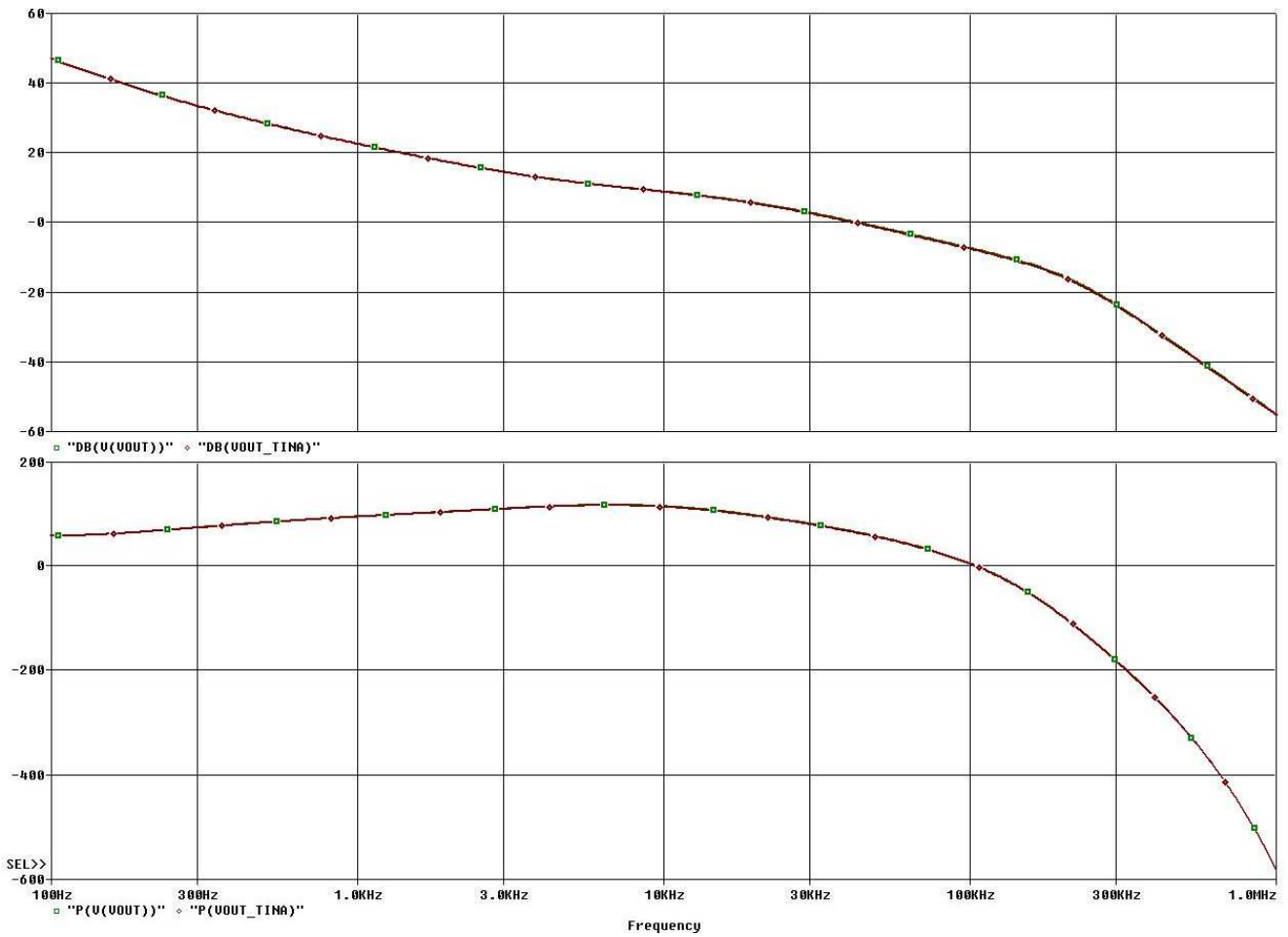
TINA Schematic:



Test Conditions and Additional Analysis Options (if any):

1. $V_{CC} = 12V$
2. $V_{IN} = 72V$
3. $R_{LOAD} = 235.7m\Omega$

Overlaid Results:



Tabulation of Results:

PARAMETER	PSPICE	TINA	UNIT
Gain at 100Hz	46.987	46.07	dB
Zero Crossover Frequency	42.633	41.621	kHz
Phase at Zero Crossover	63.773	64.303	deg

Conclusion: The simulation results of TINA and PSPICE are matching within acceptable limits.

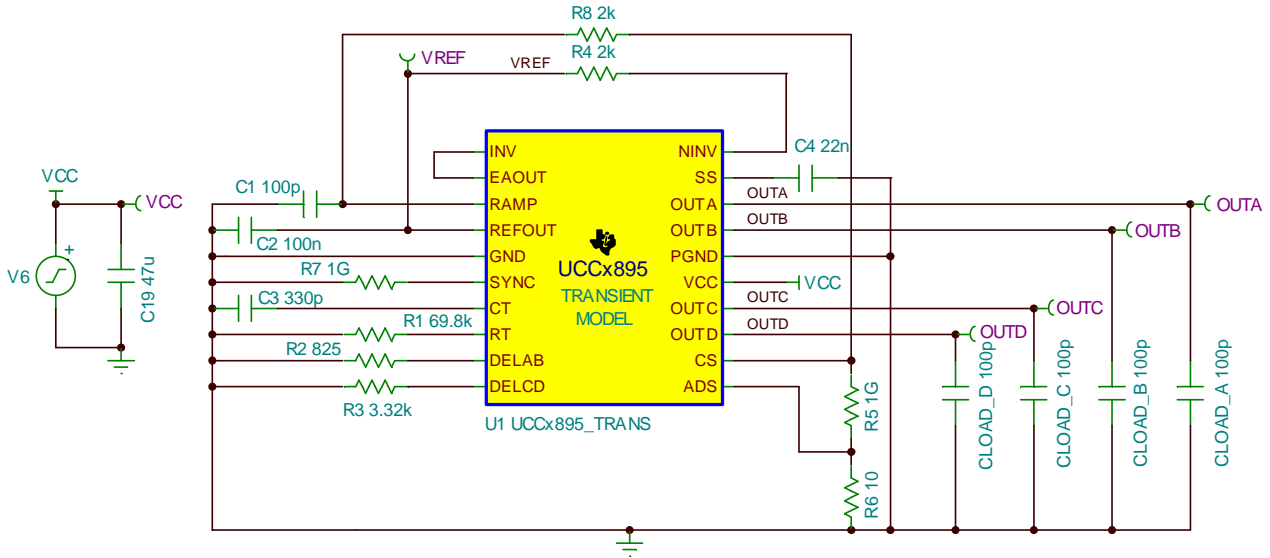
5. Validation Across Datasheet Corners

CONDITION	CORNERS	STATUS
1	$VCC_{MIN} = 10V$	Working
2	$VCC_{MAX} = 16.5V$	Working
3	$R_{Tmin} = 40k\Omega$ $C_{Tmin} = 100pF$	Working
4	$R_{Tmin} = 40k\Omega$ $C_{Tmax} = 880pF$	Working
5	$R_{Tmax} = 120k\Omega$ $C_{Tmin} = 100pF$	Working
6	$R_{Tmax} = 120k\Omega$ $C_{Tmax} = 880pF$	Working

6. Additional TINA Test-benches

6.1 UVLO

TINA Schematic:



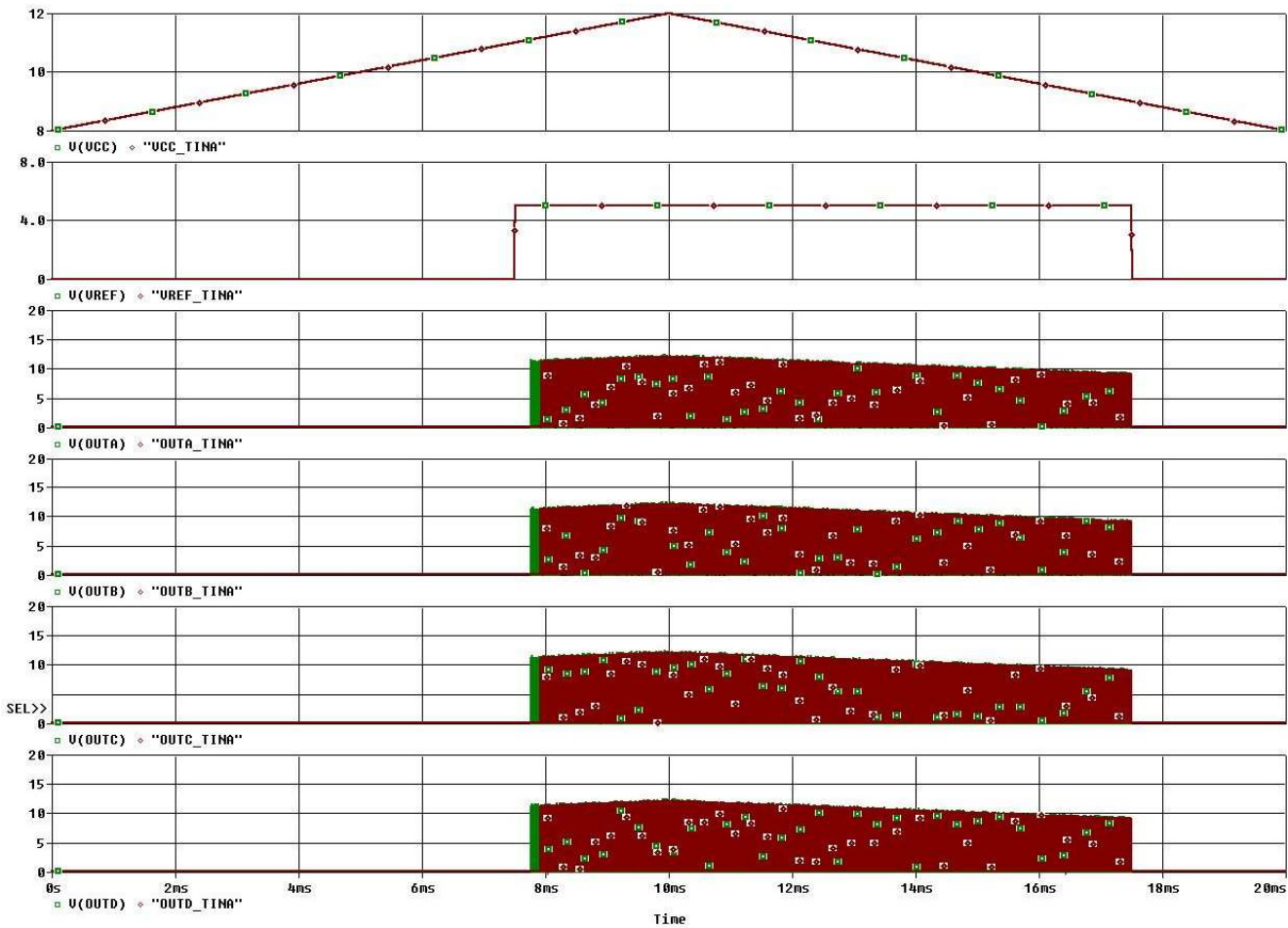
Description:

1. Above application circuit is developed to test the under voltage lockout (UVLO) functionality of the component macro model for VCC input.
2. The bias voltage VCC is ramped up slowly from 8V to 12V in 10ms and then ramped down back to 8V in next 10ms, since both the rising and falling lockout thresholds lay between this range only.
3. The VCC instant when VREF signal transitions from 0V to 5V is noted down as rising threshold and next VCC instant when VREF transitions from 5V back to 0V is noted down as falling threshold.

Test Conditions and Additional Analysis Options (if any):

1. VCC = 8V to 12V ramp in 10ms and 12V to 8V ramp in next 10ms
2. Capacitive load on all four outputs as 100pF.

Overlaid Results:



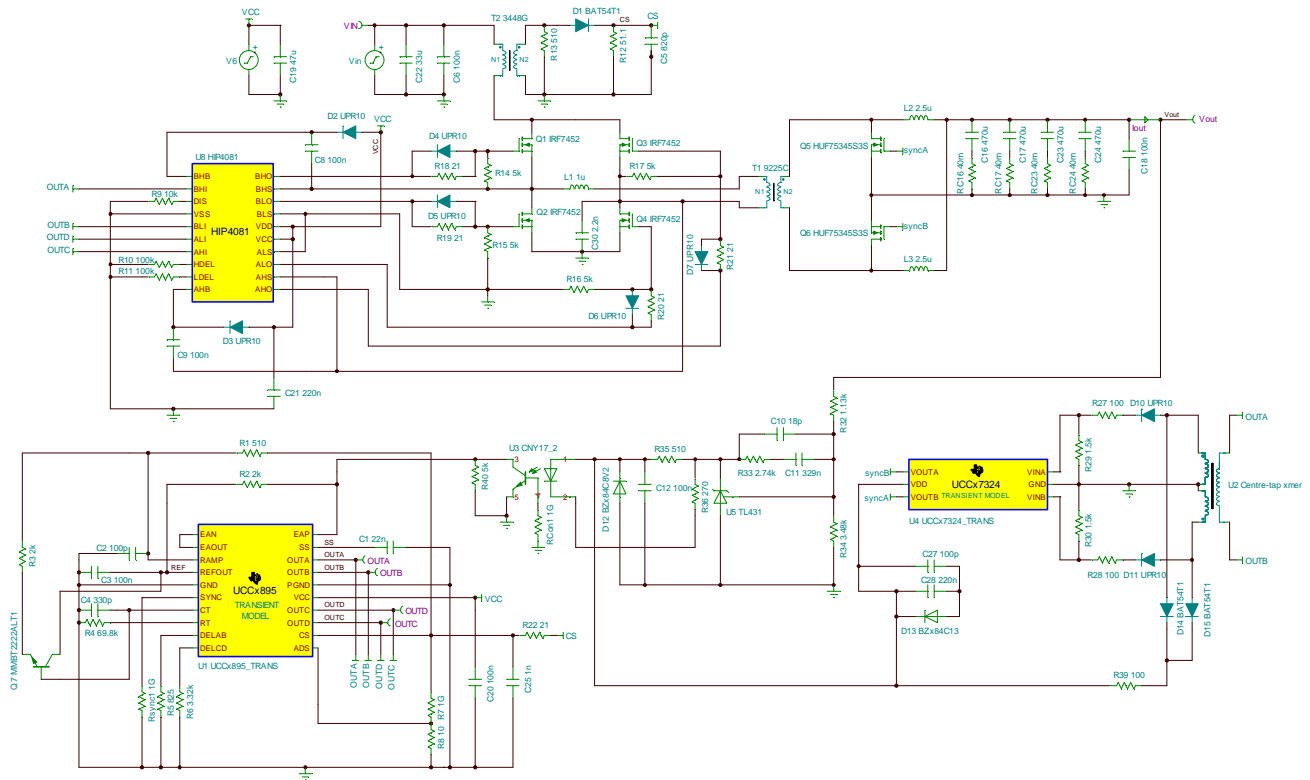
Tabulation of Results:

PARAMETER	DESCRIPTION	PSPICE	TINA	DATASHEET	UNIT
UVLO _(on)	Start-up voltage threshold	11.00	11.00	11	V
UVLO _(off)	Minimum operating voltage after start-up	9	9	9	V
UVLO _(hys)	Hysteresis	2	2	2	V

Conclusion: The simulation results of TINA and PSPICE are matching within the acceptable limits.

6.2 Line Transient

TINA Schematic:



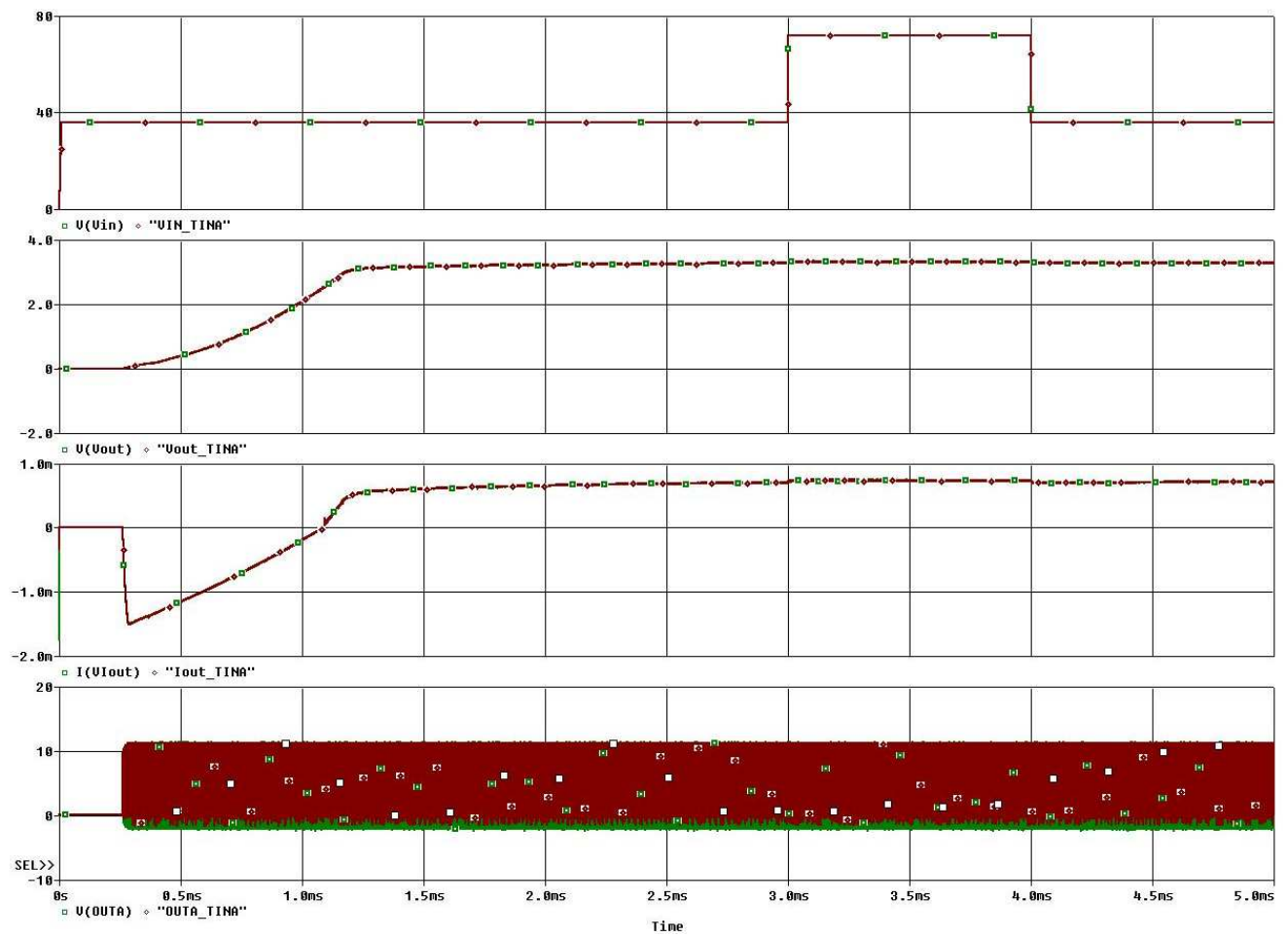
Description:

1. Above application circuit is developed to test the line transient response of the system as whole, when PWM controller is used as a part of it.
2. The application circuit is tested for line transient when it is configured for
 - 2.1. Minimum load current condition
 - 2.2. Maximum load current condition
3. The circuit is allowed to reach steady state for an input voltage of 36V and output of 1.8V and then a line transient of 1ms pulse width is applied at its input. Corresponding output variations are noted down.

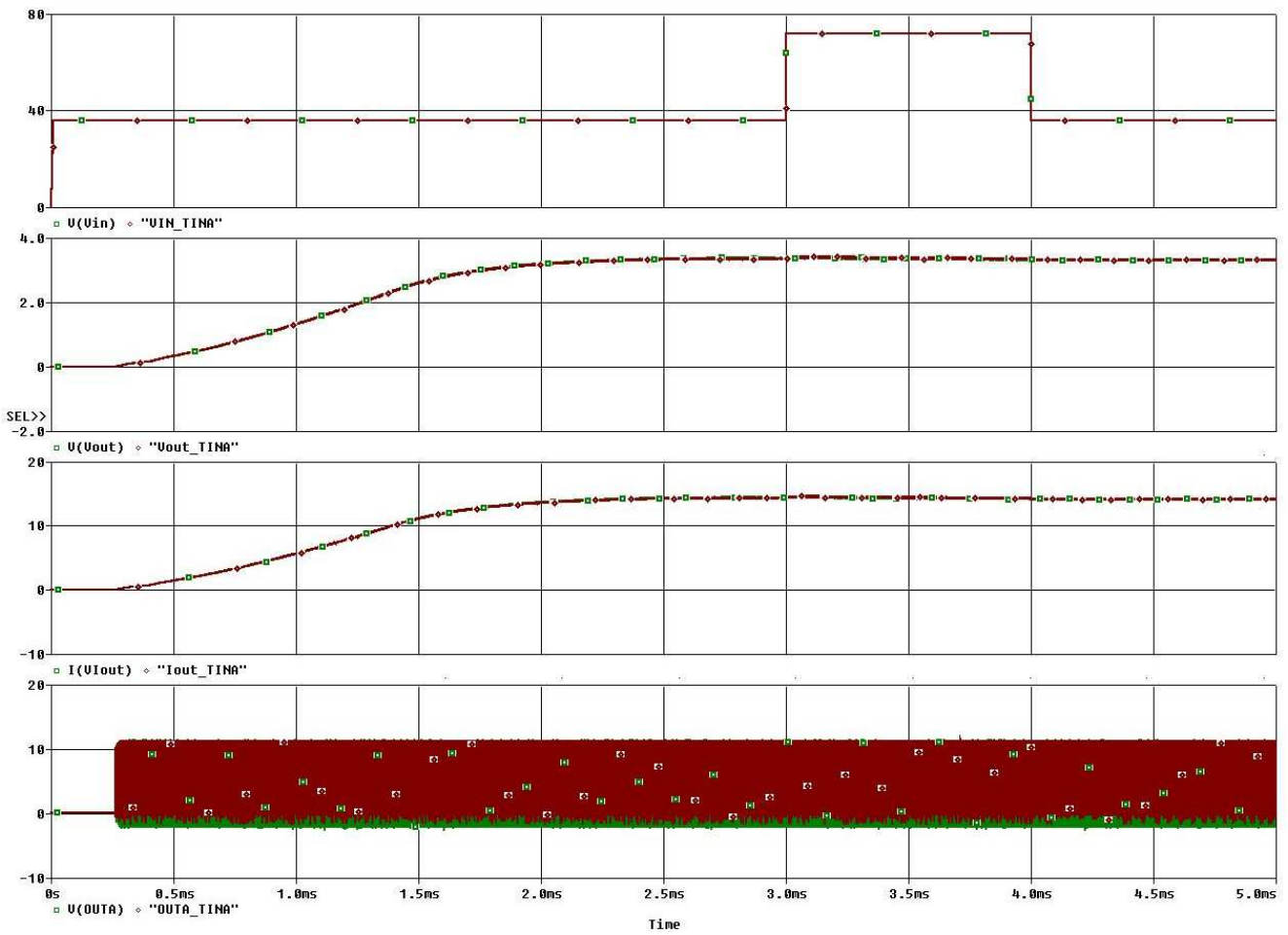
Test Conditions and Additional Analysis Options (if any):

1. VCC = 12V
2. CONDITION 1: IOU=0A
CONDITION 2: IOU= 14A
3. VIN = 36V constant input on top of which of 36V, 1ms pulse is applied after output reaches steady state.

Overlaid Results for test condition 1:



Overlaid Results for test condition 2:



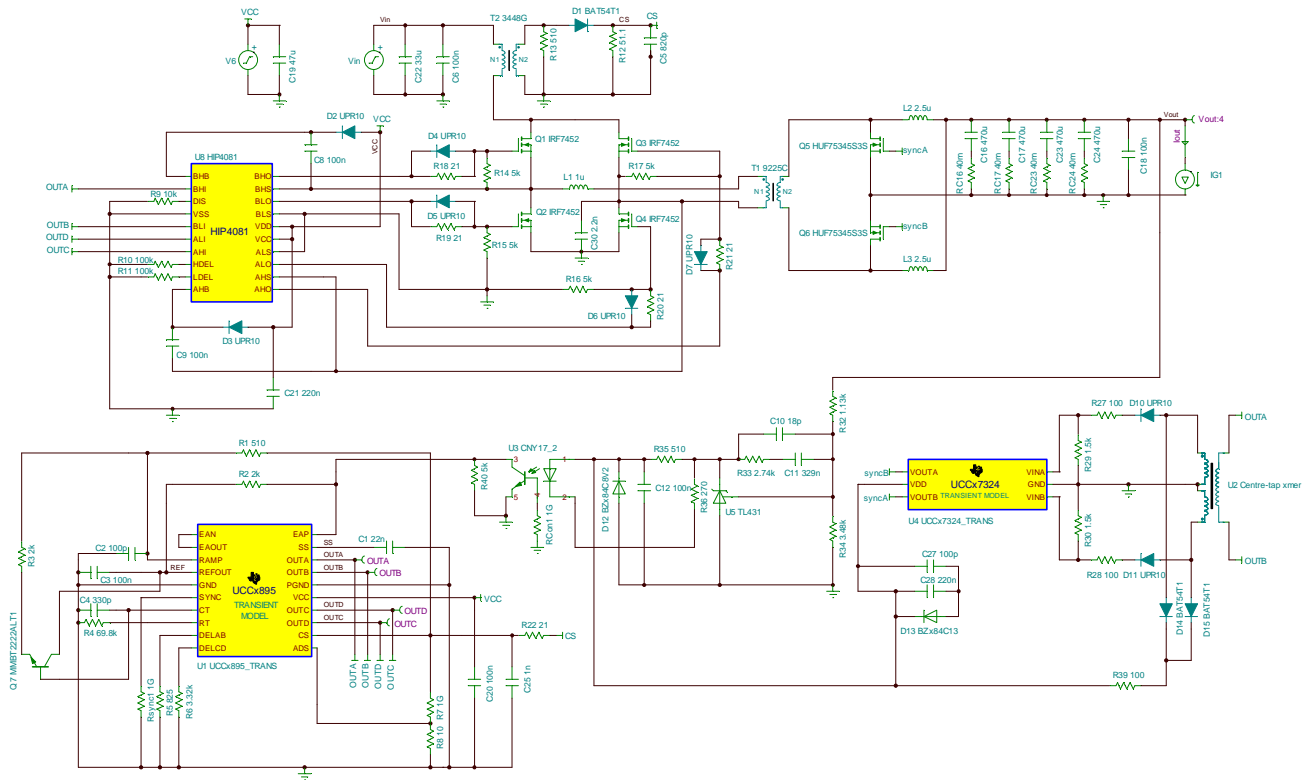
Tabulation of Results:

PARAMETER	PSPICE	TINA	UNIT
Average change in output voltage during VIN transition (@ILOAD=0A)	31.63	30.8	mV
Average change in output voltage during VIN transition (@ILOAD=14A)	52.17	58.83	mV

Conclusion: The simulation results of TINA and PSPICE are matching with each other. It is observed that even after transition in input occurs, the output shows slight increase in average value from steady state value and transient peak amplitudes are almost negligible for both conditions.

6.3 Load Transient

TINA Schematic:



Description:

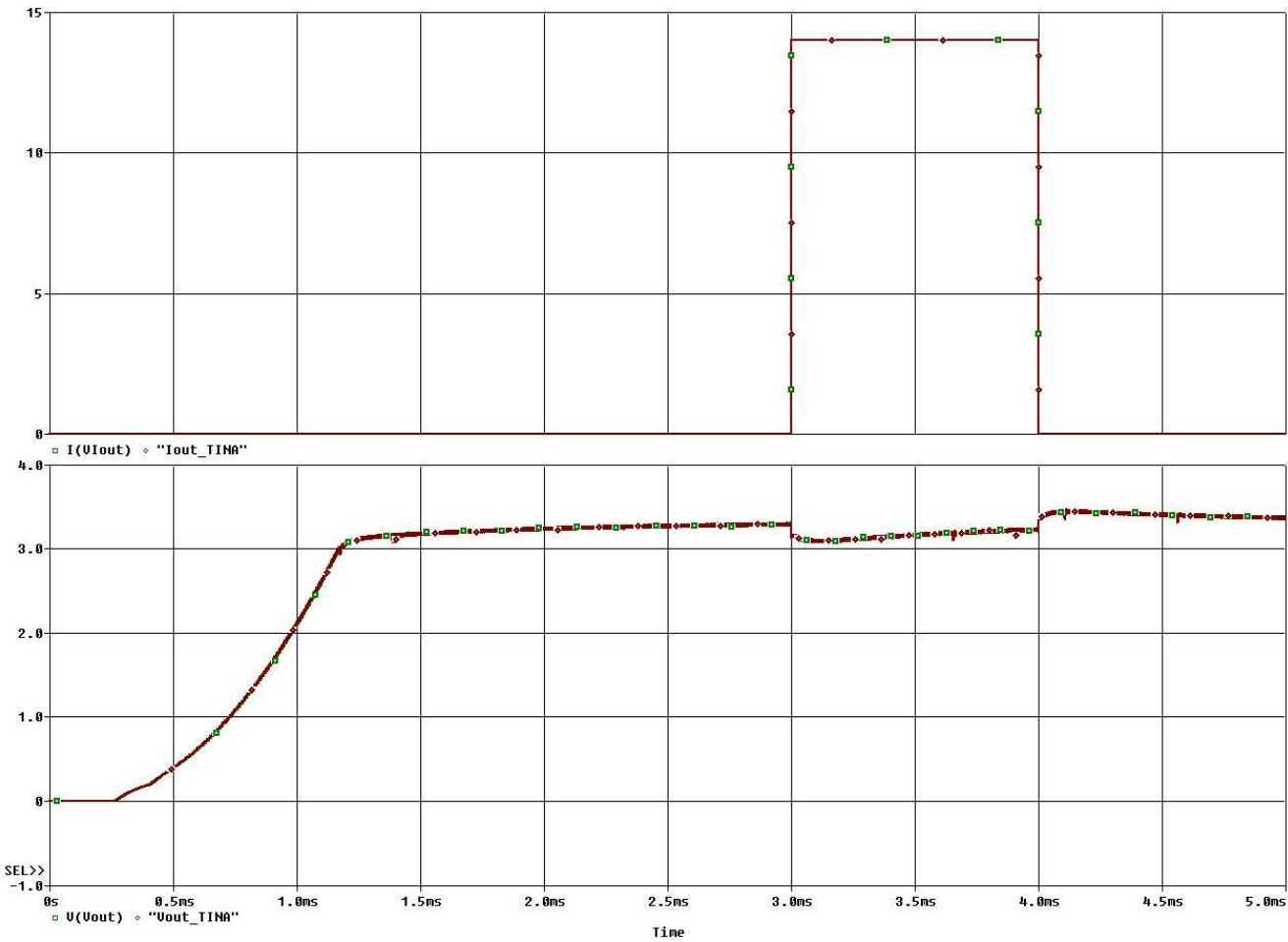
1. Above application circuit is developed to test the load transient response of the system as whole, when PWM controller is used as a part of it.
2. The application circuit is tested for line transient when it is configured for
2.1 Minimum input voltage condition
2.1 Maximum input voltage condition
3. The circuit is allowed to reach steady state for an output voltage of 1.8V and a load of 50uA and then a load transient of 1ms pulse width is applied at its input. Corresponding output voltage variations are noted down.

Test Conditions and Additional Analysis Options (if any):

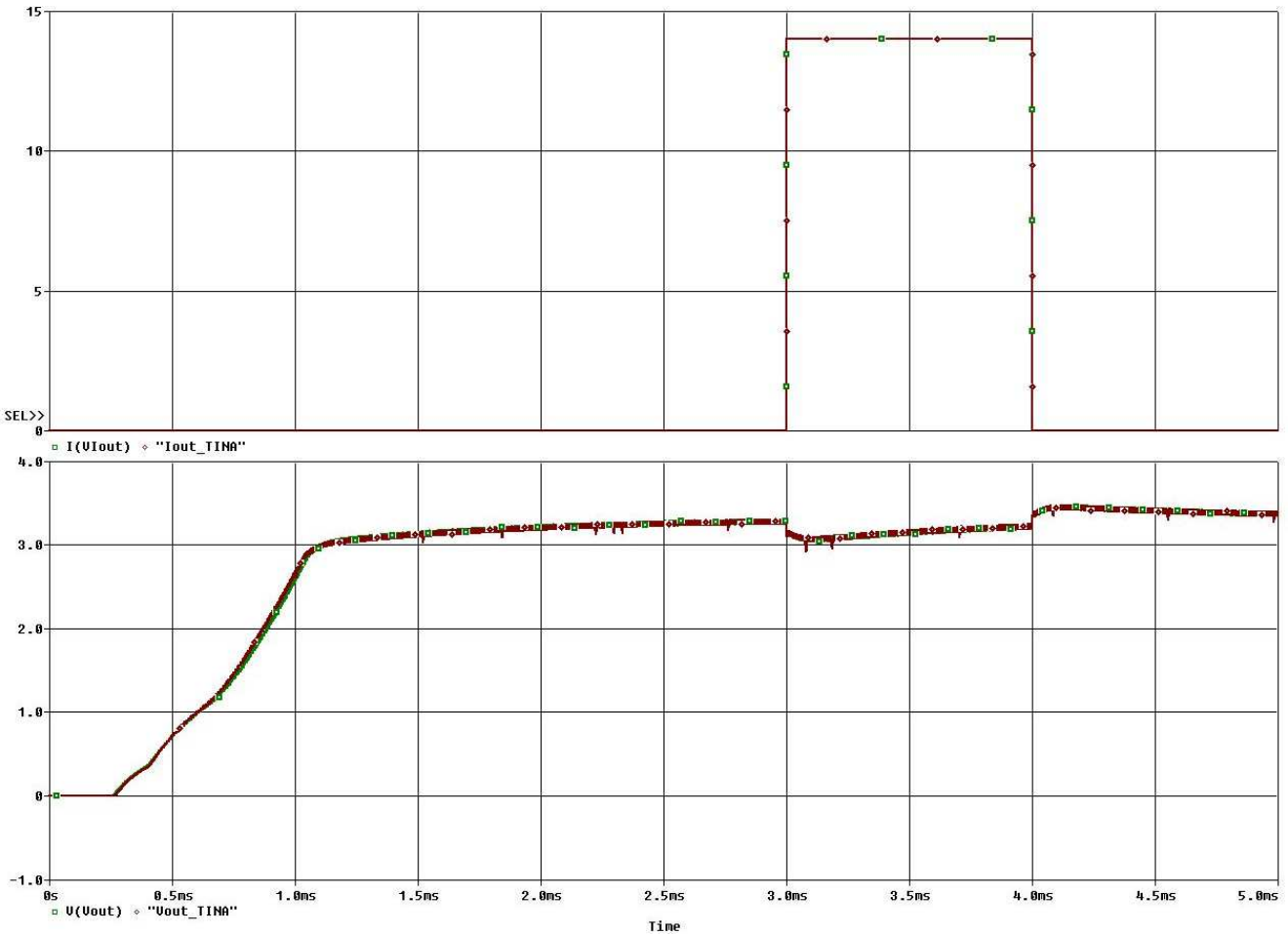
1. VCC=12V
2. CONDITION 1: VIN = 36V
 CONDITION 2: VIN = 72V
3. Iout is varied from 50uA to 14A with rise and fall time of 1us.

Overlaid Results:

Condition 1: VDD = 36V



Condition 2: VDD=72V



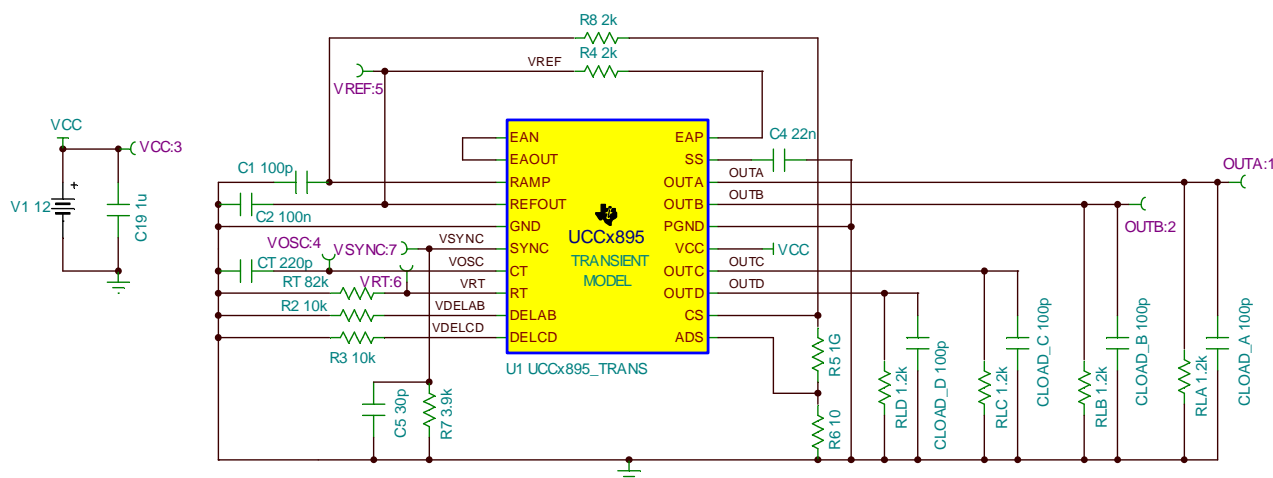
Tabulation of Results:

PARAMETER	PSPICE	TINA	UNIT
Average change in output voltage during IOUT transition (@VDD=36V)	188.7	177.80	mV
Average change in output voltage during IOUT transition (@VDD=72V)	184.07	179.25	mV

Conclusion: The simulation results of TINA and PSPICE are matching with each other. It is observed that even after transition in input occurs, the output shows slight increase in average value from steady state value and transient peak amplitudes are almost negligible for both conditions.

6.4 Oscillator Test

TINA Schematic:



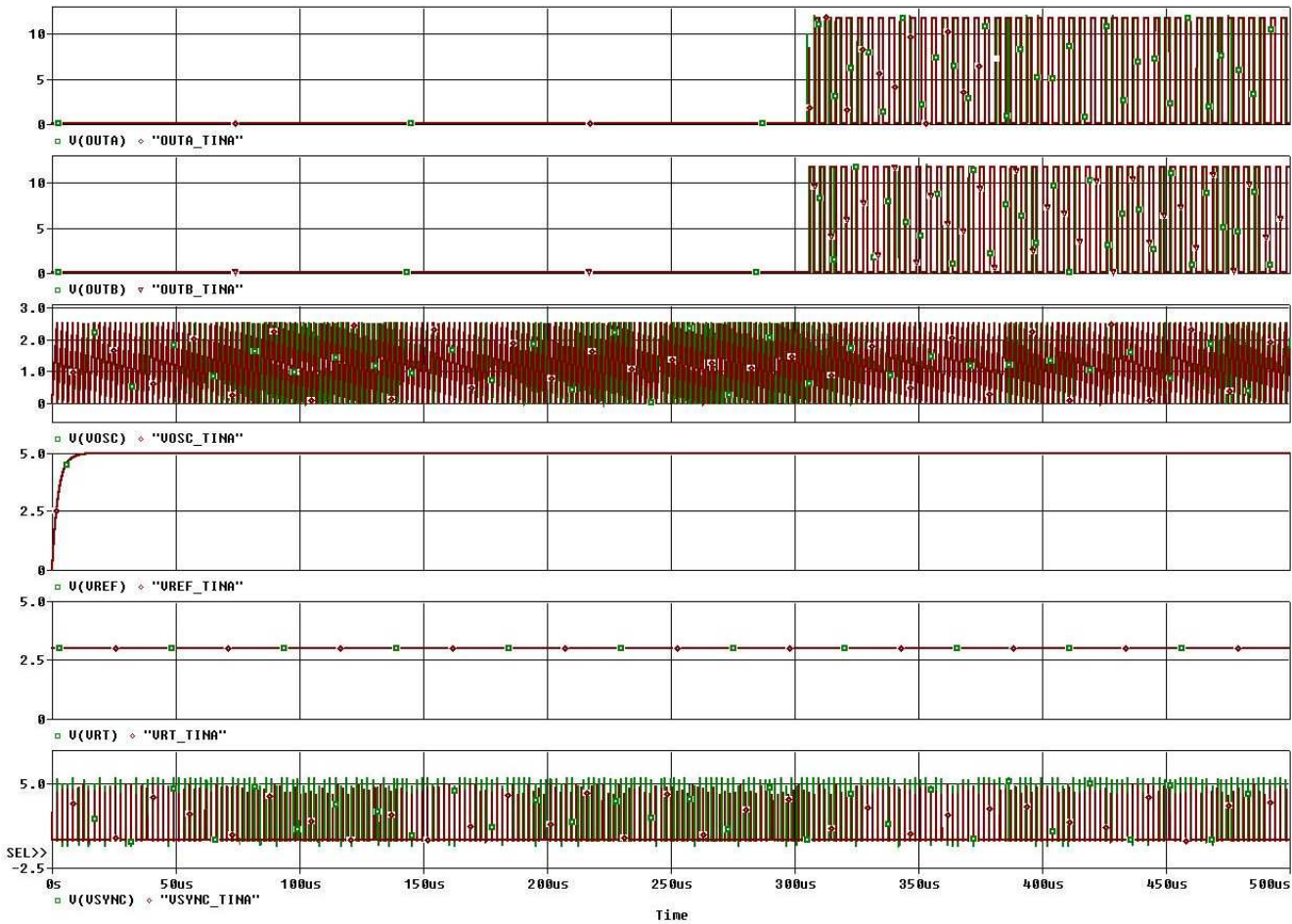
Description:

1. Above application circuit is developed to test the oscillator functionality and measure oscillation parameters.
2. Under steady state condition, different parameters of oscillation like frequency, peak and valley voltages and SYNC pulse width are measured.
3. A parallel combination of $R = 1.2\text{k}\Omega$ and $C = 100\text{pF}$ is connected at the output of each channel. In addition to this an RC combination of $3.9\text{k}\Omega$ and 30pF is connected at the SYNC terminal as per test conditions from datasheet.
4. Also repetitive measurements of oscillator frequency were carried out for different values of R_T and C_T to get Frequency vs. R_T/C_T curve shown in electrical characteristics in datasheet.

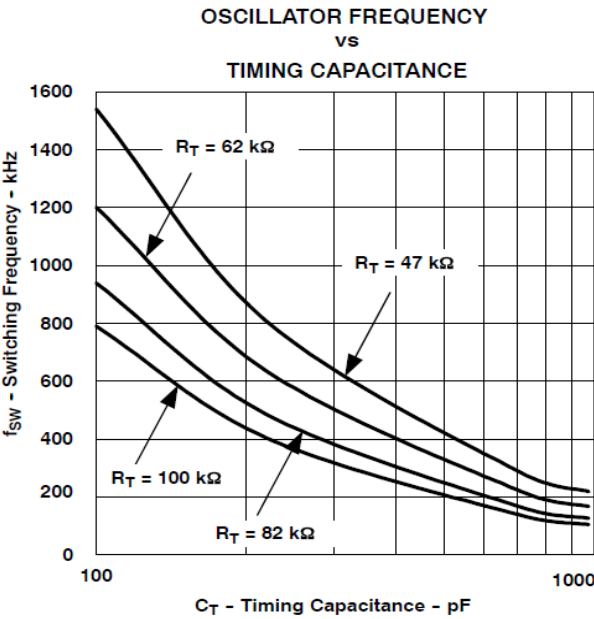
Test Conditions and Additional Analysis Options (if any):

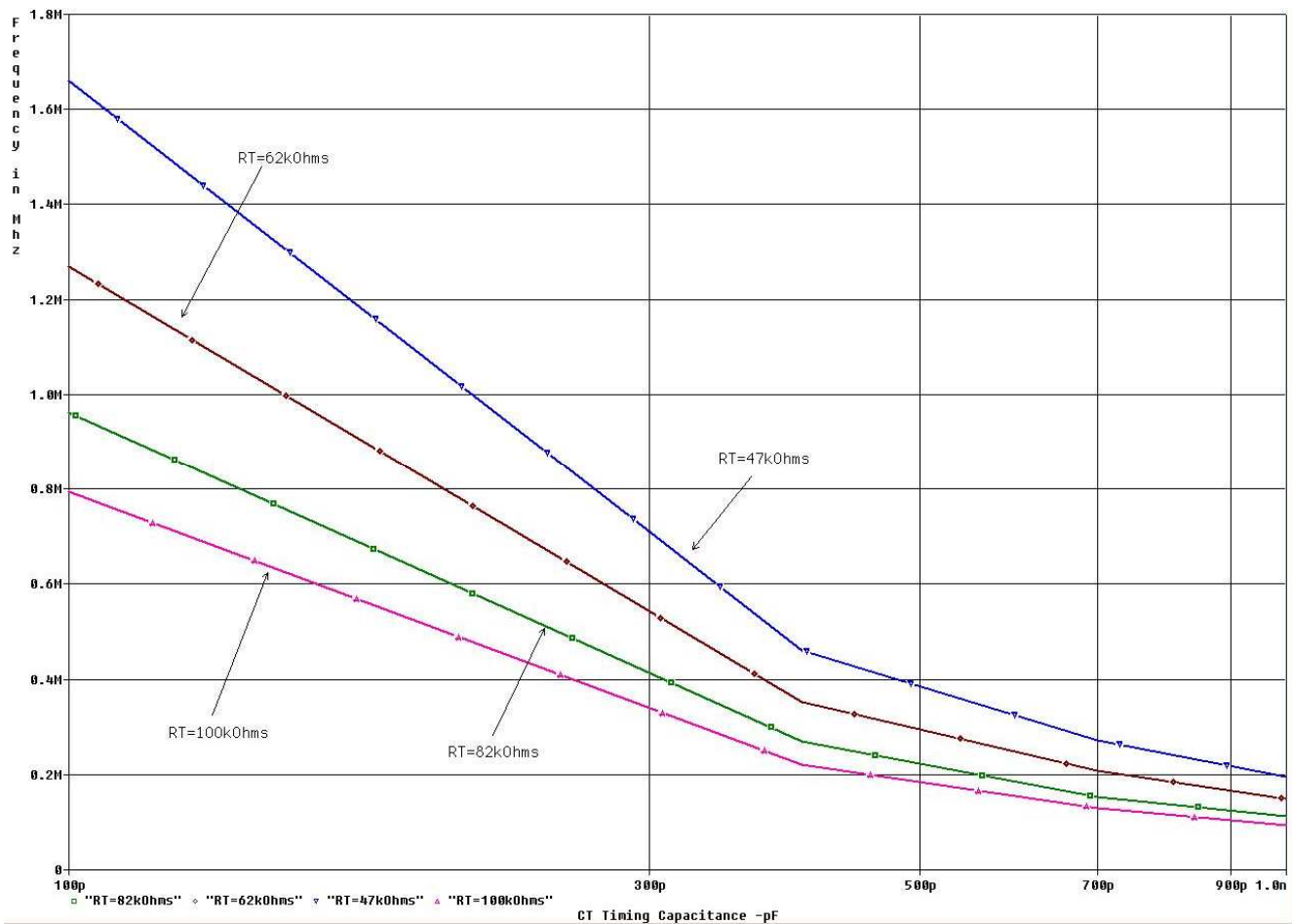
1. $V_{CC} = 12V$
2. $R_T = 82k\Omega$
3. $C_T = 220pF$
4. For Frequency vs. R_T/C_T curve, R_T is varied from $47k\Omega$ to $100k\Omega$ and C_T from $100pF$ to $1000pF$

Overlaid Results:



Characteristic Plot:





NOTE: Above measurements are carried out using parametric stepping in TINA and the results are imported in PSPICE to obtain curves.

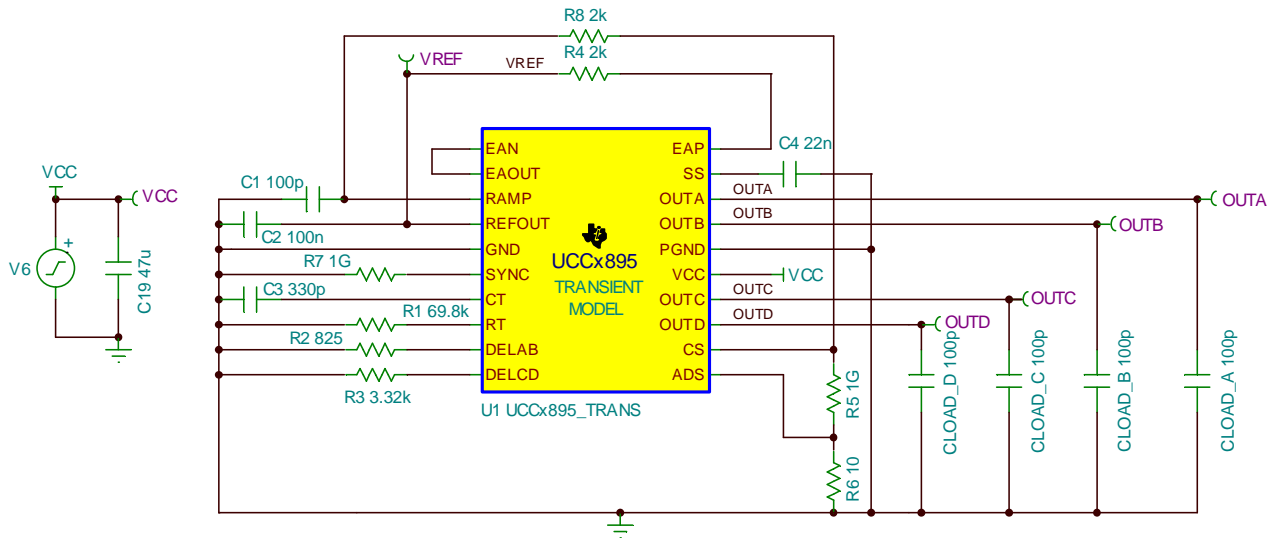
Tabulation of Results:

PARAMETER	EXPLANATION	PSPICE	TINA	DATASHEET	UNIT
f_{OSC}	Oscillator frequency	470.92	467.39	500	kHz
V_{RT}	Timing resistor voltage	3	3	3	V
$V_{CT(peak)}$	Timing capacitor peak voltage	2.5091	2.5048	2.35	V
$V_{CT(valley)}$	Timing capacitor valley voltage	0.001	0.001	0.2	V
	Sync output pulse width	18.297	20.228	85	ns

Conclusion: The simulation results of TINA and PSPICE are matching within the acceptable limits.

6.5 Steady State Analysis

TINA Schematic:



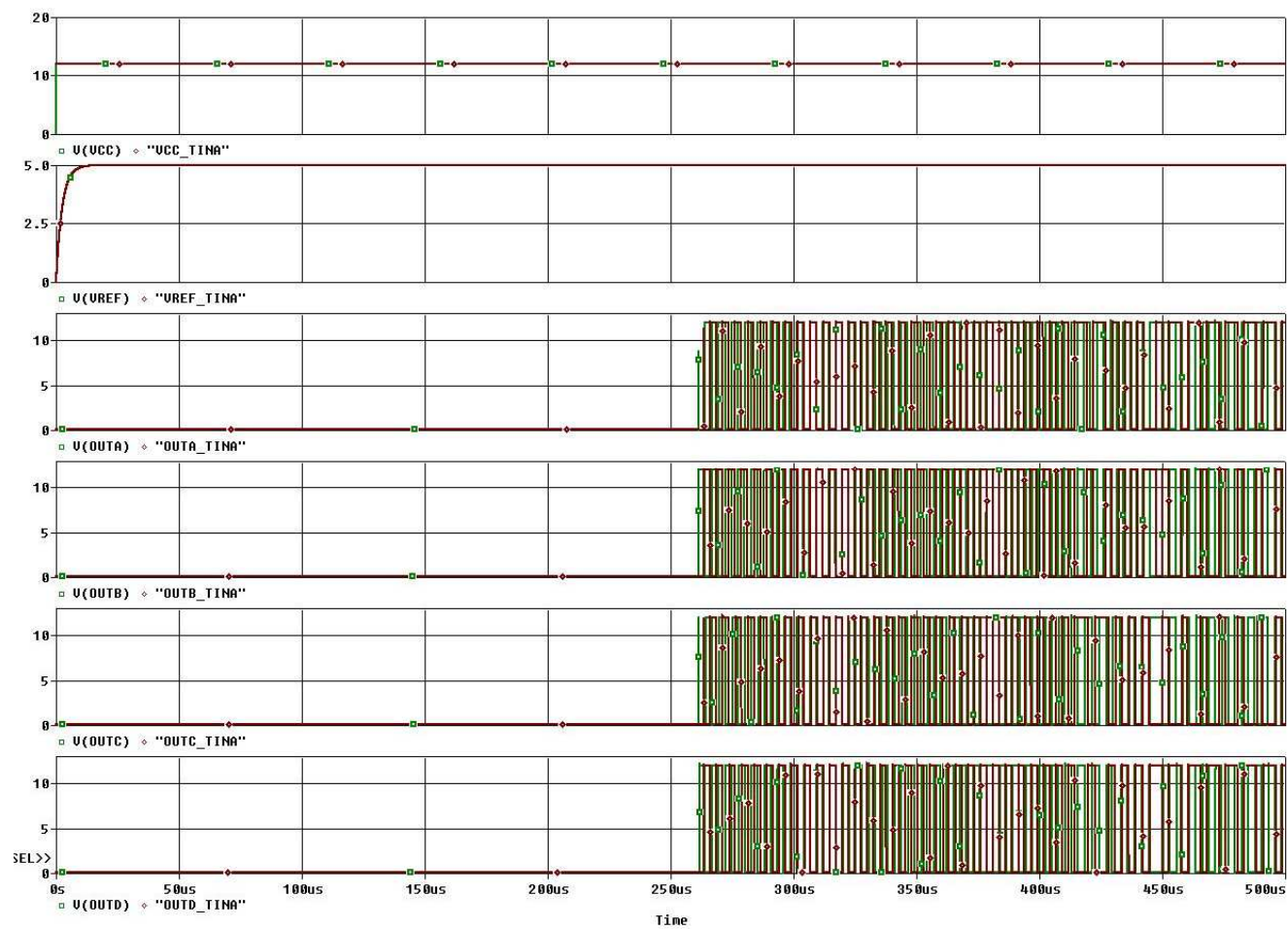
Description:

1. Above application circuit is developed to test the steady state rise and fall times at the output of the macro depending on load conditions.
2. A load capacitor of 100pF is connected at the output of each channel as per datasheet test conditions.
3. The rise and fall times are measured as 10% to 90% of the steady state output value of the channel.

Test Conditions and Additional Analysis Options (if any):

1. VCC = 12V
2. CLOAD_A = CLOAD_B = CLOAD_C = CLOAD_D = 100pF

Overlaid Results:



Tabulation of Results:

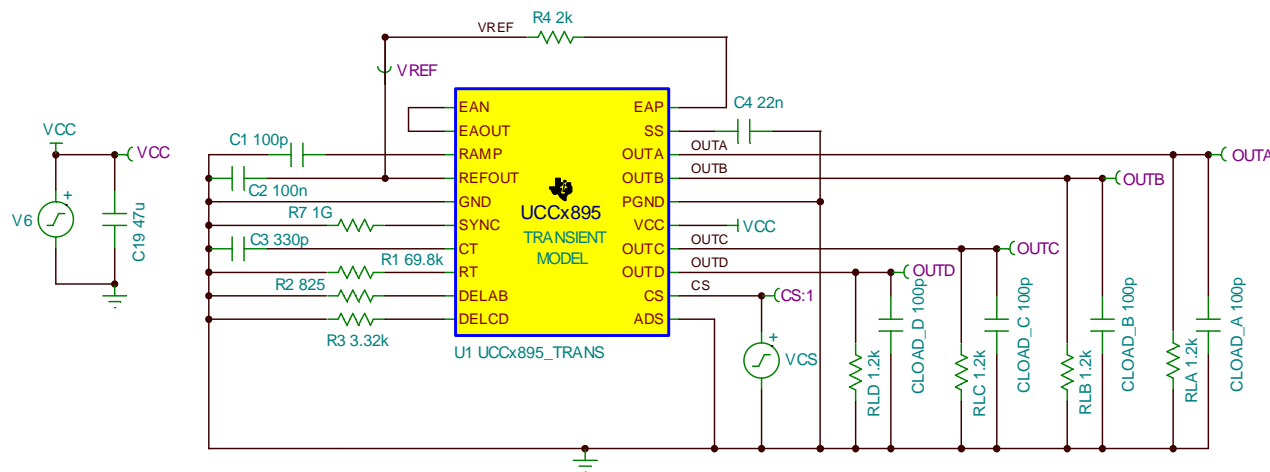
PARAMETER	EXPLANATION	PSPICE	TINA	DATASHEET	UNIT
t_R	Rise time	8.7977	7.319	20	ns
t_F	Fall time	10.184	7.566	20	ns

The rise and fall times are measured as 10% to 90% of steady value.

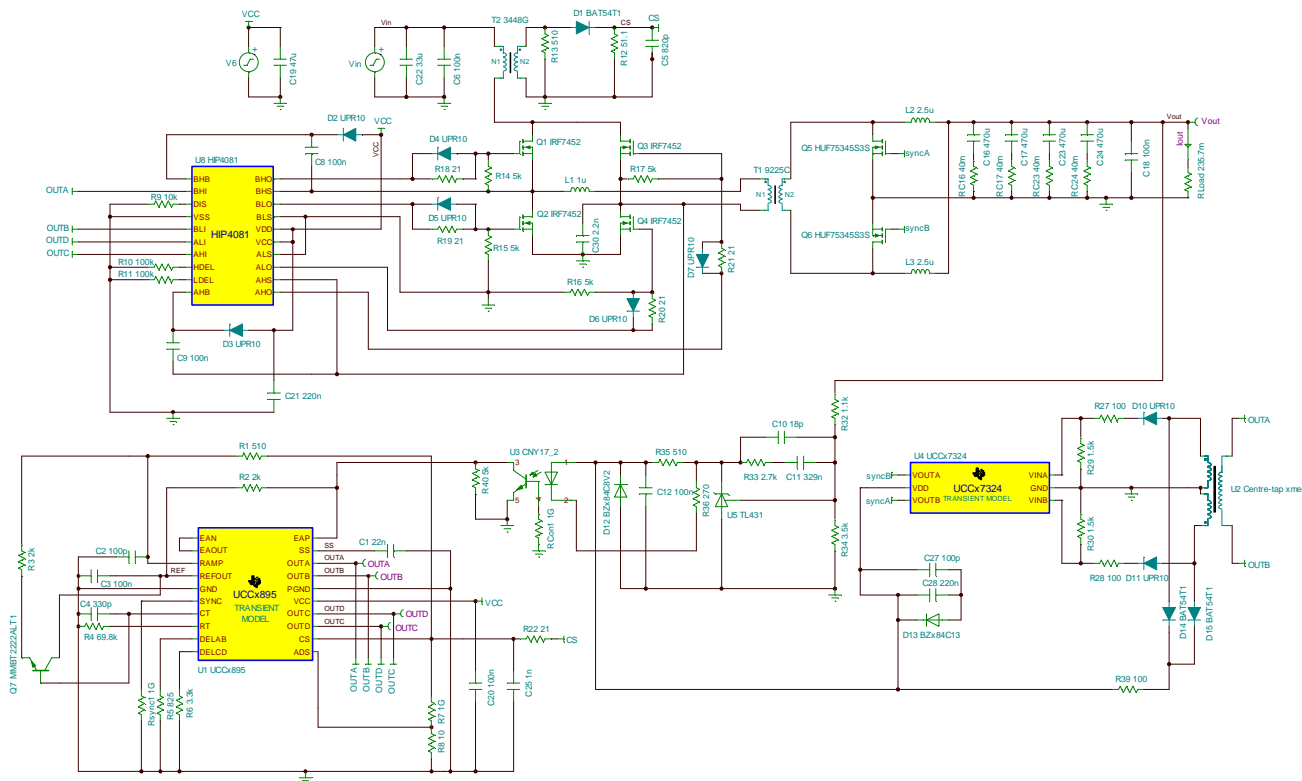
Conclusion: The simulation results of TINA and PSPICE are matching and are within the limits of typical values from datasheet.

6.6 Output Shutdown: CS

TINA Schematic 1:



TINA Schematic 2:



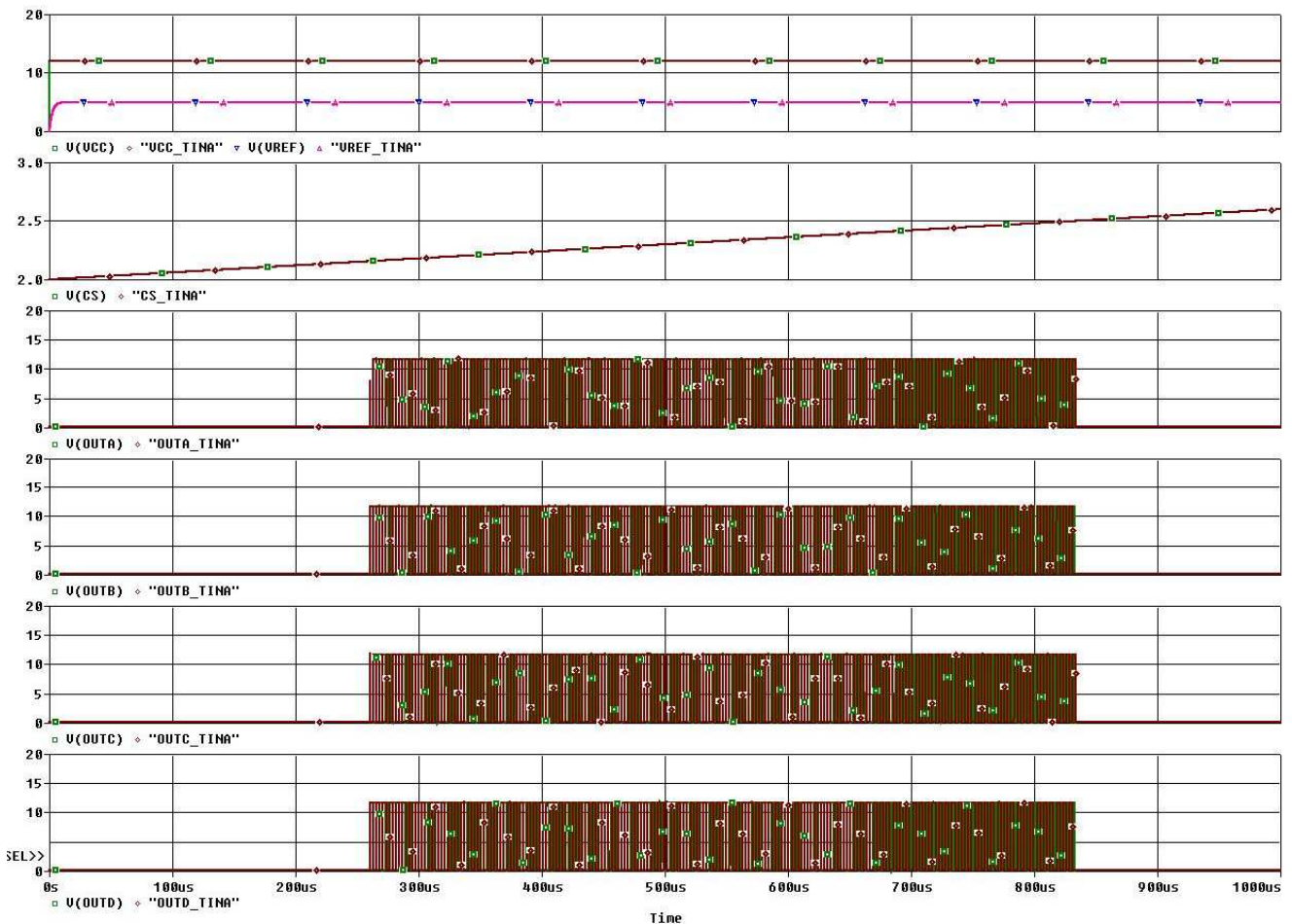
Description:

1. Above application is developed to test the shutdown condition at the output due to increase in CS input signal voltage. Generally CS pin is used to sense overcurrent condition in large rectifier circuits where the above component forms a part of the system.
2. The overcurrent condition at the output is sensed and converted back to voltage and fed back to the controller, which depending on the limit set by user, shuts down itself for overcurrent.
3. To test this functionality, the CS input signal is ramped up from 2V to 3V in 5ms, since the shutdown limit for CS lies within the range.
4. The value of CS for which switching at the output stops abruptly after the steady state has reached is noted down as shutdown limit.

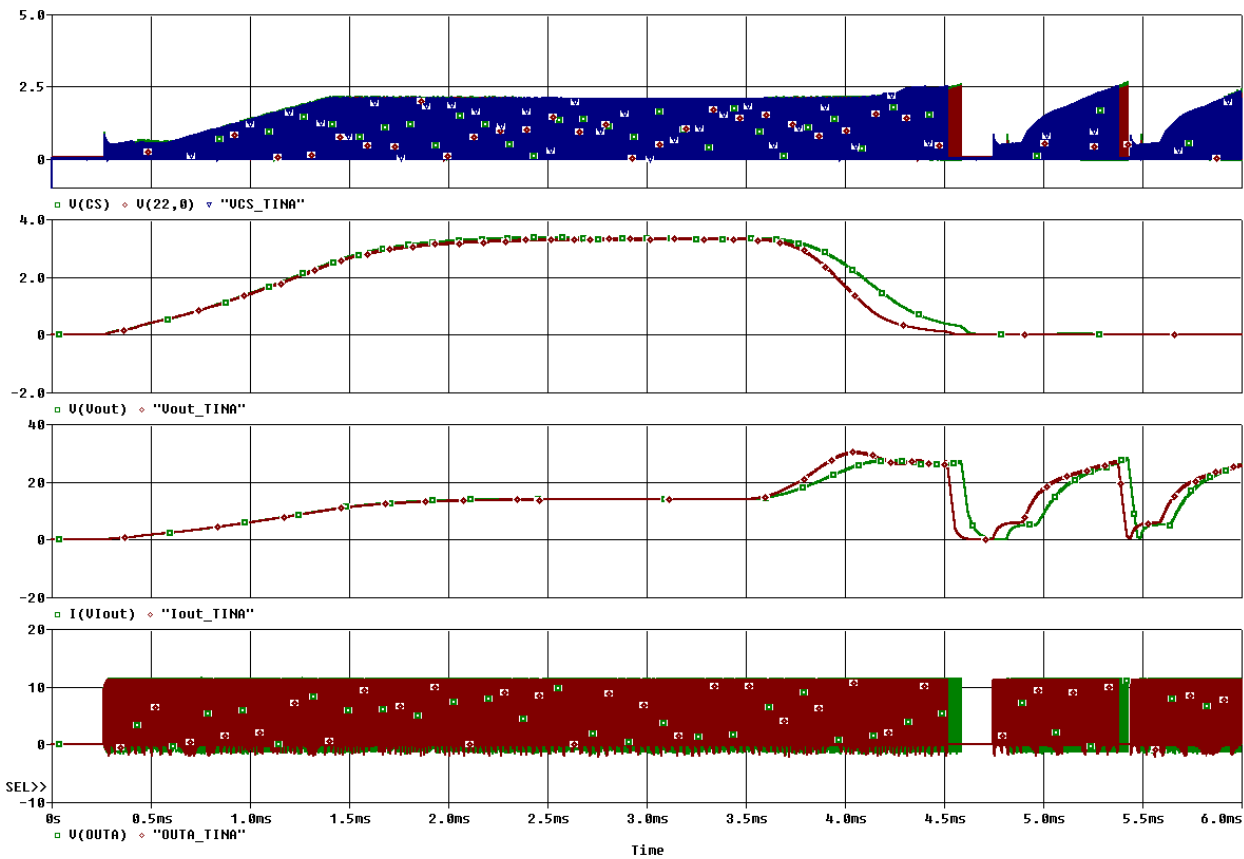
Test Conditions and Additional Analysis Options (if any):

1. VCC = 12V
2. VCS = 2V to 3V ramp up in 5ms

Overlaid Results for Condition 1:



Overlaid Results for Condition 2:



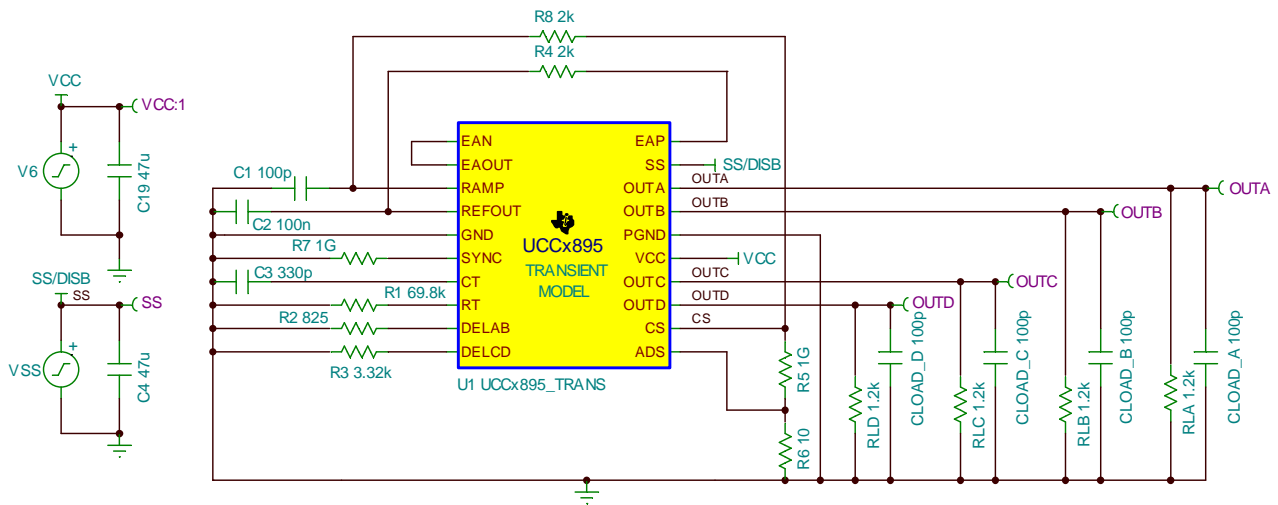
Tabulation of Results:

PARAMETER	PSPICE	TINA	DATASHEET	UNIT
V _{CS} Threshold	2.4984	2.4987	2.5	V

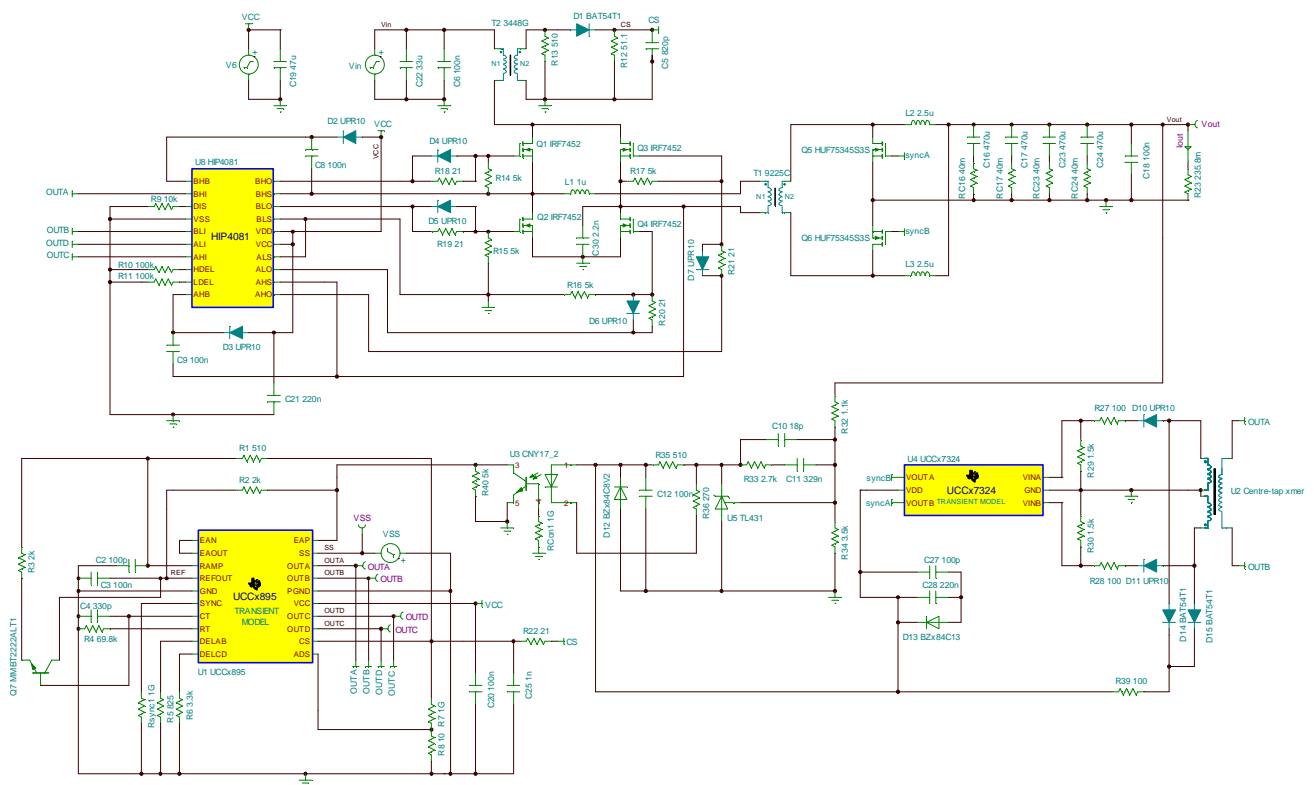
Conclusion: The simulation results of TINA and PSPICE are matching within the acceptable limits. The overlaid results of condition 2 show actual system shutdown for overcurrent condition at the system output.

6.7 Output Shutdown: SS/DISB

TINA Schematic 1:



TINA Schematic 2:



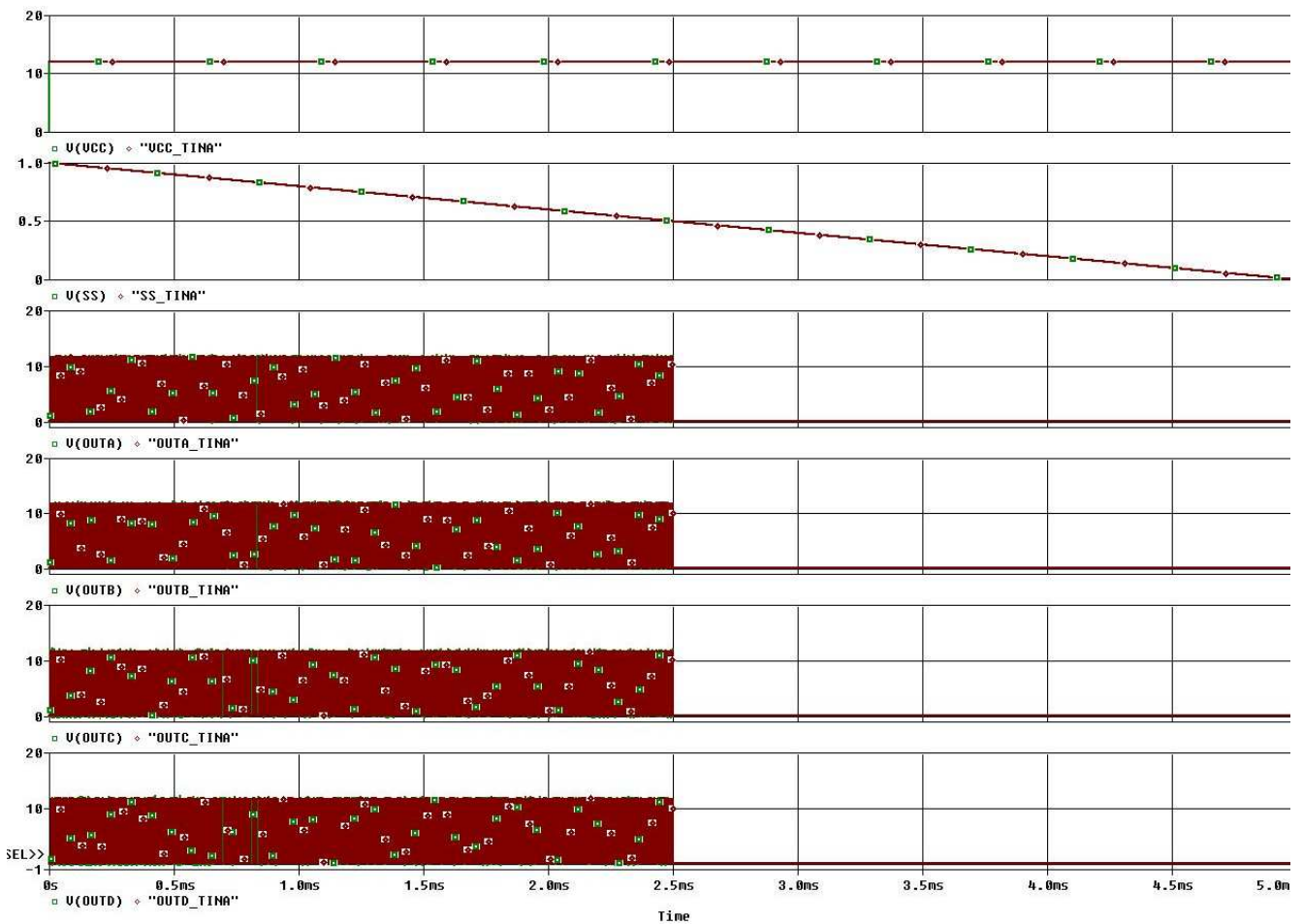
Description:

1. Above application is developed to test the shutdown condition at the output due to decrease in SS input signal voltage. Generally SS pin is utilised by user externally to force chip into disable mode or to make it enter into soft start-up mode.
2. To test this functionality, the SS input signal is ramped down from 1V to 0V in 5ms, since the shutdown limit for SS/DISB lies within this range.
3. The value of SS for which switching at the output stops abruptly after the steady state has reached is noted down as shutdown limit.

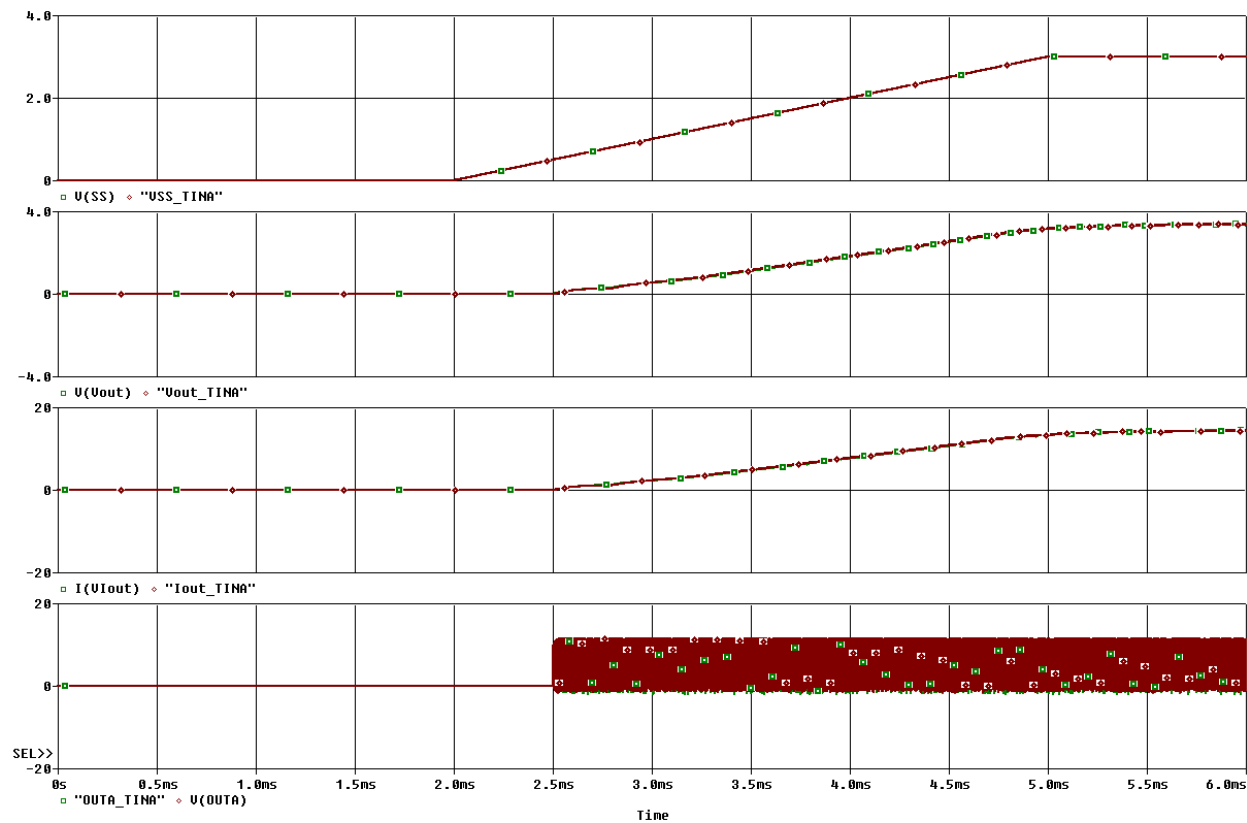
Test Conditions and Additional Analysis Options (if any):

1. VCC = 12V
2. VSS = 1V to 0V ramp down in 5ms

Overlaid Results for Condition 1:



Overlaid Results for condition2:



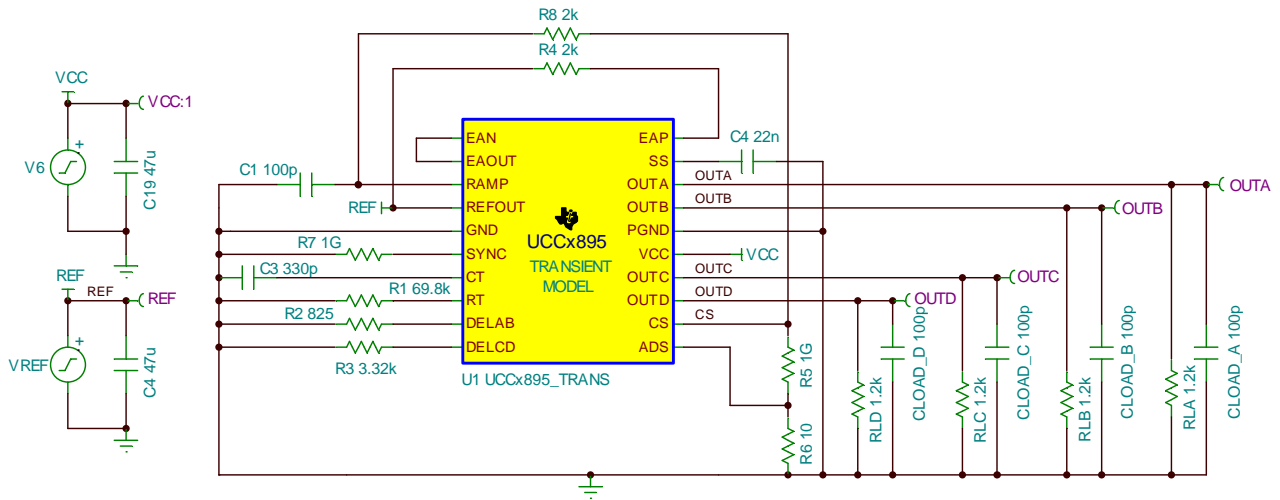
Tabulation of Results:

PARAMETER	PSPICE	TINA	DATASHEET	UNIT
V _{SS/DISB} Threshold	499.999	500.352	500	mV

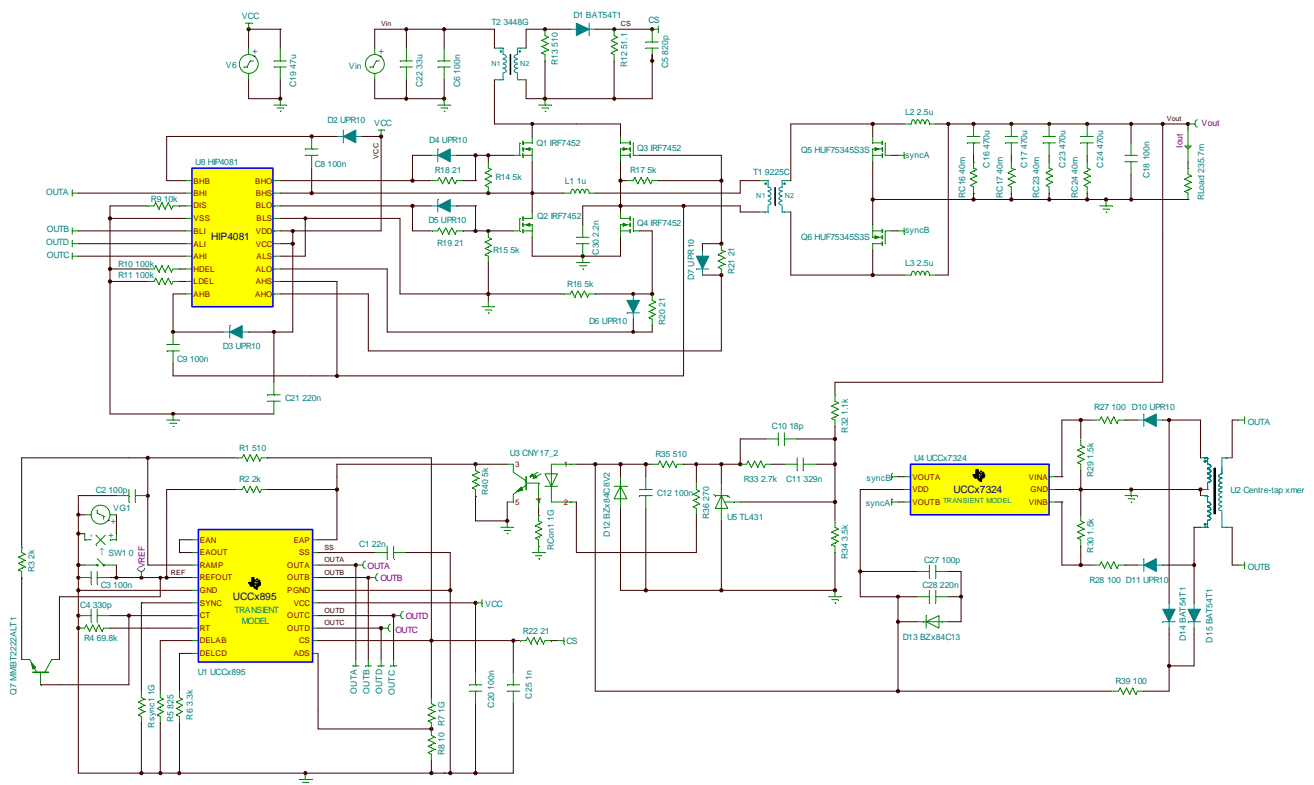
Conclusion: The simulation results of TINA and PSPICE are matching within the acceptable limits. The overlaid results of condition 2 show actual system startup behaviour that occurs only after SS/DISB terminal crosses threshold level.

6.8 Output Shutdown: REF

TINA Schematic 1:



TINA Schematic 2:



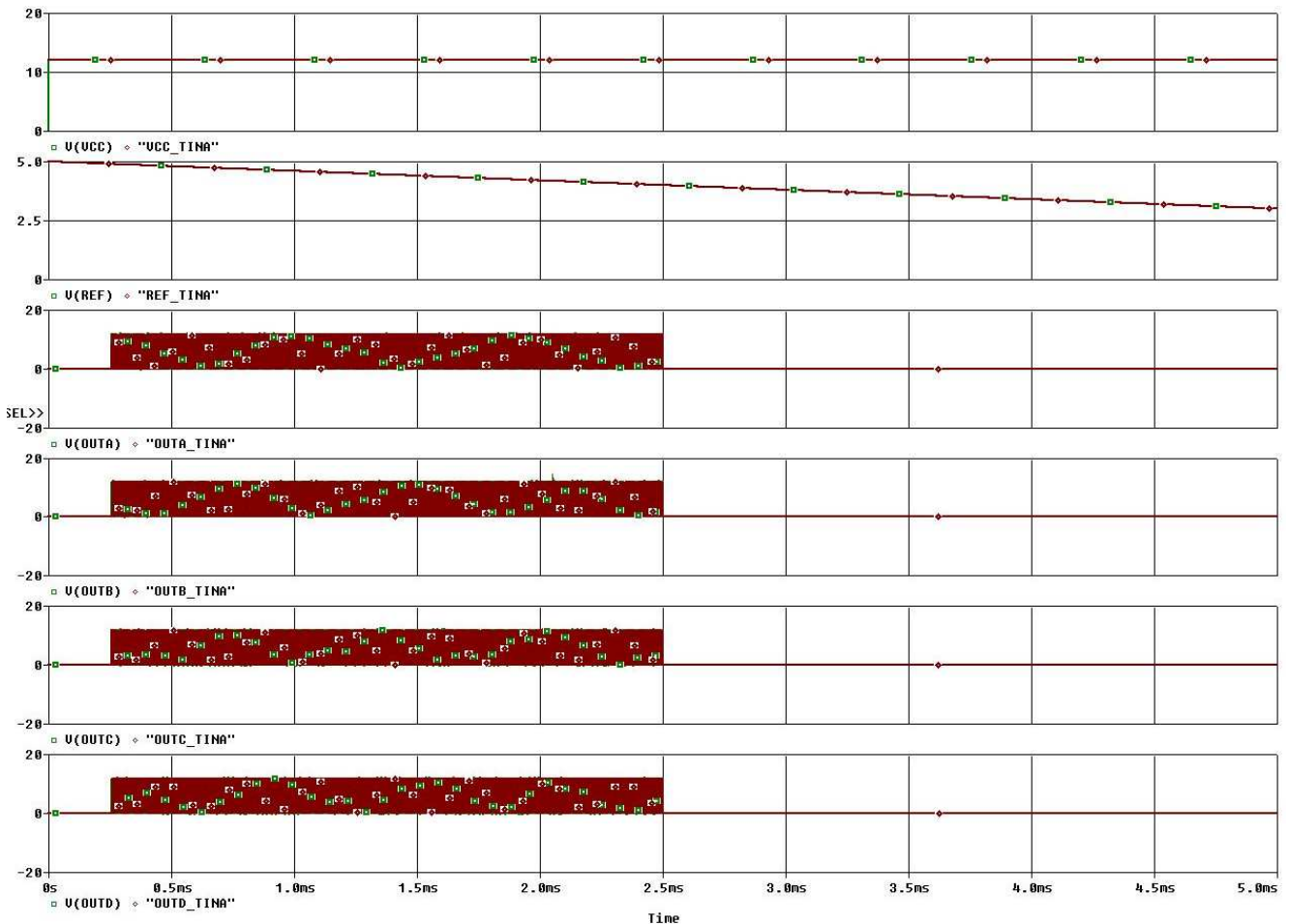
Description:

1. Above application is developed to test the shutdown condition at the output due to forced decrease in REF signal voltage. The device can provide constant 5V output through REF terminal, with limited driving capability.
2. When this pin is forced externally to drop down below threshold limit, the device shuts down.
3. To test this functionality, the REF input signal is ramped down from 5V to 3V in 5ms since the shutdown limit for REF lies within the range.
4. The value of REF for which switching at the output stops abruptly after the steady state has reached is noted down as shutdown limit.

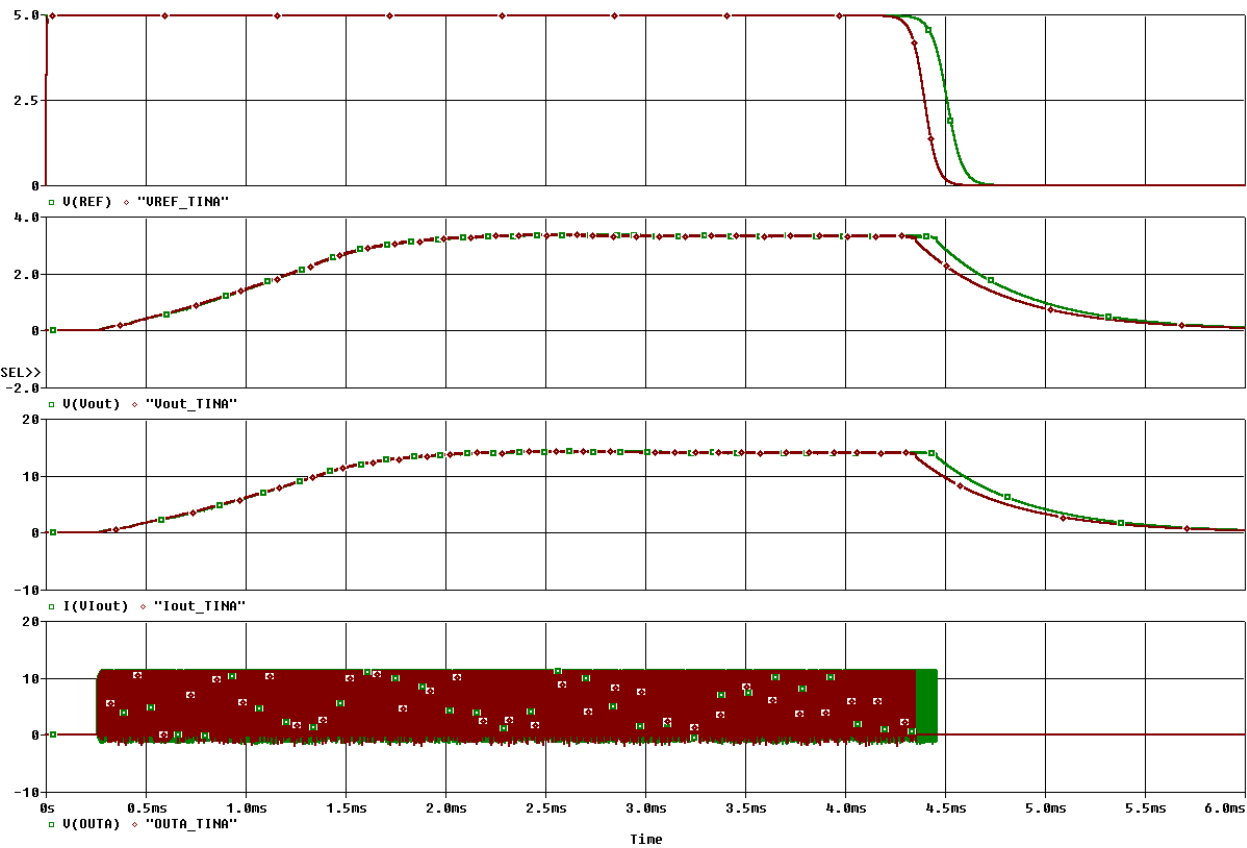
Test Conditions and Additional Analysis Options (if any):

1. VCC = 12V
2. VREF = 5V to 3V ramp down in 5ms

Overlaid Results for Condition 1:



Overlaid Results for Condition 2:



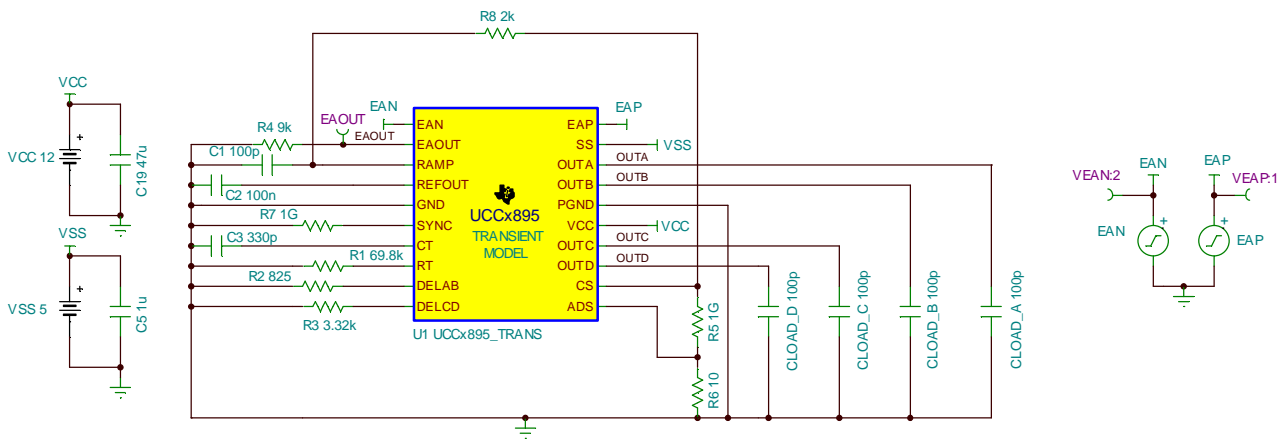
Tabulation of Results:

PARAMETER	PSPICE	TINA	DATASHEET	UNIT
V _{REF} Threshold	4.00	4.0007	4	V

Conclusion: The simulation results of TINA and PSPICE are matching within the acceptable limits. The overlaid results of condition 2 show actual system shutdown for overcurrent condition on REF terminal.

6.9 Error Amplifier

TINA Schematic:



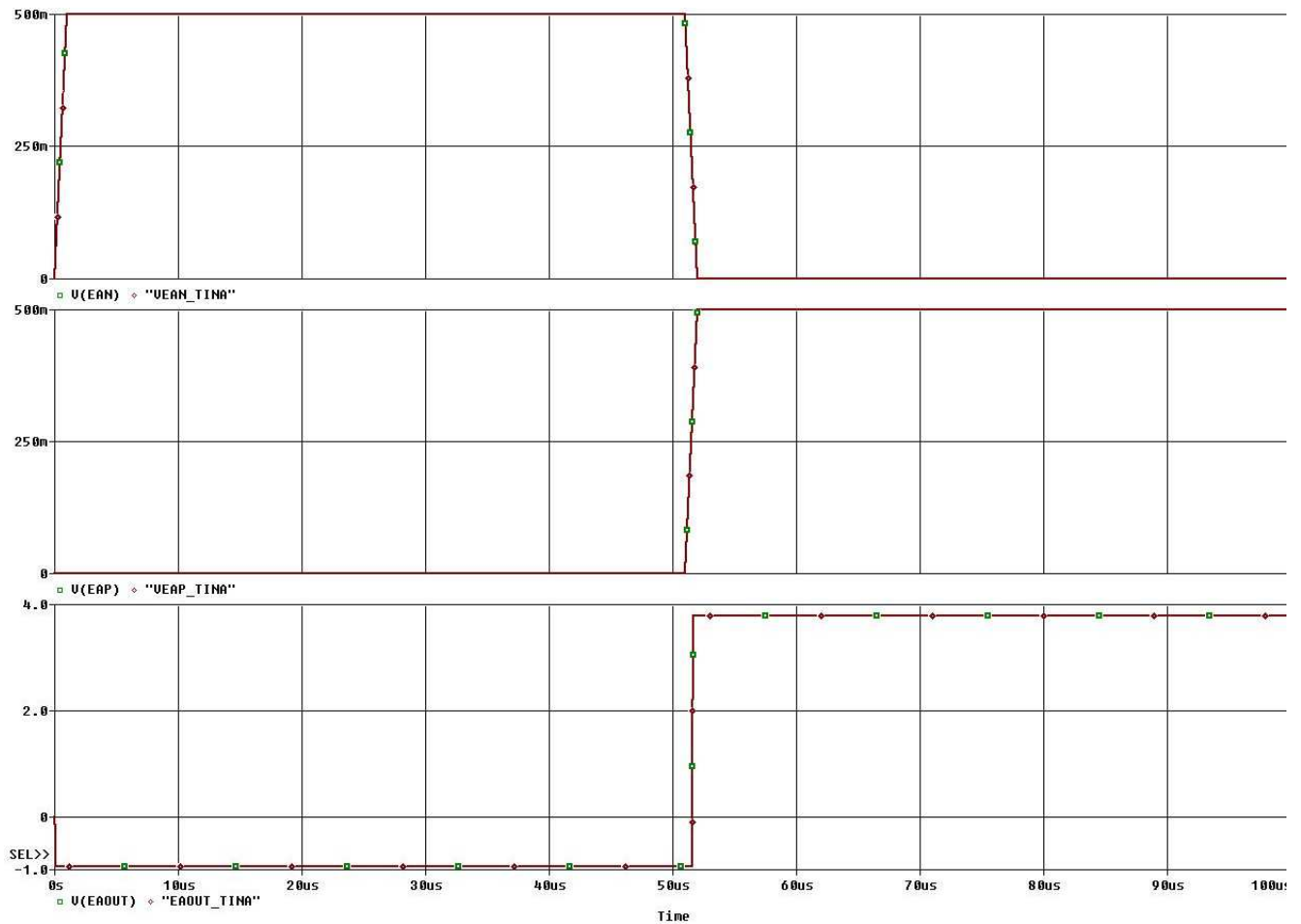
Description:

1. Above circuit is developed to test the error amplifier module in the component.
2. The AC analysis of the error amplifier is carried out to test its frequency response and to calculate unity gain bandwidth and open loop gain.
3. Also the offset voltage, High and Low level output voltages V_{OH} and V_{OL} , are calculated through transient analysis using test conditions mentioned in datasheet.

Test Conditions and Additional Analysis Options (if any):

1. $VCC = 12V$
2. $VSS = 5V$
3. $VEAN = 500mV$
4. $VEAP = 1V$ pulse with rise time = fall time = $1\mu s$ and period $100\mu s$.

Overlaid Results:



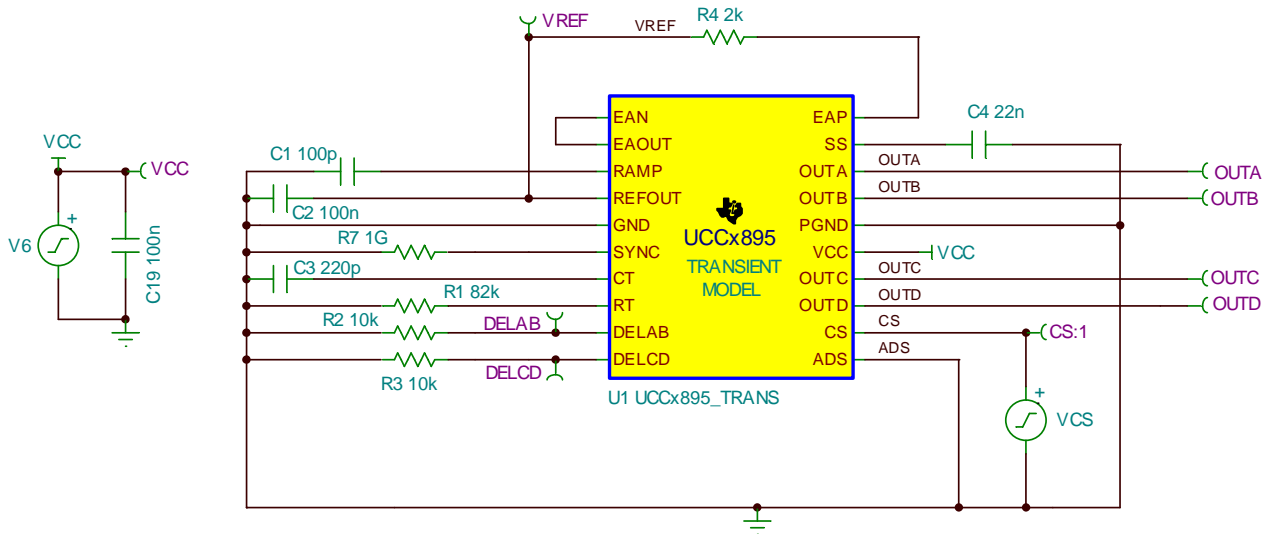
Tabulation of Results:

PARAMETER	EXPLANATION	PSPICE	TINA	DATASHEET	UNIT
V_{IO}	Offset voltage	-14.188	-14.187	0	mV
EAOUT_VOH	High-level output voltage	3.7804	3.7804	4.5	V
EAOUT_VOL	Low-level output voltage	-946.695	-946.695	200	mV

Conclusion: The PSPICE and TINA results are matching within the acceptable limits with each other but they differ with the datasheet specified values for EAOUT_VOH and EAOUT_VOL.

6.10 Adaptive Delay Set

TINA Schematic:



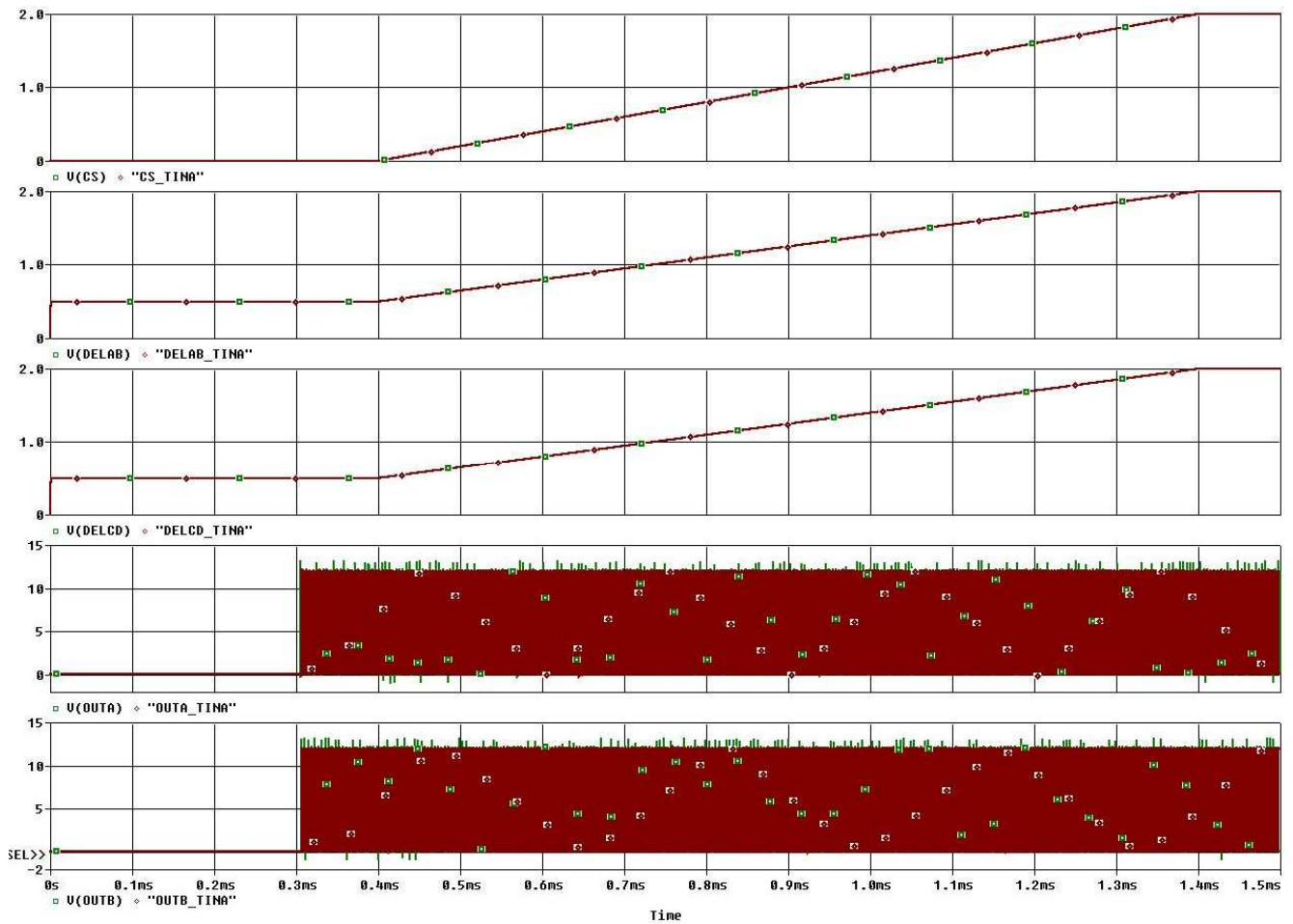
Description:

1. Above circuit is developed to test the Adaptive Delay Set (ADS) functionality in the component.
2. The CS input signal is varied from 0V to 2V in a time span of 1ms. The ADS signal input is grounded.
3. No delay modulation occurs when ADS and CS inputs are at same potential while increasing delay modulations is observed for increasing potential difference between the ADS and CS terminals.
4. Measurements are taken for two corner conditions of ADS = CS= 0V and ADS = 0V, CS=2V.

Test Conditions and Additional Analysis Options (if any):

1. VCC = 12V
2. VADS = 0V
3. VCS = 0V to 1V rising up ramp

Overlaid Results:



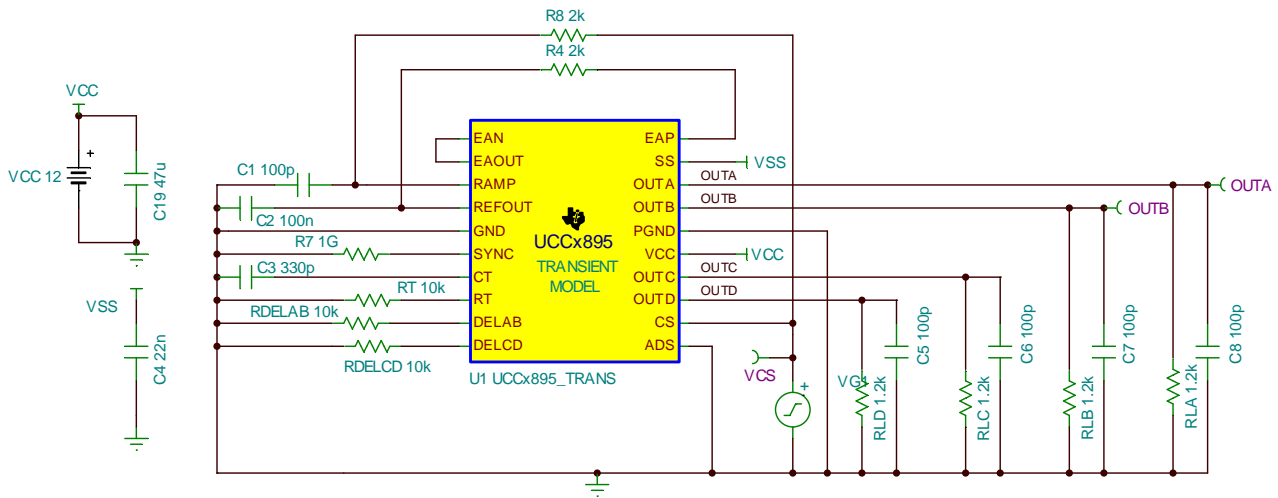
Tabulation of Results:

PARAMETER	TEST CONDITION	PSPICE	TINA	DATASHEET	UNIT
V_{DELAB}	ADS = CS = 0V	499.971	499.971	500	mV
V_{DELCD}	ADS = CS = 0V	499.971	499.971	500	mV
V_{DELAB}	ADS = 0V CS = 2V	1.999	1.999	2.0	V
V_{DELCD}	ADS = 0V CS = 2V	1.999	1.999	2.0	V
t_{DELAY}	ADS = CS = 0V	487.396	226.786	560	ns

Conclusion: The PSPICE and TINA results are matching within the acceptable limits with each other but they differ with the datasheet specified value for Delay Time. All other results match with datasheet.

6.11 Delay Programming

TINA Schematic:



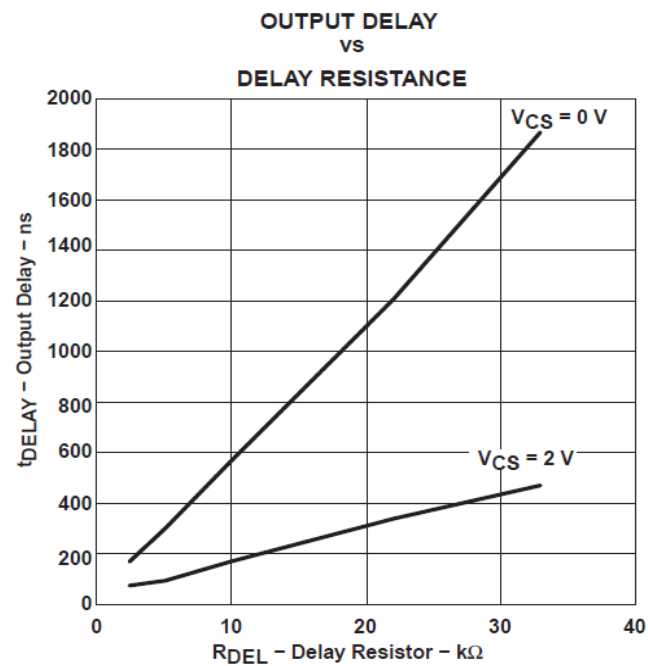
Description:

1. Above application is developed to test the delay programming functionality of the macro model.
2. The test is carried out through use of different delay resistances (RDELAB and RDELCD) and for different conditions of CS input signal.
3. Maximum delay modulation occurs when ADS is grounded. The tests are carried out for CS = 0V and CS = 2V conditions with RDELAB = RDELCD = 2k Ω to 35k Ω .

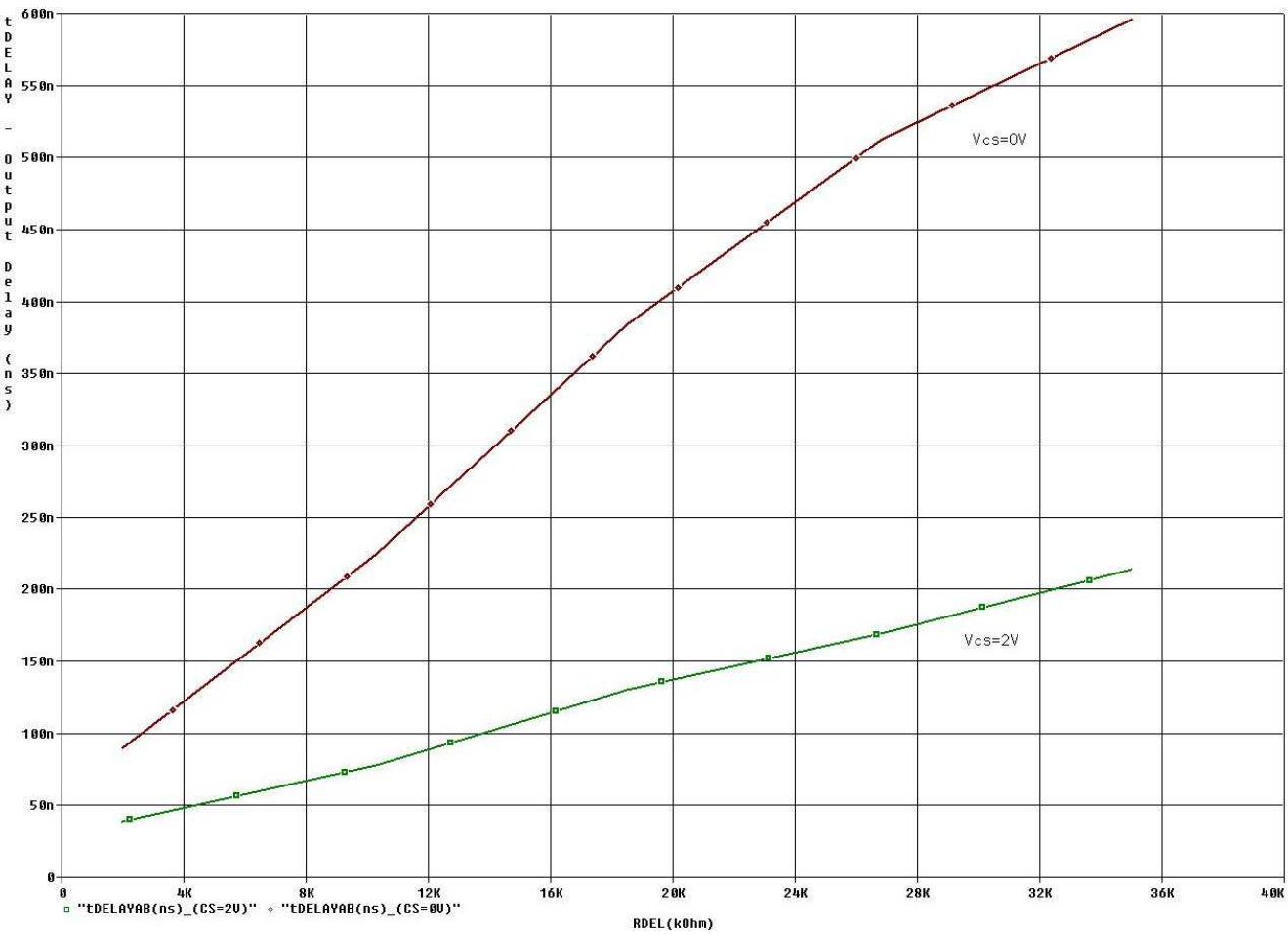
Test Conditions and Additional Analysis Options (if any):

1. VCC = 12V
2. VCS = 2V pulse with initial delay of 300us and period of 200us, rise time = fall time = 1us.
3. ADS terminal grounded.

Characteristic Plot:



TINA Results:

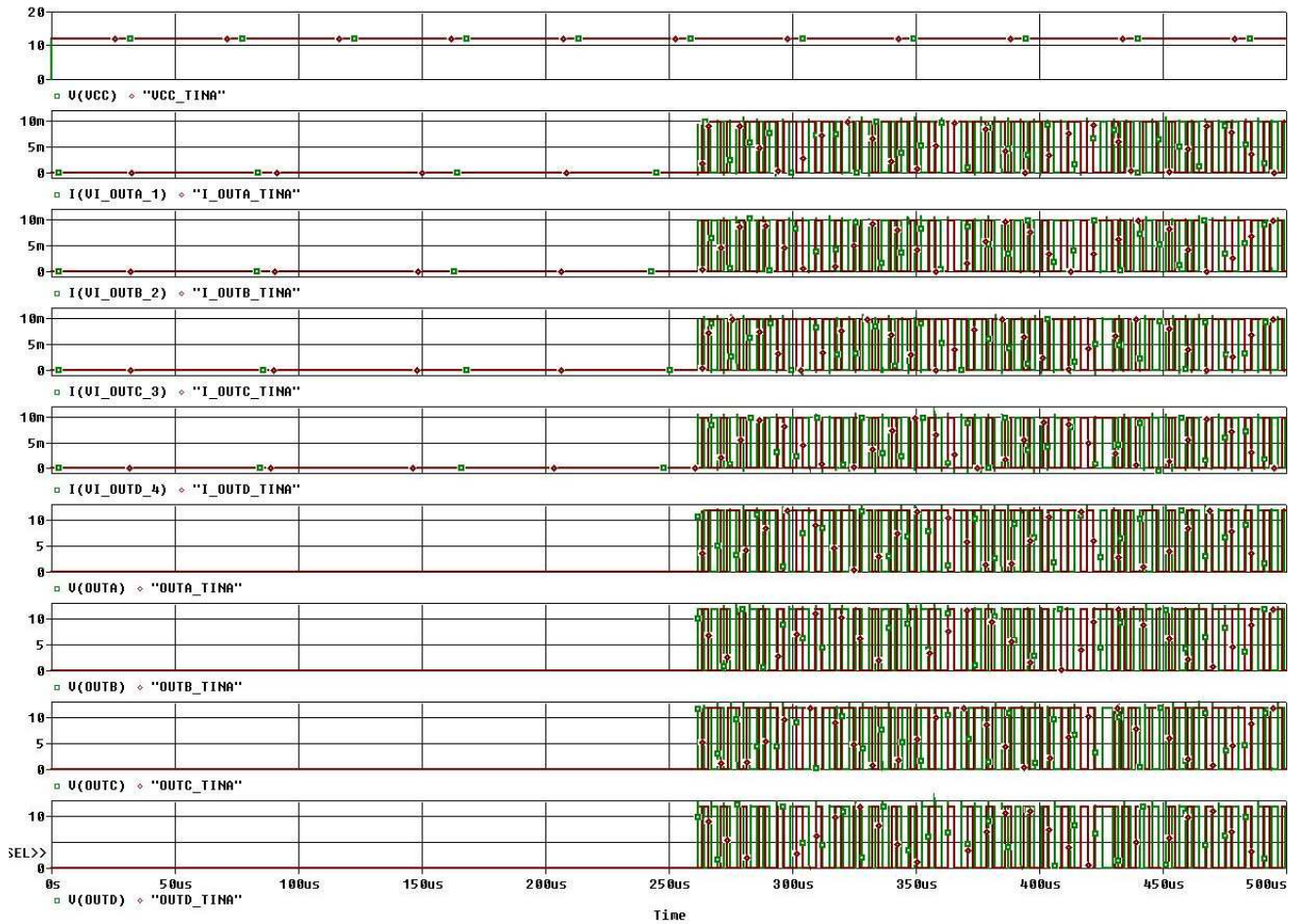


Tabulation of Results:

RDELAB	t_{DELAB}		UNIT
	CS=0V	CS=2V	
2k Ω	89.6	39.08	ns
10.3k Ω	224.15	77.9	ns
18.5k Ω	384.26	129.87	ns
26.8k Ω	512.35	168.83	ns
35k Ω	596.3	214.29	ns

Conclusion: The simulations results in TINA show same trend as that of the characteristic plot from datasheet.

Overlaid Results:



Tabulation of Results:

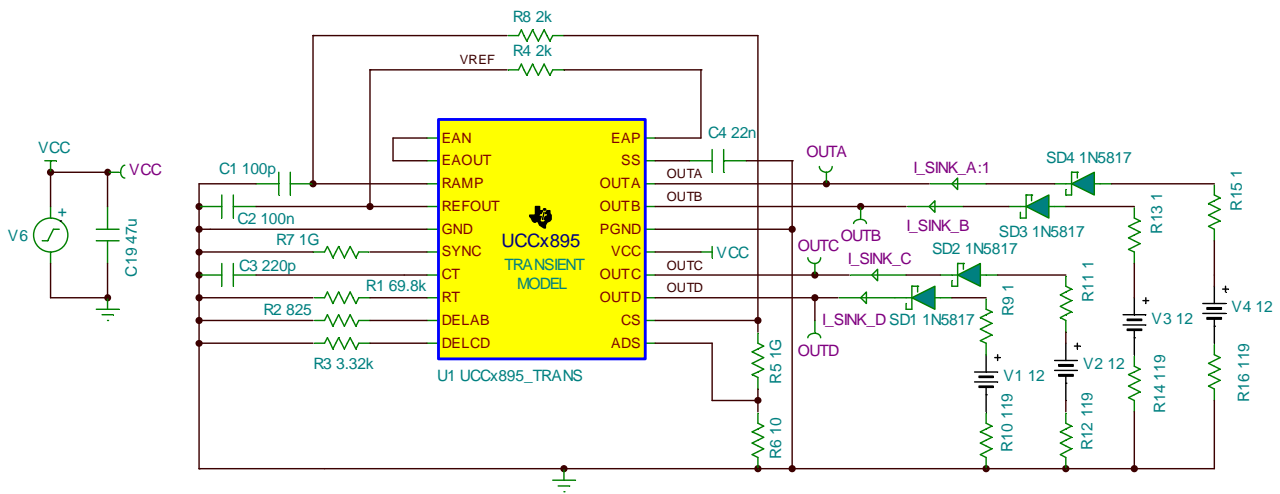
PARAMETER	TEST CONDITION	PSPICE	TINA	DATASHEET	UNIT
IOUT_HO	RL = 1.2kΩ	9.756	9.756	10	mA
VOUT_HO	RL = 1.2kΩ	11.707	11.707	11.750	V
IOUT_HO	RL = 120Ω	92.308	92.308	-	mA
VOUT_HO	RL = 120Ω	9.2308	9.2308	-	V

Same values of IOUT and VOUT are observed on all 4 channels for individual test conditions.

Conclusion: The PSPICE and TINA results are matching within the acceptable limits.

6.13 Output Sink Capacity

TINA Schematic:



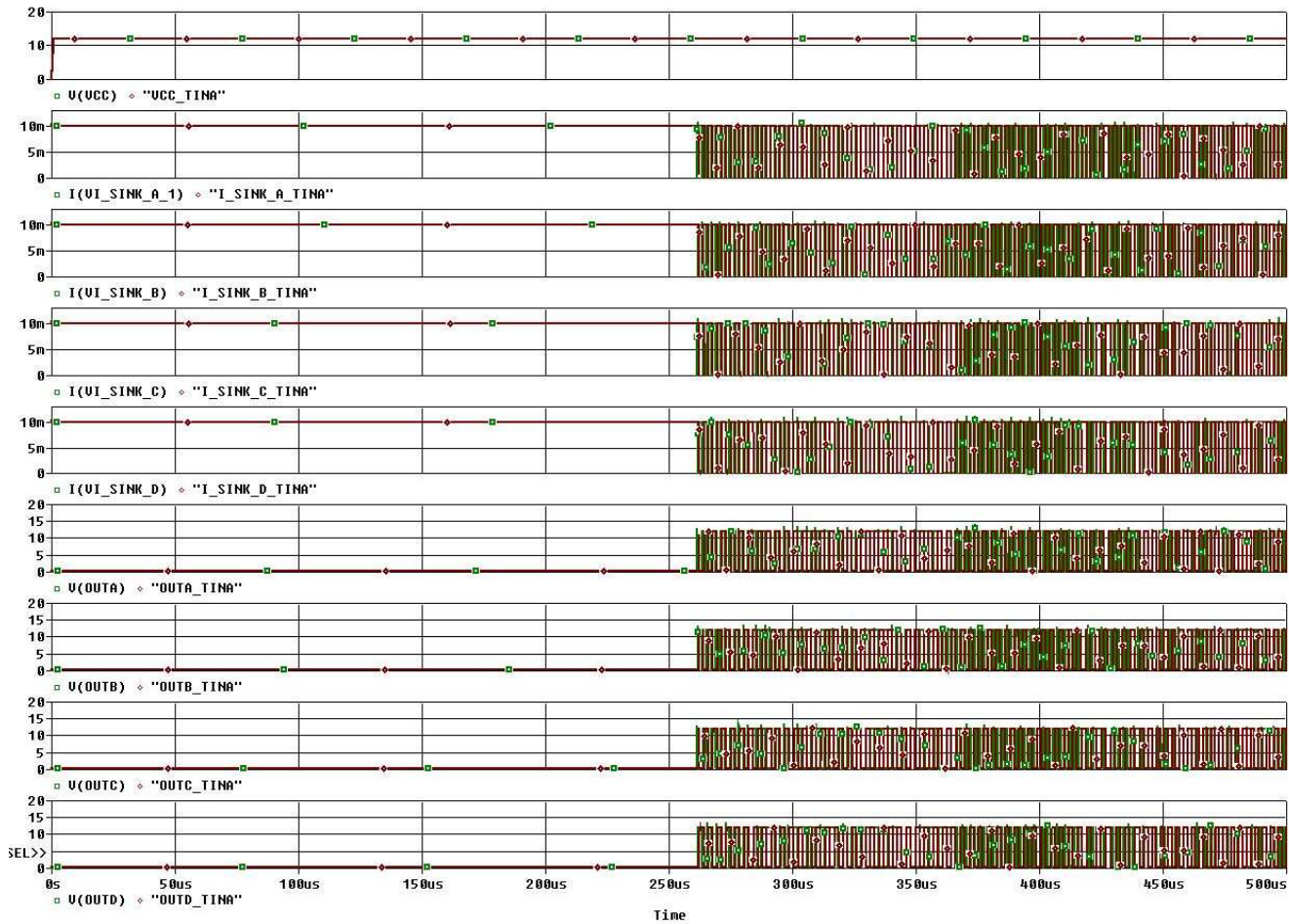
Description:

1. Above application is developed to test the response of the component under loading condition and also to test the output current sinking capacity of the model.
2. The circuit is tested for two different load current conditions (10mA and 100mA) through use of different load resistor values. Additional DC source and Schottky diode combination is connected at the load to clamp the output to 12V.
3. The output voltage and the output current through load resistor are monitored.

Test Conditions and Additional Analysis Options (if any):

1. VCC = 12V
2. RLOAD = 1147.82Ω

Overlaid Results:



Tabulation of Results:

PARAMETER	TEST CONDITION	PSPICE	TINA	DATASHEET	UNIT
IOUT_LO	RL = 1.147kΩ	9.94	9.94	10	mA
VOUT_LO	RL = 1.147kΩ	399.830	399.830	150	mV
IOUT_LO	RL = 120Ω	78.26	78.26	-	mA
VOUT_LO	RL = 120Ω	2.45	2.45	-	V

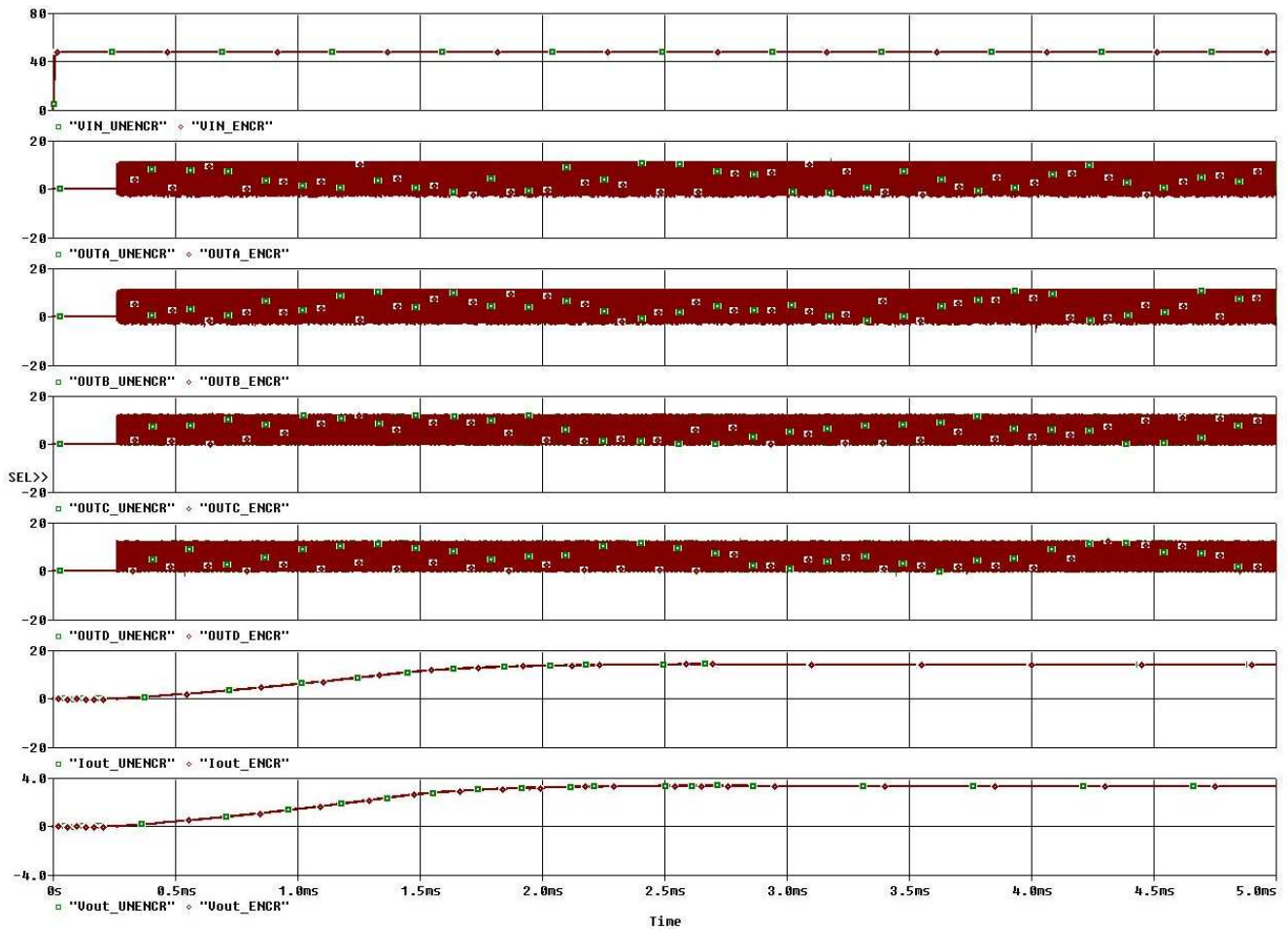
Same values of IOUT and VOUT are observed on all 4 channels for individual test conditions.

Conclusion: The PSPICE and TINA results are matching within the acceptable limits.

7. Encrypted Model Validation

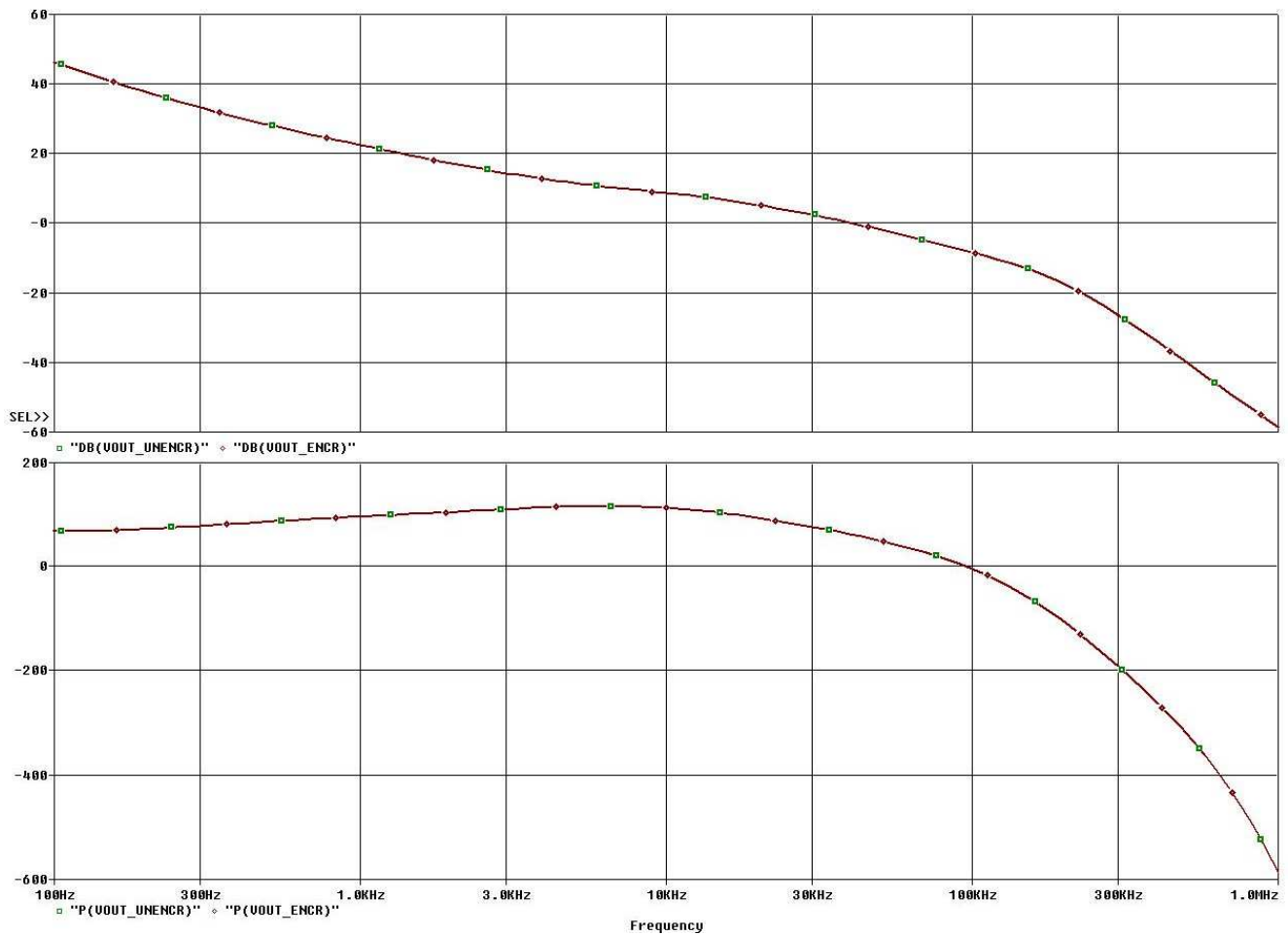
7.1 Transient Analysis

Overlaid Results:



7.2 Average Analysis

Overlaid Results:



Conclusion:

1. To validate the encrypted model, the Transient and Average testbenches have been simulated using the encrypted model.
2. These results are overlaid on the simulation results of same testbenches simulated using unencrypted model by importing both waveforms in PSPICE.
3. The overlaid results match.

8.2 Average Analysis

