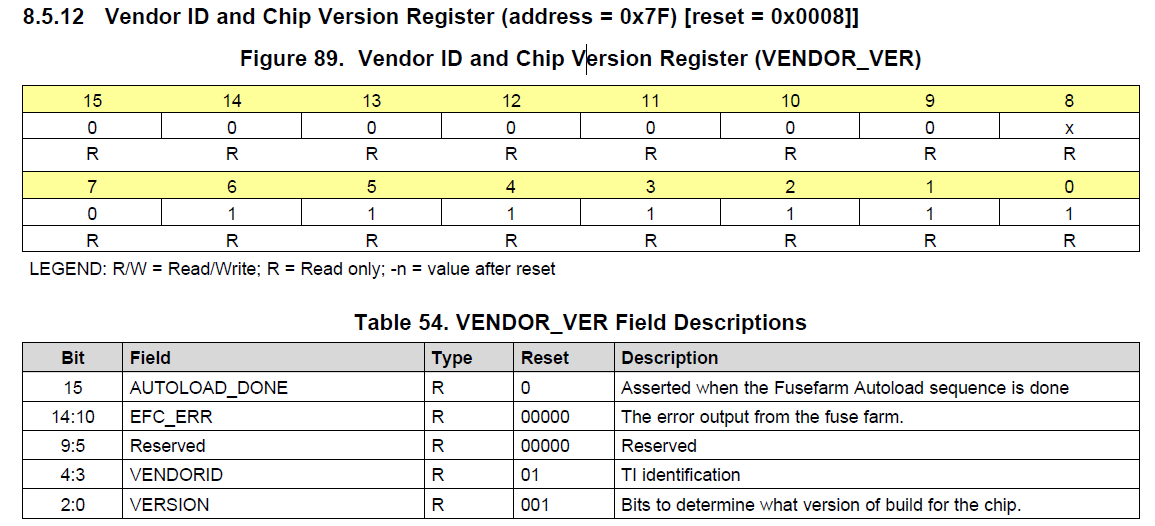
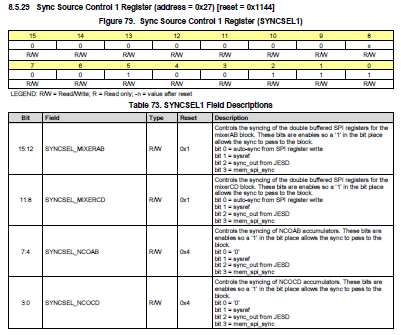
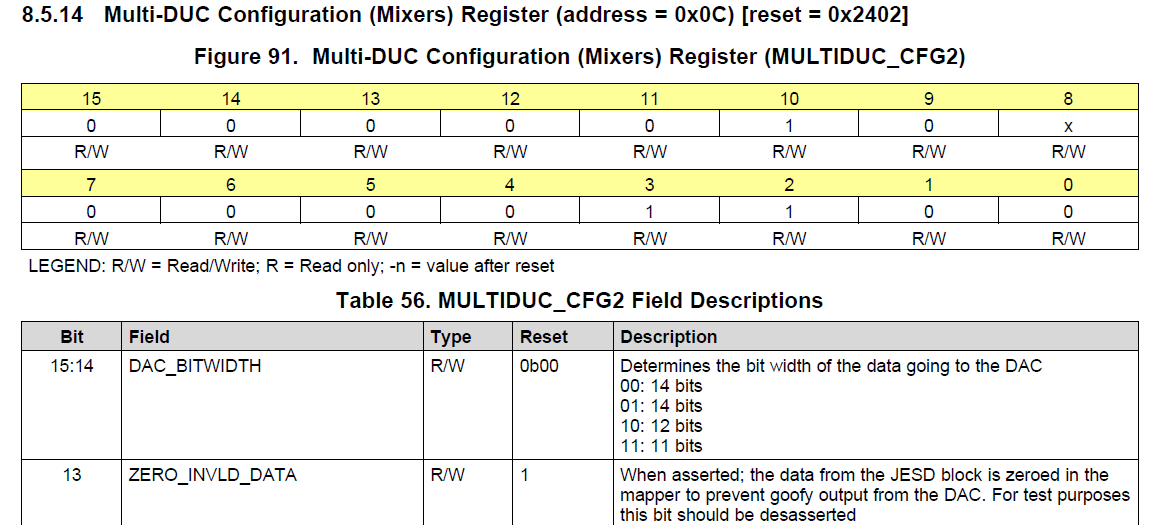
1. After power is applied and external reset is pulsed from low to high, verify bits [15:10] are 100000. If not, the fuse farm did not load. This has to occur before moving on.



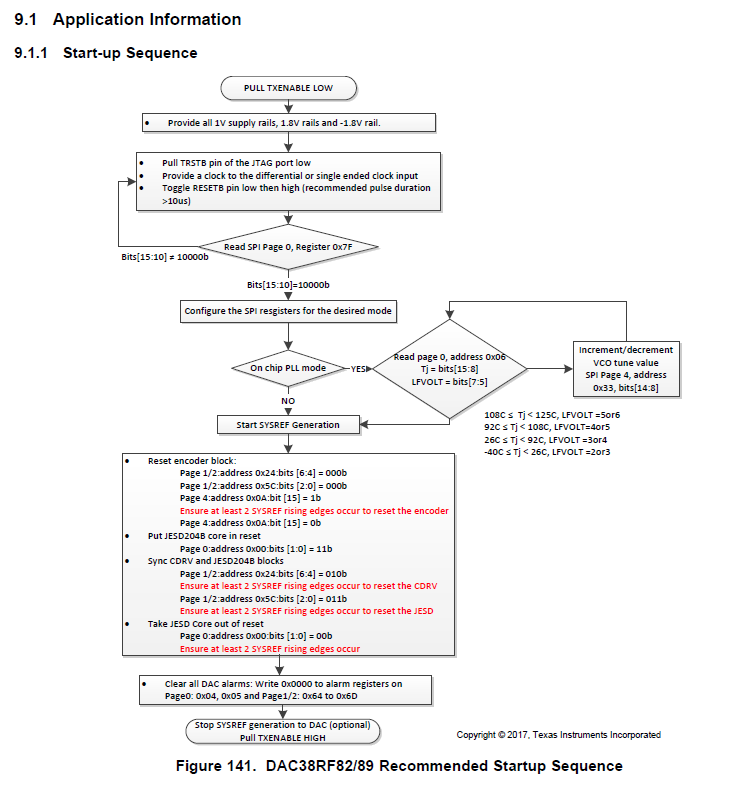
1. To check for SYSREF, run the DAC in NCO only mode and synchronize the NCO blocks to SYSREF. Make sure SYSREF is not an integer divided of the NCO frequency used. If SYSREF is present, the NCO will be unstable. Set address 0x27 in page 1 and 2 to 0x2828 to use SYSREF as the SYNC source. If SYSREF is present, the DAC output will now be many tones as the NCO will be constantly reset by the SYSREF signal. If SYSREF is disabled, the DAC output will be a stable NCO tone.



1. If SYSREF is DC coupled, it must have a CM voltage of 0.5V and at least a 100mV swing.
2. To verify if ILA data is wrong, set bit 13 of register 0xC in page 1 and page 2 to enable the ILA check sequence. With this bit set to a “1”, if the DAC has no output, setting this bit to a “0” turns off the ILA checker, and if there was a problem with only the ILA data, and all other registers are configured properly, the DAC will then start sending an output.



1. Lanes must be enables and assigned to the proper order.
2. Must do the proper reset sequence after the configuration file has been loaded.
3. SYSREF starts SYNC going low after JESD block is released from init state.
4. Follow the start-up sequence per the data sheet in section 9.1.



1. Suggest using SYSREF in continuous mode until link is consistently established.
2. Make sure 1 < K < 32 and 17 < F\*K < 1024 are meet.
3. RBD must be equal to or less than K.
4. Make sure the SYSREF is the correct frequency.

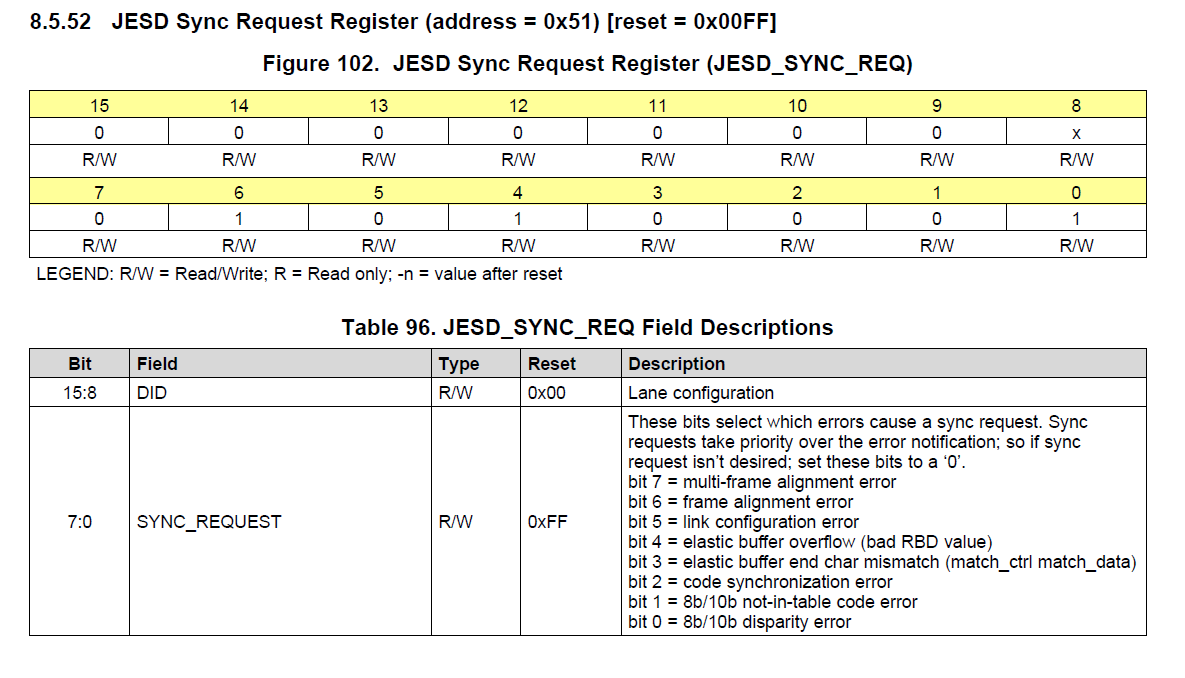
The clock supplied to the SYSREF pins should follow the standards for the SYSREF signal defined in the JESD204B specification. It must be synchronous with DACCLK and have sufficient setup and hold times with respect to DACCLK for proper alignment of the local multi-frame clock (LMFC) edge for deterministic latency. If a multiple pulse or continuous SYSREF signal is provided to the SYSREF pins, the frequency of the signal must be chosen such that the LMFC frequency is an integer multiple of the SYSREF frequency. This prevents the SYSREF signal from occurring in the middle of an LMFC cycle which will trigger a SYSREF alarm. The frequency of the LMFC is given by:

Where linerate is the throughput rate of a single lane given in bits/s and F and K are as defined in the JESD204B standard. The frequency of SYSREF can then be define as:

Where n is an integer, such that an integer number of LMFC cycles occur in a single SYSREF cycle. For ease, the SYSREF frequency can simply be set to the LMFC frequency.

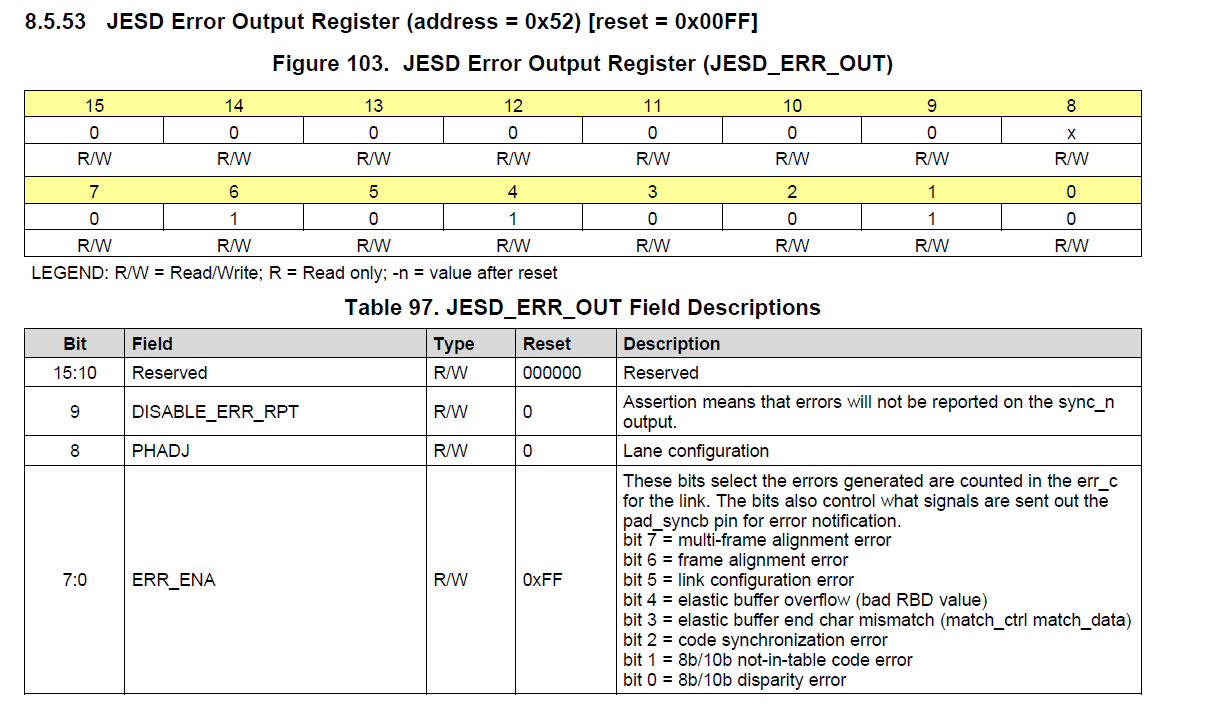
In the case of a non-periodic SYSREF signal (gapped pulse, or multiple-pulse) the SYSREF signal should be DC-coupled to the DAC SYSREF input. The SYSREF input pins require a 0.5-V common-mode voltage, while most clocking standards have common-mode voltages above 1 V. If the LMK04828 is used as the clock source, then the LCPECL output format can be used. The LCPECL output format has a common-mode voltage of 1.1 V, which can be lowered through a resistive voltage divider to 0.55 V using the termination scheme shown in figure 2. The left side resistor network should be kept close to the clock chip to provided proper source termination to maintain good signal integrity at the DAC’s SYSREF pins.

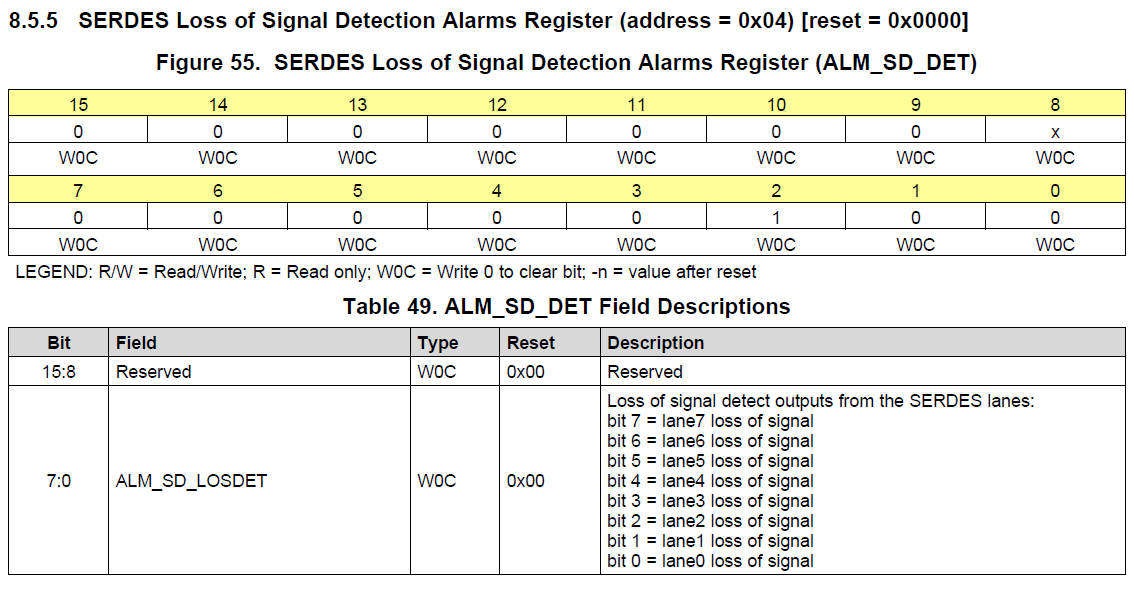
1. The following register determines which error will cause SYNC to de-assert (go low):



The default value used by TI is 0x001F.

1. This register reports JESD errors. GUI default is 0xFF. If bit 9 is set to 0, if any of the errors occur, a short SYNC pulse will occur.





If any lane reports a loss of signal, the device will pull SYNC low. These map directly to the input pins.

1. If JTAG is not used, TRSTN must be tied low.