ARRIA 10 AFE74xx XCVR 2x44210 JESD REFERENCE DESIGN USER GUIDE

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I. DESCRIPTION

Overview:

The "A10_AFE74xx_XCVR_2x44210_7p3728G.qar" is a reference design developed to target Arria10 EVM board to interface with AFE74xx through JESD protocol. It is a transceiver firmware and both the Rx and Tx section of firmware supports the JESD mode 2x44210 at lane rate 7.3728G.

Rx design description:

RX side of FW has *altera_jesd204b_rx* IP and *xcvr_jesd_rx* IP to get JESD data from the AFE74xx at lane rate 7.3728G lane rate. The design has a simple Rx transport layer specific to this mode (2x44210) that captures samples from the ADC, re-order the bits and give out 16 samples every link clock (2 samples per lane). The results can be verified using Signal Tap.

Tx design description:

TX side of FW has *altera_jesd204b_tx* IP and *xcvr_jesd_tx* IP to send digital data (Sine wave 10MHz) to the DAC through JESD interface and it operates at lane rate of 7.3728 G. The design has a simple Tx transport layer which generates sine and cosine samples by the DDS compiler in firmware. The generated samples are reordered as per the JESD mode (2x44210), 2 samples per lane, with 4 lane for I data and other four lanes for Q data and sends it to the *xcvr_jesd_tx* IP. The results can be verified using a scope or Spectrum analyzer.

Note: This version of the FW is a fixed line rate firmware and hence will work only at 7.3728G. For any other line rate the firmware needs to be recompiled for that specific line rate.

This document gives a brief on the compilation and verification process involved. Section II discusses on how to restore the project from .qar file and the compilation process involved. Section III discusses on how to get the data in Signal Tap and validate the same. Section IV discusses on generation of tone for DAC. Section V discusses the debug signals added in project.

Signals	Description	Direction
device_clk	reference clock from AFE74xx	
mgmt_clk	100MHz oscillator clock	
global_rst_n	Active Low User reset	Input
sysref	SYSREF Signal	input
tx_syncn	Tx Sync Signal	
rx_serial_data	Serial Data from ADC	
tx_serial_data	Serial Data to DAC	Output
rx_dataout	Transport Layer data output (16 samples for every link clock)	Ordered from the Dr
rx_somfout	SOMF aligned with rx_dataout	transport layer module
rx_validout	Data valid Signal aligned with rx_dataout	
Jesd204_tx_link_data	Transport Layer data out (16 samples for every link clock)	Output from the Tx transport layer module

Following are some of the important inputs and the output signals with their description. User can make use of these signals in their custom modules.

Jesd204_tx_link_valid	Valid signal of the transport layer data	
-----------------------	------------------------------------------	--

Note: Tx SYNC signal of the device routed to FMC is not connected to FPGA in the Arria10 EVM. Hence the SYNCB0CMOS of the device is bluewired to Arria10 EVM through J7 SMA connector.

In AFE74xx used for testing, the lower four SERDES lanes P & N pins of the JESD interface are swapped, hence Rx lane polarity inversion is implemented in the design to address that. Due to this, Rx lane polarity inversion constant given to the JESD IP module (csr_rx_lane_polarity) is '0x0F'. But on the Tx side no lane inversion is required hence Tx lane polarity inversion constant given to the JESD IP module (csr_tx_lane_polarity) is '0x0F'.

II. COMPILING QUARTUS PROJECT

1. Restore the Quartus project

Open Quartus 16.1. Click File -> Open and choose the qar file

"A10_AFE74xx_XCVR_2x44210_7p3728G.qar"

Click OK in the dialog box that pops up next

S Restore Archived Project	×
Archive name:	
f design\241018\Release\A10_AFE76xx_XCVR_2x44210_7p3728G.qar	
Destination folder:	
gn/241018/Release/A10_AFE76xx_XCVR_2x44210_7p3728G_restored	
Overwrite any existing files in the destination folder	
OK Cancel Help	

Quartus will restore the contents to A10_AFE74xx_XCVR_2x44210_7p3728G_restored folder in the same location as that of qar file. User can change the location or the name of the folder.

2. Compiling the project

In Quartus IDE (environment), go to Project Navigator window located left side. This will show the device for which the firmware was compiled and the hierarchy of Verilog modules used.

Tasks window right below the Project Navigator will list all the tasks involved in compiling a design. To compile the project, double click "Compile Design" and all the subtasks listed will be executed in sequence

This will generate a ".SOF file" in the following location

Relative path of the example design +

"\A10_AFE74xx_XCVR_2x44210_7p3728G _restored\prj\output_files"

🕥 Quartus Prime Standard Edition - C:/Soliton_Work/Chinna/4t4r txcvr ref desig	n/241018/Release/A10_AFE76xx_XCVR_2x44210_7	p3728G_restored/prj/jesd204b_	ed - jesd204b_ed 👘 📾
File Edit View Project Assignments Processing Tools Window	Help		Search altera.com
□ 🚾 🖬 🗲 🗅 🗊 🤊 C [jesd204b_ed	/ * * * © ► F K + © A	🌣 😘 🗢	
Project Navigator	Compilation Report - je	sd204b_ed	
Entity:Instance	Table of Contents	Flow Summary	
Arria 10: 10AX11552F45I15GE2	Flow Summary	< <filter>></filter>	
▲ A10_AFE76xx_2x44210_4T4R_REFDESIGN ^A B	Flow Settings Flow Elapsed Time Flow Elapsed Time Flow CS Summary Flow Log Analysis & Synthesis Flow Messages Flow Suppressed Messages	Flow Status Quartus Prine Version Revision Name Top-level Entity Name Family Device Timing Models Logic utilization (in ALMs) Total registers Total priot nemory bits Total priot nemory bits Total DSP Blocks Total DSP Blocks	Successful - Wed Oct 24 06:55:18 2018 16:10 Build 196 10/24/2016 SJ Standard Edition Jesd204b_ed A10_AFE75cs_2x44210_4T4R_REFDESiGN Arria 10 10AX115S2F45I1SGE2 Preliminary N/A 21256 30 0 12,916,784 0 8
		Total HSSI TX channels	8
		Total PLLs	10
Tasks Compilation *			
Task Time			
Compile Design 00:14:52			
Analysis & Synthesis 00:04:33			
99% Fitter (Place & Route) 00:10:19			
0% Assembler (Generate programming files) 00:00:00			
0% FimeQuest Timing Analysis 00:00:00			
0% EDA Netlist Writer 00:00:00			
Edit Settings			
Program Device (Open Programmer)			
* All Co All	Co Find. Co Find Next sed time is 00:02:02 1552F45IISGE2 are preliminary		

Once the SOF file is generated, proceed to next section. It will take 20 min approximately to compile the design

III. VALIDATING WITH AFE74xx

1. Configure ADC

- The reference clock from device should be stable before downloading firmware. So, the device has to be configured first before we program the board.
- Open AFE GUI (Version 1.8.5 RC4) and set values as shown in the below snapshot



• In AFE GUI press buttons 'init Script', 'Get Rx/Tx Dig path and JESD Config', 'LMK Config' & 'Run Complete Startup Sequence' in sequence

					AFE/6)	x				2	Broadd	ast 🦻 Reconnect
uick Start	Configuration	5 LMK0428	AFE76xx RX	AFE76xx TX	Low Level	/iew						USB Status
VM Name	AFE76xx EVM	1									ſ	Init. Get RX/TX Dig p and JESD Co
System CLH CLK Option Internal PL	CRate Ext DAC	CLK (MHz) R	DSA Sett	TX		Intern			Intern			LMK Run Complet Config Startup Sequer
nternal PLL MK_Ref(M) 122.88	Hz) Fref_(MHz) F	dac_(MHz) ID	DSA 0	RX Update Updat	DAC A	with NCO		-	with NCO	DACC	1	Reset, Read Chip ID Check Efuse
IV (Fdac/Fa	adc) 3 💌 Fadc_(M	Hz) 2949.12	Cross-Bar	Cnfg. Update		Interp.	ISD	SD	Interp.		2	Configure DDC Configure RX DSA
RX AB lecimation F	VTX Dig Path Confi Factor 8 (IQ) or 4 (F	teal)	1234567	RX OFF	DAC B	with NCO			with NCO	DAC D	4	Configure AGC and TDD Control
RXA	AB Data Type Sel	Complex 💌	Switch EN	Selection Cnfg.							5	Jesd_Sync_Source
cimation F	actor 8 (IQ) or 4 (F	Complex	lex): 0x 0C	DAC 1 23014567	ADCA	Decim. with			Decim. with	ADC C	6	Configure PLL
X_Interpola actor	ation 24_I	• 0	lex): 0x 30 lex): 0x C0	DAC 2 45230167 DAC 3 67234501		NCO	JES	JES	NCO		7	(JESD_TX)
	JESD Settings	s	ERDES Lane On/OF	F Update		Decim	0	O I	Decim		8	TX Data path and JESD_RX Co
DC 0/1 Path	44210/42220	/ 2 • RX SE	RDES TX (ADC)	SERDES RX (DAC)	ADC B	with	-		with	ADC D		Check Calibration Status
DC 2/3 DAC Path	44210/42220	/ 2 • RX	IX FF Bit[k] = 1, SERDES L	Dx FF Lane k is on.							D	AC] TX JESD
	(ecc. 10 ())	I. COMPRESS	Bit[k] = 0, SERDES I	Lane k is off.	1							Sync
X NCO#0	1700 TX RF N	CO 1700 RX	FBRX RX/FB NCO								SY	SREF Equal SY
X_NCO#1	0 TX BB N	CO 0 0F	F 💽 SPI contro	4							Co	nt M. Pu
X_NCO#2	0 Dual	For	help, refer to 'Config	guration/Notes for Q	uick Start"							Ungate Gate
X_NCO#3	0 Band [Cnfg. Enable Table	path jQ0 Ct	ip_ID EFUSE	STATUS	Status/Info 0 Display	8		PG Versi	PLL Loc Status	k .	Seq. Dum	p Mode "AFE76xxiPython
X ID's RX (0,1,2, 💌 TX ID's 1	X 0,1,2,3 •	in Version Done E	cone	ADC Calib			Clos All Pat	e es	Test Script 1	OFF	SupportScriptsVogF
RX NCO ID'S	0 TX NCO I	D's RF 41 CO Update	15		0					Test Script 2	Conve CFG for	rt to rmat "~\SupportScripts\ logFile_converted_t w_level_read.cfg"

• Press on the small folder icon in the 'AFE GUI' and load 'SYNC0CMOS' and 'DDC Ramp' config files

		AFE76xx			Broadcas	at 🧊 🏓
Start Configuration LMK0428 A	AFE76xx RX AFE76xx TX	Low Level View				
	1	and the second se			-	
Register Map 🛛 😁 🏷 🥳	55 55	Linked Update Mode Immed	sate	Sear	ch Next	
Register Name	Address Default Mode	Size Value 7 6 5 4 3 2	1 0 Field View			60.00
⊟ LMK04828	Choose or Enter Path of File	í.				X
2000						0
×002	I exas Instr	uments + AFE/bix_v1.8.5_rc4 + Configura	tion Files	• +• Search	Configuration Files	P
x004	Oranging and Manufalder				in . 10	0
x005	Organize • New folder				000 T L	
x006	A	Name	Date modified	Type	Size	
x00C	Pavorites	AFE 14 74 Charl ADC and DAC da	0.00 /2010 2.20 03.4	CEC ER-	00 K	
X00E	Desktop	AFE_14.7400ps_AUC and UAC.ctg	9/0/2010 3:25 PM	CPG File	80 K	
×100	Downloads	dac output with constant input.cfg	6/5/2018 3:04 PM	CFG File	19 K	В
x101	Recent Places	dacB original.cfg	6/5/2018 3:04 PM	CFG File	4 K	B
x103	HSDC Pro Installe	C DDC Ramp.cfg	2/28/2018 2:50 PM	CFG File	1 K	В
x104	HSDCPRO DEPO	C ddc Ramp_old.cfg	8/27/2018 5:48 AM	CFG File	1 K	в
x106	Tractation	C ddcy Bamp - off cfg	8/27/2018 5-47 AM	CEG File	1.6	8
x107	Ja Texas Instrument	init and a factor	6/E/2010 2:01 PM	CFC File	10.1	
x108	🍰 Remote Station 🛯	init config.crg	0/5/2018 3304 PW	CFG File	19 K	8
x109	ISDCPro Data	E LMK_configuration_14.7Gbps.cfg	9/5/2018 4:35 PM	CEG File	6 K	8
x10B	TSW14Jxx INI File	ImkConfig_7pSgbPs.cfg	6/5/2018 3:04 PM	CFG File	2 K	8
x10C	-	ImkConfig_10gbPs.cfg	6/5/2018 3:04 PM	CFG File	2 K	8
x10D	The libraries	ImkConfig 15gbPs.cfg	6/5/2018 3:04 PM	CFG File	2 K	в
x10E	Cibranes	E BBD adjustment of a	9/17/2018 #-45 PM	CEG File	1.6	R
x110	Documents	E CONCOCHOS -C-	10/33/3050 51.53	CEC EL-	14	
x111	J Music *	B SYNCOCMOS.ctg	10/22/2018 11:55	CFG File	1 K	5
x113	File na	me		* Custom	Pattern (*.cfo)	-
x114		(h)				
x115				OK	- Cance	tion 1
x116						100
x11/						
Register Description						
		* Block	Address W	rite Data	Read Data_Generic	
		6	x 0 x	0	× 0	
					[automa automa]	
		*	X	Vrite Register	Read Register	

• Press the 'SYSREF Cont M' button in AFE GUIs



- Download Firmware (Refer Section 2)
- Press on DAC SYNC button (highlighted in the snapshot below) in AFE GUI



With this step we should be able to see Ramp data from ADC and a clear tone from DAC

2. Programming Arria 10 development kit

Connect USB Blaster to Arria10 development kit. Go back to Quartus project, and double click Program Device in tasks window. This will open the programmer tool.

Click on Auto Detect and choose "10AX115S2E2" in the Select Device window and click OK

				[
Enable real-time I	ISP to allow	llasterii [USB-2] w background prog	Mode: ramming when a	JTAG vailable		Progress:			
▶ ¹⁰ Start		File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine
Auto Detect Delete Add File Change File Save File Add Device 1 ^N Up 1 ^N Up	•	Found devices w 10AX115R 10AX115R 10AX115S 10AX115S 10AX115S 10AX115S 10AX115S 10AX115S 10AX115S 10AX115S 10AX115S	ith shared JTAG #E2 #E5 1 2 2 2 2 2 2 2 2 2 2 2 5 3 3 5 3 5 5 3 5 5 5 5	D for device 1. Ple	ase select your	r device.			

Right click on "10AX115S2E2" in the JTAG chain and choose Edit-> Change File. Browse and select the .SOF file generated in previous section



Check the Program/Configure box and click start. Progress bar should start incrementing



3. Checking Results in Signal Tap

Once the development kit is programmed, user can view the results in Signal Tap which probes signals from the kit using USB blaster and JTAG interface. It can be opened from Quartus Tools-> SignalTap II Logic Analyzer

🕞 Qu	artus Prime Standard Edition - C:/Soliton_Work/Chinn	a/4t4	r txcvr ref design/241018/A10_AFE76xx_2x44	210_	ADC_DAC_INTEG/Proje	ct/prj/jesd204b_ed - jesd204b_ed	
Eile	Edit View Project Assignments Processing	Io	ols <u>W</u> indow <u>H</u> elp				Search altera.com
	■ + D D つ C [jesd204b_ed		Run Simulation Tool	٠	Q Q A Q S		
Project	Navigator Hierarchy Q I & × Entity:Instance	- Cr	Generate Simulator Setup Script for IP		:04b_ed iummary		
Arr	ia 10: 10AX115S2F45I1SGE2	0	Launch Design Space Explorer II		Filter>>		
-	A10_AFE76xx_2x44210_4T4R_REFDESIGN 📥	۲	TimeQuest Timing Analyzer		Status	Successful - Wed Oct 24 06:44:08 2018	
	sld_hub:auto_hub		Advisors	٠	us Prime Version	16.1.0 Build 196 10/24/2016 SJ Standard Edition	
	sld_signaltap:debug_signals_rx sld_signaltap:debug_signals_tx core_plt;esd_plt_inst icd204b pp_topsignals_tx	* *	C <u>h</u> ip Planner Design Partition Planner Netlist <u>V</u> iewers		on Name evel Entity Name f	jest2045_ed A10_AFE76xx_2x44210_4T4R_REFDESIGN Amia 10 10AX11552F45I15GE2	
Þ	T jesd204b_tx_topjesd_tx_DAC isd204b_tx_topjesd_tx_DAC Å reset_gen:u0	~?	SignalTap II Logic A <u>n</u> alyzer In-System Memor <u>y</u> Content Editor Logic Analyzer Interface Edito <u>r</u>		g Models utilization (in ALMs) registers pins	Preliminary 9,663 / 427,200 (2 %) 21715 51 / 960 (5 %)	
١١	•	01	In_System Sources and Probes Editor		virtual pins	0	
Tasks	Compilation 💌 🗏 🗇 🕈 🗙	33	SignalProbe Pins		plock memory bits	12,910,592 / 55,562,240 (23 %)	
	Task	-	ITAG Chain Debugger		DSP Blocks	0/1,518(0%)	
-	Compile Design		Fault Injection Debugger		HSSI TX channels	8/72(11%)	
× -	Analysis & Synthesis	· · · ·	System Debugging Tools	×	PLLs	10/144(7%)	
× -	Fitter (Place & Route)	-	IB Catalog				
× .	Assembler (Generate programming files)		Nios II Software Build Tools for Eclipse				
× .	TimeQuest Timing Analysis	*	Qsys				
×	EDA Netlist Writer						
	Edit Settings	1	Tel Scripts				
	Program Device (Open Programmer)		Customize Options License Setup				
•		0	Install Devices				

Signals which are currently probed are

Signals in Rx Instance:

- **rx_sync_n** Active low SYNC signal from *altera_jesd204b_rx* IP. If SYNC is established, this signal will be high
- sysref SYSREF signal to Base IP
- **somf[3]** SOMF Signal from *altera_jesd204b_rx* IP
- Jesd204_rx_link_data 256 bit link data from *altera_jesd204b_rx* IP (grouped into 8 lanes of 32 bit each)
- **rx_dataout** transport layer data out (16 samples of data for every link clock). User has to use rx_dataout along with rx_somfout and rx_validout
- **rx_somfout-** SOMF signal aligned with transport layer rx_dataout
- **rx_validout** Data valid signal aligned with transport layer rx_dataout

Signals in Tx Instance:

- **tx_sync_n** Active low SYNC signal to *altera_jesd204b_tx* IP. If SYNC is established, this signal will be high
- sysref SYSREF signal to Base IP
- jesd204_tx_pcs_data 256 bit pcs data from *altera_jesd204b_tx* IP (grouped to 8 lanes with 32 bit data for each lane)
- **ddsio**|fsin_0 & ddsio|fsin_1 The 16 bit output samples from each DDS compiler (see DAC wave form generation section).
- **jesd204_tx_link_valid** Data valid signal aligned with transport layer jesd204_tx_link_data.

Other signals can also be probed. Each time, signals are added/removed from signal tap, the project has to be compiled again

Following is the Signal Tap window. Hardware and Device tabs should be selected/listed properly. The Instance section lists both the Tx and Rx instances. Double clicking on any particular instance will display its corresponding signals.

tanc	e Man	hager:	🔊 🔍 🔳	Ready to a	cquire						×	JTAG Cha	n Configurati	on: JTAG read	ly	
ance	e		Sta	tus	Enabled	LEs: 13340	Memory: 871628	Small: NA	Medium: N	A Large: NA		Hardware	LISB-Blaster	11 (USB-11	-	Setu
2	debug	g_signa	als_tx Not	running	1	6842 cells	4481024 bits	NA	NA	NA		That Gittar C.	oob blaster	1000 1		Jocia
2	debug	g_signa	als_rx Not	running		6498 cells	4235264 bits	NA	NA	NA		Device:	@1: 10AT11	15S1 (0x02E06	DDD) -	can C
												>> SOF	Manager:	ig_viol	/jesd204b	_ed.sof
rigg	ger: 201	18/10/	24 03:58:20 #1					Lock mode:	🔐 Allow all char	nges 💌	Signal Conf	iguration:				
				No	ode			Data Enable	Trigger Enable	Trigger Condition						-
ype	Alias	s			Name			517	517	1 Basic AND	Clock con	e_pll:jesd_pl	_inst outclk_(0		
		sysre	ef					V	1		Data					
x_sync_n									V							
		jesda	204b_rx_top:jesd_rx_	ADC altera	jesd204b_ncu	jesd204 somf[3]	V	V	111	Sample d	epth: 8 K	 RAM typ 	e: Auto	_	•
		rx_va	alidout						V		Segm	ented: 2 4	K sample sea	emnts		÷
3		±	b_rx_top:jesd_rx_AD	C altera_jes	d204b_rx:u_je	esd204 jesd204_	rx_link_data[2550]	1	1	AND						E.A.
		rx_so	omfout					9			Nodes All	located: 🧿	Auto	Manual:	517	19
3		·	.sd_rx_ADC Transpor	rt_layer_AFE	76xx_2x442	rx:jesd_transport	1 rx_dataout[2550]		v	AND	Pipeline F	actor 0				
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											Туре:	Cor	tinuous			•
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											Nodes	Allocated: @	Auto	O Manual:	517	-
											171	the second				
											LY_I Reco	oro data disc	ontinuities			

If Hardware or device is not listed, click on Setup and choose the right port to which USB blaster is connected

Instance Manag	ger. 📉 😥 🔳	Ready to ac	quire			_			×	JTAG Chai	n Configuration: JTAG ready	×
Instance		Status	Enabled	LEs: 1334	40 Memory: 871628	Small: NA	Medium: NA	Large: NA		Hardware:	USB-Blasterii [USB-1]	Setup
🕄 debug_s	signals_tx	Not running		6842 cell	s 4481024 bits	NA	NA	NA				
🛃 debug_s	signals_rx	Not running		6498 cell	s 4235264 bits	NA	NA	NA		Device:	@1: 10AT115S1 (0x02E060DD) *	Scan Chain
rrigger: 2018, Type Alias 5 5 7 5 7 5 7 7 5 7 7 5 7 7 5 7 7 7 7	/10/24 035820 #1 sysref rx_sync_n esd204b_rx_topjesd rx_somfout ⊞sd_rx_ADC Tran	Nor I_rx_ADC altera_iv _ADC altera_jesd sport_layer_AFE7	de Name esd204b_ncu i204b_ncu_jei 76xx_2x442_r	jesd20 sd204]j xjesd_	Hardware Setup Hardware Setup Select a programming ha hardware setup applies o Currently selected hardw Available hardware item Hardware USB-Blasteril	rAG Settings ardware setup Inly to the curu are: No Harr Is USB-BI	to use when program ent programmer wind dware dware dware dware dware tware tware Port Local USB-1	ming devices. This	Add Hardwa	ing re Ivare Close	Anager: A g viol/jesd204 nstjoutcik_0 RAM type: Auto sample segments uto Manual: 517 nuous external_storage_qualifier Auto Manual: 517 timulites mi	
-	_											, '
🏓 Data	👼 Setup											

Select debug_signal_rx and Click on Run Analysis

e Ean Alew Fiolect	Processing Tools	Window	Help								Search altera	LCOM
B B つ C 単 66	▶ 🖏 🕜											
tance Manager: 🔯 😡	Ready to a	cquire						×	JTAG Chai	n Configuration: JTA	G ready	
ance	Status	Enabled	LEs: 13340	Memory: 871628	Small: NA	Medium: NA	A Large: NA		Hardware:	USB-Blasterii (USB-1	1 •	Setup.
debug signals tx	Not running	V	6842 cells	4481024 bits	NA	NA	NA					
debug_signals_rx	Not running	V	6498 cells	4235264 bits	NA	NA	NA		Device:	@1: 10AT11551 (0x	02E060DD) *	Scan Ch
igger: 2018/10/24 03:58:	20 #1				Lock mode:	🚅 Allow all chan	iges 🔻	Signal Cont	figuration:	Manager: 🚠 🔳	ıg_viol/jesd204	4b_ed.sof
	N	ode			Data Enable	Trigger Enable	Trigger Condition					
ype Alias		Name			517	517	1 Basic AND	Clock cor	e_pll:jesd_pll	_inst outclk_0		
sysref					1	1		Data				
rx_sync_n					1	V						
jesd204b_rx_t	op:jesd_rx_ADC altera_	jesd204b_rx:	u_jesd204 somf[3]		V	88	Sample o	lepth: 8 K	RAM type: Aut)	
rx_validout					7			Segm	ented: 2 4	K sample segments		*
Eb_rx_top:	jesd_rx_ADC altera_jes	d204b_rx:u_j	esd204 jesd204_	rx_link_data[2550]	7	1	AND	Nadas Al			al. Intern	[A]
rx_somfout					V	<u>v</u>		Nodes Al	located:	Vuto O Mani	at. 517	(V)
tsd_rx_AD	C Transport_layer_AFE	2x442	rx:jesd_transport	t1 rx_dataout[2550]		v	AND	Pipeline I	Factor: 0			-
								Storage	qualifier:			
								Type:	Con	tinuous		•
								Input p	ort: auto_stp	external_storage_q	alifier	
												*
								Nodes	Allocated: 🥹	Auto 🕖 Man	ual: 517	
								🗹 Rec	ord data disco	ontinuities		
								Dis:	able storage q	ualifier		

Transport layer data out for 2x44210, 7.3728G Lane Rate with Ramp test pattern is below.

🟸 Sign	nalTap I	Logic Analyzer	- [A10_AFE76xx_2x44210	0_4T4R_REFD	ESIGN.stp]*												Σ
<u>F</u> ile <u>F</u>	<u>E</u> dit <u>V</u>	iew <u>P</u> roject	Processing Tools	Window	<u>H</u> elp									Searc	h altera.c	com	1
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	debug	signals tx	Not running	V	6842 cells	4481024 bits	NA	NA	NA		na	ruware.	USD-Diasteri	ii [USB-1]		Setup	
2	debug	signals_rx	Not running	V	6498 cells	4235264 bits	NA	NA	NA		De	vice:	@1: 10AT11	15S1 (0x02E060	DD) 🔻	Scan Chai	ir
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-		rx_sync_n				SOMF from Ba	ase IP		_							^	
-		jesd204b_rx_to	op:jesd_rx_ADC altera_j	esd204b_rx:	u_jesd204 somf[3]]		J									ł
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	\vdash	±p:jes	sd_rx_ADC altera_jesd20	04b_rx:u_jes	d204 jesd204_rx_	link_data[191160]	OB680B69h	0B6A0B6Bh	COBECOBEDH	OBGEOBGEN A	087008	71h /	08720873h	08740875h	08760	0877h	l
	\vdash	·p:jes	so_rx_ADC attera_jeso2	04b_rx:u_jes	a204]Jesa204_fx_	link_data[159126]	OB680B69h	OBGAUBGBN	V DOBOCOBODA /		087008		08/208/3h	08740875h	08760	077h	l
	\vdash	⊡op.j	esd_rx_ADC[attera_]esd.	2040_fx:u_e	esd204[Jesd204_fx	Link_data[12796]	OBesoBesh	OBSAGBSB	ABODDING COL		087000		OB/20B/3h	08740875h	08760	Baab	l
		top.	jesd_rx_ADC[attera_jesc	12046_1X.U_	esd204]jesd204_n	k_link_data[9564]	OBesoBesh	ORCAORCRE	Accold E-01	A antitation V	087000		087208735	08740875h	08760	B77h	l
	\vdash	t x to	priesd or ADCIaltera ie	ed204b_rcu	iesd204]Jesd204_1	r link data[31.0]	OB680B60h1	OB6A0868b		iddasolc X	087005	71h Y	087208725	087408755	08760	B77h	l
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		⊡ sd rx AD	CITransport laver AFE	76xx 2x442	priesd transport1	In dataout[255_0]					_	Dela	iyed SOMF	OP			l
	\square		Transport laver AFE76	xx 2x442 rx	iesd transport11p	dataout[255_240]	(OB64h)	OB66h	OB68h	oB6Ab X	A-i0860	hΧ	OB6Eh	OB70h	087	2h	l
	\square		Transport laver AFE76	x 2x442 rx	iesd transport11	dataout[239224]	OB64h	OB66h	OB68h	oB6Ah X	A-00860	h Χ	OB6Eh	X oB70h	087	'2h) =	l
5		DC	Transport layer AFE76	x 2x442 rx	jesd transport1/r	dataout[223208]	OB64h	OB66h	OB68h	oB6Ah X	B-10860	h χ	OB6Eh	OB70h	087	2h	l
6		DC	Transport_layer_AFE76	xx_2x442_rx	:jesd_transport1[rx	dataout[207192]	OB64h	OB66h	OB68h	oB6Ah X	B-q0860	in X	0B6Eh	OB70h	087	'2h	l
5		DC	Transport_layer_AFE76	xx_2x442_rx	:jesd_transport1 n		OB64h	OB66h	OB68h	oB6Ah X	0860	h X	OB6Eh	OB70h	087	zh	l
6		DC	Transport_layer_AFE76	xx_2x442_rx	:jesd_transport1 n		0864h	OB66h	OB68h	OB6Ah X	0860	in X	OB6Eh	OB70h	<u>087</u>	'2h	l
6		DC	Transport_layer_AFE76>	xx_2x442_rx	:jesd_transport1 rx	_dataout[159144]	OB64h	OB66h	OB68h	OB6Ah X	D-i0860	h X	0B6Eh	OB70h	<u>087</u>	2h	l
6		DC	Transport_layer_AFE76>	xx_2x442_rx	:jesd_transport1 rx	_dataout[143128]	0864h	OB66h	OB68h	OB6Ah X	D-allo	in X	OB6Eh	OB70h	<u>087</u>	'2h	l
6		±DC	Transport_layer_AFE76>	xx_2x442_rx	:jesd_transport1 n	_dataout[127112]	OB65h	0867h	<u> 0869h</u>	<u>oB6Bh</u>	A-i1860	n X	086Fh	0871h	<u>087</u>	'3h	l
5		±DC	Transport_layer_AFE76>	x_2x442_rx	:jesd_transport1 n	_dataout[11196]	OB65h	0B67h	(<u>0869h</u>)	OB6Bh X	A-allo	n X	0B6Fh	0B71h	<u>087</u>	'3h	l
6		AD	C Transport_layer_AFE	76xx_2x442	_rx:jesd_transport1	rx_dataout[9580]	OB65h	OB67h	COB69h	OB6Bh X	B-ibset	h X	0B6Fh	OB71h	<u>087</u>	'3h	l
5		±AD	C Transport_layer_AFE	76xx_2x442	_rx:jesd_transport1	rx_dataout[7964]	OB65h	0867h	X OB69h	OB6Bh	B-adBet	n X	0B6Fh	0B71h	<u>087</u>	'3h	l
-		±AD	C Transport_layer_AFE	76xx_2x442	_rx:jesd_transport1	rx_dataout[6348]	OB65h	OB67h	X oB69h	OB6Bh X	OB6D	n X	OB6Fh	<u>0871h</u>	(<u>087</u>	'3h	l
-		±AD	C Transport_layer_AFE	76xx_2x442	_rx:jesd_transport1	rx_dataout[4732]	OB65h	0867h	X oB69h	OB6Bh X	0860	n X	0B6Fh	X <u>0871h</u>	(<u>087</u>	<u>'3h</u>	l
-		•AD	C Transport_layer_AFE	76xx_2x442	_rx:jesd_transport1	rx_dataout[3116]	OB65h	0867h	X oB69h	OB6Bh X	D-idBet	n X	0B6Fh	X 0871h	(<u>087</u>	<u>'3h</u>	l
1			DC Transport_layer_AFE	E76xx_2x442	2_ncjesd_transport	1 rx_dataout[150]	(OB67h	X <u>0869h</u>	OB6Bh X	D-allo	n_X	0B6Fh	X <u>0B71h</u>	(<u>087</u>	<u></u>	ſ

The transport layer is implemented only for the mode 2x2RX_44210.

Octet	1	2	3	4			
Lane 0	A-	A-	·i1				
Lane 1	A-	q0	A-q1				
Lane 2	B-	·i0	B-i1				
Lane 3	B-	q0	B-q1				
Lane 4	C-	·i0	C-i1				
Lane 5	C-	q0	C-q1				
Lane 6	D	·iO	D-i1				
Lane 7	D-	D-q11					

From the ADC datasheet, the sample format of JESD mode 2x44210 is as follows

Note: The samples specified as A & B are from one device and samples C & D from the other.

User should take the transport layer data along with SOMF (Start of Multi-frame) "rx_somfout" signal and rx_validout signals. These signals are in alignment with transport layer rx_dataout signal

rx_dataout follows the following sequence for 2x2Rx_44210

• The first link clock on the rising edge of rx_somfout, rx_dataout signal contains two 16 bit samples for each channel, with samples as [A-i0, A-q0,...,D-q0] on the MSB 128 bits with A-i0 as MSB and [A-i1,A-q1,...,D-q11] on the LSB 128 bits with A-i1 in MSB.

Similarly select the TX instance 'debug_signal_tx' and Click on Run Analysis

🟸 SignalT	ap II Logic Analyzer - [A10	_AFE76xx_2x4421	0_4T4R_REFD	ESIGN.stp]*										
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🕄 deb	bug_signals_rx	Not running	V	6498 cells	4235264 bits	NA	NA	NA			Device:	@1: 10AT115	51 (0x02E060DD)	 Scan Chain
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	tx syncn													
	□04b tx top;jesd	tx DAClxcvr ies	sd tx:i0 xcvr	iesd txliesd204	tx pcs_data[2550]									
	+top;jesd t	x DAClxcvr iesd	txi0 xcvr ie	sd txliesd204 tx	pcs_data[255224]	(748B2A84h)	D8A31C96h	D9C63FB4h	6BF01ADBh	CB1B3206	ih X F54393	30h X 5064605	5h X 1F795970h)	(FD7F627Eh)
5	top:jesd t	x DAC xcvr jesd	tx:i0 xcvr je	sd txljesd204 tx	pcs_data[223192]	(E9345F20h)	D358E847h	87722C67h	(0B7F907Ah)	F17CD97	h 776C60	76h 804F5D5	Fh (6229553Dh)	(84FE4014h)
6	top:jesd t	x DAC xcvr jesd	tx:i0 xcvr je	sd txjesd204 tx	pcs_data[191160]	748B2A84h	D8A31C96h	D9C63FB4h	6BF01ADBh	CB1B3206	ih 🛛 F54393	30h X 5064605	5h (1F795970h)	FD7F627Eh
6	top:jesd_t	x_DAC xcvr_jesd	tx:i0_xcvr_je	sd_tx jesd204_tx	pcs_data[159128]	E9345F20h	D358E847h	87722C67h	OB7F907Ah	F17CD97	h 776C60	76h 804F5D5	Fh (6229553Dh)	84FE4014h
5	+top:jesd_	tx_DAC xcvr_jesc	d_tx:i0_xcvr_j	esd_tx jesd204_t	x_pcs_data[12796]	748B2A84h	D8A31C96h	D9C63FB4h	6BF01ADBh	CB1B3206	ih (F54393	30h 5064605	sh (1F795970h)	FD7F627Eh
5	x_top:jesd	tx_DAC xcvr_jes	d_tx:i0_xcvr	jesd_tx jesd204_	tx_pcs_data[9564]	E9345F20h	D358E847h	87722C67h	OB7F907Ah	F17CD97	h 776C60	76h 804F5D5	Fh (6229553Dh)	84FE4014h
6	x_top:jesd	tx_DAC xcvr_jes	d_tx:i0_xcvr	jesd_tx jesd204	tx_pcs_data[6332]	748B2A84h	D8A31C96h	D9C63FB4h	6BF01ADBh	CB1B3206	ih F54393	30h 5064605	sh (1F795970h)	FD7F627Eh
6	tx_top:jes	d_tx_DAC xcvr_je	sd_tx:i0_xcvr	jesd_tx jesd204	tx_pcs_data[310]	E9345F20h	D358E847h	87722C67h	OB7F907Ah	F17CD97	h 776C60	76h 804F5D5	Fh (6229553Dh)	84FE4014h
6	□ Transport_laye	r_AFE76xx_2x44	2_tx:jesd_trar	nsport1 jesd204_	tx_link_data[2550]									
6	ort_layer_	AFE76xx_2x442_	tx:jesd_trans	port1 jesd204_tx	link_data[255224]	06321BCBh	309343F5h	55606450h	(7059791Fh)	7E627FFD	h 7DE178	20h 6EE5627	1h (5323416Dh)	(2DD018E3h)
6	ort_layer_	AFE76xx_2x442_	tx:jesd_trans	port1 jesd204_tx	link_data[223192]	(7FD97CF1h)	766C6C77h	SFSD4F80h	(3D552962h)	1440FE84	h E8D3D3	CEN CO14AE3	2h 9EAE91FDh	(887C8272h)
5	ort_layer_/	AFE76xx_2x442_	tx:jesd_trans	port1 jesd204_tx	link_data[191160]	06321BCBh	(309343F5h)	(55606450h)	(7059791Fh)	7E627FFD	h 7DE178	20h (6EE5627	1h (5323416Dh)	(2DD018E3h)
5	ort_layer_	AFE76xx_2x442_	tx:jesd_trans	port1 jesd204_tx	link_data[159128]	(7FD97CF1h)	766C6C77h	SF5D4F80h	(3D552962h)	1440FE84	h E8D3D3	CEh CO14AE3	2h 9EAE91FDh	(887C8272h)
6	±port_layer	_AFE76xx_2x442	_tx:jesd_tran	sport1 jesd204_t	<pre>k_link_data[12796]</pre>	06321BCBh	309343F5h	55606450h	(7059791Fh)	7E627FFD	h 7DE178	20h 6EE5627	1h (5323416Dh)	(2DD018E3h)
6	sport_laye	r_AFE76xx_2x44	2_tx:jesd_tra	nsport1 jesd204_	tx_link_data[9564]	(7FD97CF1h)	766C6C77h	SF5D4F80h	(3D552962h)	1440FE84	h E8D3D3	CEN CO14AE3	2h 9EAE91FDh	(887C8272h)
-	sport_laye	r_AFE76xx_2x44	2_tx:jesd_tra	nsport1 jesd204_	tx_link_data[6332]	06321BCBh	(309343F5h)	55606450h	(7059791Fh)	7E627FFD	h X 7DE178	20h (6EE5627	1h (5323416Dh)	(2DD018E3h)
-	nsport_lay	er_AFE76xx_2x4	42_tx:jesd_tr	ansport1 jesd204	_tx_link_data[310]	(7FD97CF1h)	(766C6C77h)	SF5D4F80h	(3D552962h)	1440FE84	h E8D3D3	CEh CO14AE3	2h (9EAE91FDh)	(887C8272h)
*	sd_tx_DAC Transpo	ort_layer_AFE76x	x_2x442_tx:je	esd_transport1 je	sd204_tx_link_valid									
6	DAC Transport	t_layer_AFE76xx_	2x442_tx:jes	d_transport1 dds	ddsi0 fsin_o[150]	<u>3093h</u>	5560h	7059h	7E62h	7DE1h	6EE5	h 🛛 5323h	2DDoh	O33Ah
6	DAC Transport	Layer_AFE76xx_	2x442_tx:jes	d_transport1 dds	ddsi1 fsin_o[150]	43F5h	6450h	791Fh	(7FFDh)	7820h	6271	h 416Dh	18E3h	ED79h

- 'jesd204_tx_pcs_data' shows the 256 bits of data which will be sent to DAC serially, It is grouped as 32 bit buses so that each bus corresponds to data of a single lane.
- 'jesd204_tx_link_data' shows the 256 bits of data which is formed by rearranging the data generated by the DDS module so that it suits 2x4421 mode of DAC.

It is grouped as 32 bit buses so that each bus corresponds to data of a single lane.

• 'ddsi*|fsin_0' shows the 16 bits of sample data (sine wave of 10 MHz) which is generated by the DDS module.

It is possible to view the output of each DDS as a 10 MHz wave, within the chipscope.

The procedure:

1. Right click -> Bus Display Format -> Signed decimal in Two's Complement

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Image: Instructure Image:		·		±x_top	p:jesd_tx_E	AC xcvr_je	sd_tx:i0_xcvr	jesd_tx jesd204	_tx_pcs_data[6332]	(FC807880	hX748B2A84I	XD8A31C96h	XD9C63FB4h	X6BF01ADBhX	B1B3206h (Fs	<u>5439330h</u>	50646055h	X1F795970h	FD7F627Eh)
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B		·	<u>[]]</u>	Fransport	_layer_AFE	76xx_2x44	2_tx:jesd_trai	nsport1 jesd204_	tx_link_data[2550]			V	·					V	
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• We can plot the samples of any dds instance ouput(fsin_o) and we should get a sine wave as follows(plot of 'ddsi0|fsin_o[15:0]')

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4. Spectrum Analyzer

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•										11					+	

The frequency as seen in the Spectrum Analyser:

Note: As NCO frequency is set to 1.7G and the generated frequency is 10 MHz, we see a tone from the DAC at NCO Freq+ Generated frequency i.e. 1.71G

IV. DAC wave form generation

This FW (and Transport Layer) has been made specifically for 2x4421 mode. A tone is generated within the FW. This tone is being sent continuously (free-running) to the DAC from the FPGA.

1. Generation of Sinewave:

- A DDS Compiler is being used within the FW in order to generate the tone. In this design, a Sine wave of frequency of 10 MHz is being generated.
- The DDS compiler will require a sampling clock as input. In this firmware, the sampling frequency of the DDS compiler is 184.32 MHz
- For every link clock cycle we need to send 32 bits of data to the *altera_jesd204b_tx* IP. Hence we use 2 instances of DDS compiler modules to generate 2 waves of 10 MHz each. However

each instance is offset by an equal value (for this mode the phase offset is one-half of the output wave i.e., 10/2 = 5Mhz) such that in each link clock 2 samples of a 10 MHz Stone is generated. All two samples are concatenated (jesd204_tx_link_data signal) and given as an input to the *altera_jesd204b_tx* IP.

- The concatenated output (jesd204_tx_link_data) consists of four 16-bit samples. In this mode 2 samples are provided for each lane. Hence the output of the transport layer is a 256 bit bus, which contains sixteen 16-bit samples for 8 lanes.
- The DAC sampling rate for this lane rate (7.372G) is 368.64 Msps/ Channel. Each DDS Compiler instance generates a 10 MHz wave w.r.t a sampling rate of 184.32 MHz Therefore when we combine the outputs of two such instances for a single cycle, a tone of 10 Mhz is generated for a sampling rate of 368 Msps.

2. Changing the Sine wave frequency:

- In order to change the generated Sine wave frequency, we need to change the phase offset and phase increment values.
 - (Calculation has been presented for 20 MHz sine wave case)
 - \circ Phase offset = [2^Phase width /(Sampling frequency/Required frequency)]/2

- = [4294967296/18.432]/2
- = 233016888.889/2
- = 116508444.444

By rounding off to the nearest integer we get 116508444 which is 6F1FC71C in hexadecimal.

- Phase increment = 2^Phase width /(Sampling frequency/Required frequency)
 - = 2^32/(184.32/10)
 - = 4294967296/18.432
 - = 233016888.889

By rounding off to the nearest integer and making it a multiple of phase offset, we get 23301689 which is DE38E38 in hexadecimal.

For more detailed information about the DDS compiler module please refer to the Altera document available at the following link:

ups://www	v.ane	ra.com/en		S/puis/merature/ug/
IP Parameter Editor - dds.gsy	s* (C:\Soliton	Work\Chinna\4t4r txcvr ref des	ign\24101	8\Release\A10_AFE76xx_XCVR_2x44210
ile Edit System Generate Vi	ew Tools He	p		
N Parameters			d D	Details 💠 🔛 Block Symbol 🔅 🔄 🗗 🗖
System: dds Path: nco ii 0				
NCO				Show signals
altera_nco_i		De	etails	nco ii D
			*	
Architecture Frequency Opti	ional Ports S10	Optimization	_ 1	clk out
* Precisions				cik fsin_o fsi
Phase Accumulator Precision:	32	bits		reset n out_valid
Angular Resolution:	16	bits		in in in in its in the interview of the
Magnitude Resolution:	16	bits		ciken ciken
Phase Dithering				phi_inc_(31.0) phi_inc_i
* Generated Output Frequ	ency Parame	iers		phase_mod_(31.0) phase_mod_i
Clock Rate:	184.32	MHz	_	a
Desired Output Frequency:	10.0	MHz		
Phase Increment Value:	233016889			
Real Output Frequency:	10.0	MHz		
				🐻 Presets 🔅 🗕 🗖 🗖
Frequency Domain Time Doma	in		- 4	Presets for nco_i_0
Magnitude (dB)				×
°				Project
-20				Library
-40				-No presets for NCO 16.1
-60			-	
Messages 83				
Type Path N	ressage			
				Apply Update Delete New
			,	
Errors, 0 Warnings				Generate HDL Finish

https://www.altera.com/en_US/pdfs/literature/ug/ug_nco.pdf

V. STATUS LEDS

Few signals added for debugging are listed below,

link_clk_led: This signal indicates if the link clock (lane rate/40 clock) from ADC is available or not. A signal which toggles for every 160ms, derived from link clock is connected to this LED(D7).

rx_altsyncn_led: This signal refers to the SYNC out from *altera_jesd204b_rx* IP and is given to LED D6 on board. It will be ON if SYNC is lost. Under normal process, this LED will be OFF. **tx_syncn_led:** This signal refers to the SYNC input to *altera_jesd204b_tx* IP and is given to LED D9 on board. It will be ON if SYNC is lost. Under normal process, this LED will be OFF

Apart from the above two LEDs, few other signals are assigned to LED mainly to prevent logic deletion by Fitter tool and it can be ignored

Note: Both the LEDs are active low