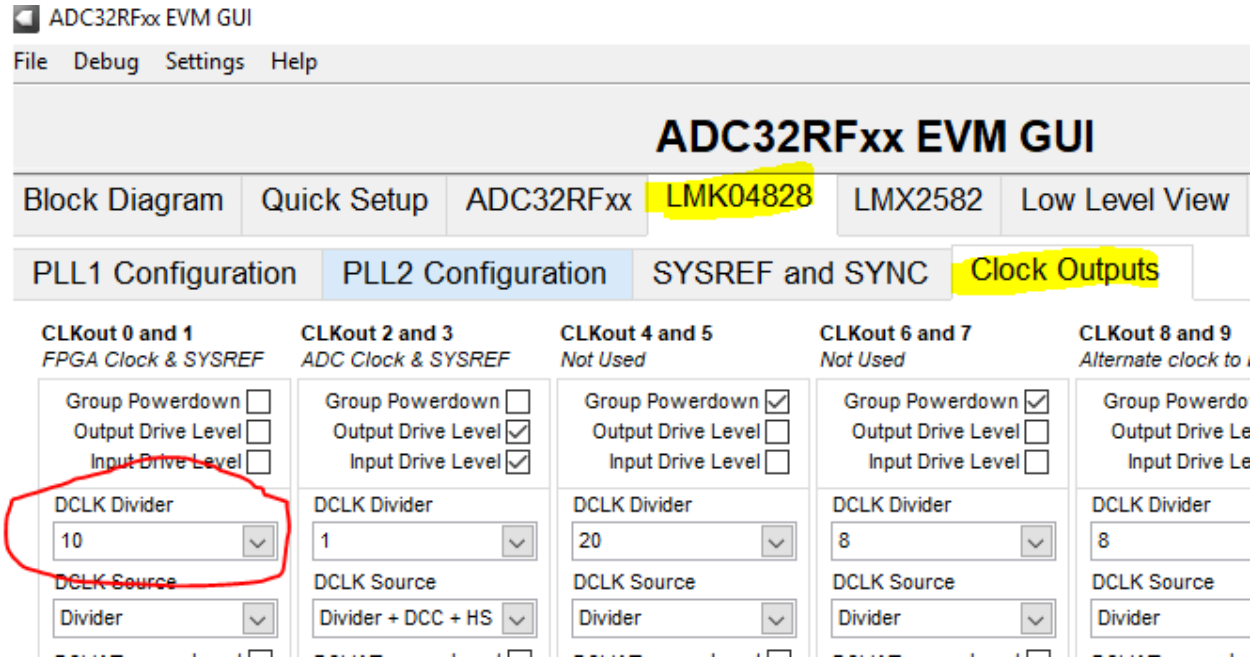
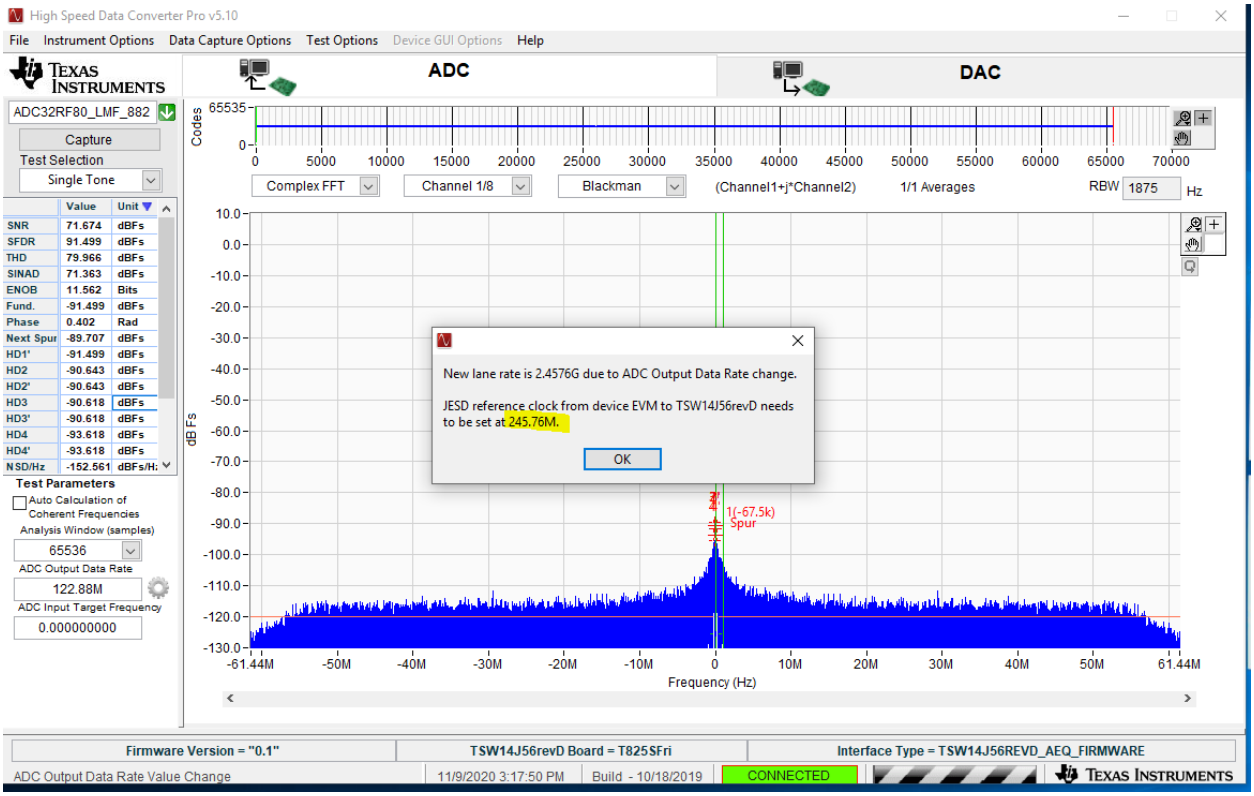
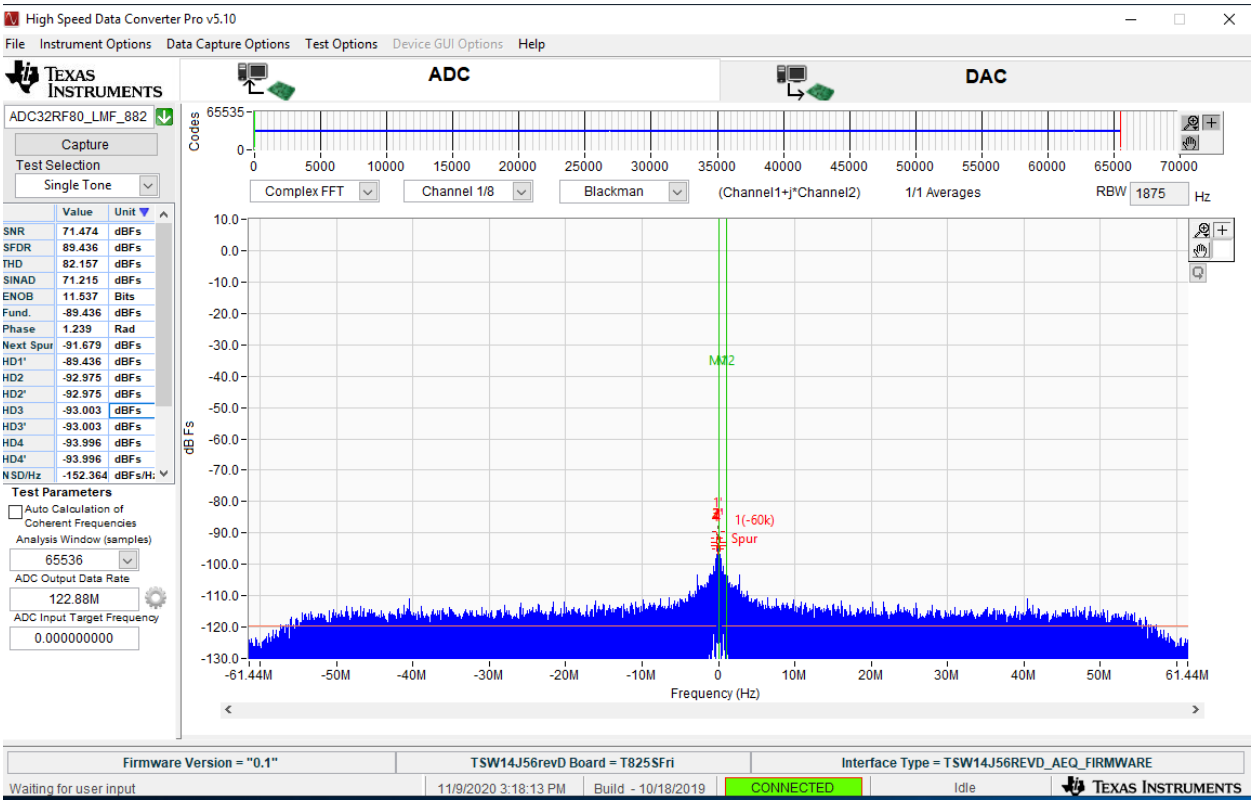

ADC32RFxx EVM GUI
File Debug Settings Help
ADC32RFxx EVM GUI
Block Diagram
Quick Setup
ADC32RFxx
LMK04828
LMX2582
Low Level View
PLL1 Configuration
PLL2 Configuration
SYSREF and SYNC
Clock Outputs
CLKout 0 and 1
FPGA Clock & SYSREF
CLKout 2 and 3
ADC Clock & SYSREF
CLKout 4 and 5
Not Used
CLKout 6 and 7
Not Used
CLKout 8 and 9
Group Powerdown
Output Drive Level
Input Drive Level
DCLK Divider
10
1
20
8
8
DCLK Source
Divider
Divider + DCC + HS
Divider
Divider
Divider


High Speed Data Converter Pro v5.10
File Instrument Options Data Capture Options Test Options Device GUI Options Help
Texas Instruments
ADC
DAC
ADC32RF80_LMF_882
Capture
Test Selection
Single Tone
Value Unit
SNR 71.674 dBFs
SFDR 91.499 dBFs
THD 79.966 dBFs
SINAD 71.363 dBFs
ENOB 11.562 Bits
Fund. -91.499 dBFs
Phase 0.402 Rad
Next Spur -89.707 dBFs
HD1' -91.499 dBFs
HD2 -90.643 dBFs
HD2' -90.643 dBFs
HD3 -90.618 dBFs
HD3' -90.618 dBFs
HD4 -93.618 dBFs
HD4' -93.618 dBFs
NSD/Hz -152.561 dBFs/Hz
Test Parameters
Auto Calculation of Coherent Frequencies
Analysis Window (samples)
65536
ADC Output Data Rate
122.88M
ADC Input Target Frequency
0.000000000
Codes
Complex FFT
Channel 1/8
Blackman
(Channel1+j*Channel2)
1/1 Averages
RBW 1875 Hz
dB FS
New lane rate is 2.4576G due to ADC Output Data Rate change.
JESD reference clock from device EVM to TSW14J56revD needs to be set at 245.76M.
OK
1(-67.5k) Spur
Frequency (Hz)
Firmware Version = "0.1"
TSW14J56revD Board = T825SFri
Interface Type = TSW14J56REVD_AEQ_FIRMWARE
ADC Output Data Rate Value Change
11/9/2020 3:17:50 PM
Build - 10/18/2019
CONNECTED
Texas Instruments


High Speed Data Converter Pro v5.10
File
Instrument Options
Data Capture Options
Test Options
Device GUI Options
Help
Texas Instruments
ADC
DAC
ADC32RF80_LMF_882
Capture
Test Selection
Single Tone
Value
Unit
SNR 71.474 dBFs
SFDR 89.436 dBFs
THD 82.157 dBFs
SINAD 71.215 dBFs
ENOB 11.537 Bits
Fund. -89.436 dBFs
Phase 1.239 Rad
Next Spur -91.679 dBFs
HD1' -89.436 dBFs
HD2 -92.975 dBFs
HD2' -92.975 dBFs
HD3 -93.003 dBFs
HD3' -93.003 dBFs
HD4 -93.996 dBFs
HD4' -93.996 dBFs
NSD/Hz -152.364 dBFs/H
Test Parameters
Auto Calculation of Coherent Frequencies
Analysis Window (samples)
65536
ADC Output Data Rate
122.88M
ADC Input Target Frequency
0.000000000
Codes
65535
0
0 5000 10000 15000 20000 25000 30000 35000 40000 45000 50000 55000 60000 65000 70000
Complex FFT
Channel 1/8
Blackman
(Channel1+j*Channel2)
1/1 Averages
RBW 1875 Hz
dB Fs
10.0 0.0 -10.0 -20.0 -30.0 -40.0 -50.0 -60.0 -70.0 -80.0 -90.0 -100.0 -110.0 -120.0 -130.0
M2
1
1(-60k)
Spur
-61.44M -50M -40M -30M -20M -10M 0 10M 20M 30M 40M 50M 61.44M
Frequency (Hz)
Firmware Version = "0.1"
TSW14J56revD Board = T825SFri
Interface Type = TSW14J56REVD_AEQ_FIRMWARE
Waiting for user input
11/9/2020 3:18:13 PM
Build - 10/18/2019
CONNECTED
Idle
Texas Instruments