**AFE JESD204C**

**3. Physical Layer Error**

The AFE79xx devices have two SerDes macros. Each SerDes macro is composed by a STX block with four transmitter lanes, a SRX block with four receiver lanes, and a common PLL block for STX and a common PLL block for SRX. The two SerDes macro provides total of eight SerDes transceiver lanes. The SerDes transmitters, or STX, transmits the serialized JESD204 data streams from the ADC and DDC logics to the ASIC/FPGA. The SerDes receivers, or SRX, receives the serialized JESD204 data streams from the ASIC/FPGA devices to the DAC and DUC logics. The following shows the general block diagram for the SerDes transceivers. Within each SerDes macro, two consecutive STX lanes or two consecutive SRX lanes can be enabled or disabled independently to optimize the power dissipation. For instance, STX1 and STX2 can be powered down together.

During the JESD204 operation, the SerDes block can detect errors and notify the user physical layer issues. The following error reporting’s are available:

**SerDes Receiver Loss of Signal (LOS):**

* This detector of this error is located for each SerDes receiver SRX ports (SRX1 to SRX8). Each SRX has a dedicated alarm.
* This error is triggered when the SRX port is in electrical idle state or has very weak signal input.
* Related C Functions: getJesdRxMiscSerdesErrors()

**SerDes PLL Unlock:**

* Besides the on-chip PLL, there is a dedicated on-chip SerDes PLL to provide all the necessary clocking for the SerDes block. This error is triggered when SERDES Rx/Tx PLL losses lock.
* Related C Functions: getJesdRxMiscSerdesErrors()

**SerDes Receiver FIFO Error:**

* Depending on the encoding type of the JESD204C usage, the SerDes block either operates at a rate close to 8B/10B or 64B/66B. To handle various encoding rates and to be able to hand off the data optimally to the JESD204C block, the design includes a FIFO in between the SerDes block and the JESD204C block.
* The SerDes block and the JESD204C block operates in different clock domain to handle various encoding rates. The FIFO in between the blocks absorbs the delay in data hand-off between the two blocks.
* The write-to-FIFO process is where the SerDes hands off the data output to the JESD204 block. This rate can be generically classified as FIFO\_WRITE\_CLK, and is derived from the SerDes SRX lanes and associated CDR clock. The read-from-FIFO process is where the JESD204 block reads the data from the FIFO. The JESD204 block reads from the FIFO and operates at a rate that is generically called FIFO\_READ\_CLK.
	+ FIFO error occurs whenever the FIFO\_WRITE\_CLK and/or FIFO\_READ\_CLK are either missing or have mismatch in clock rate.
	+ FIFO error can be cleared through the forced JESD204 RX block reset, assuming both FIFO\_WRITE\_CLK and FIFO\_READ\_CLK are stable.
	+ The following C function access the FIFO errors: getJesdRxLaneFifoErrors()

**Link and Lane Errors**

The AFE can detect link and lane errors on the DAC JESD204C RX logic. Please see Table 1 for the summary of the error detections.

**Table 1. AFE Link and Lane Error Detections**



**4.2.1 8B/10B Errors (8B/10B Encoding Specification Only)**

* **Disparity error**: the received code group exists in the 8b/10b decoding table, but is not found in the proper column to the current + or – running disparity. The 8b/10b encoding scheme utilizes disparity to keep the number of zero bits and number of one bits to 1:1 ratio and maintains DC balance on the physical SerDes line. Typically, for every negative disparity (i.e. four zeros and six ones) code, there follows a positive disparity (i.e. six zeros and four ones) code. There are other exceptions for completely balanced code (i.e. Five zeros an five ones). The error occurs when the disparity sequence received is not within the rules of the 8b/10b encoding.
* **Not-in-table error**: the received code group is not found in the 8b/10b decoding table for either disparity. With 8-bit word, there are 28 or 256 bit combinations. This is translated into 10-bit word, which has 210 or 1024 bit combinations. When a not-in-table error occurs, this is usually a true bit error since the detected word lies within the 768 unused bit sequences.

Error Handling:

* If error occurs, please check the JESD204C TX logic device (i.e. FPGA or ASIC) to see if it is initialized correctly with proper 8b/10b coding logics running. Uninitialized 8B/10B coding logic may result such error.
* Typically, both 8b/10b not-in-table and 8b/10b disparity occur simultaneously, and indicate general bit error due to the SerDes signal conditioning. This raises the need to improve signal integrity through use of equalizer, for example.
* If only 8b/10b disparity occurs, the error may lead to the 8b/10b logic in the JESD204C IP not being reset properly.
* Probe the SerDes lines with high speed scope to check the eye diagram for SerDes signal quality. PRBS pattern such as PRBS9 may be run over period of time for bit error check.
* Check if the SRX of the AFE80xx are detecting any bit errors. Re-adapt the SRX of the AFE80xx and adjust the signal integrity settings (i.e. FIR settings from STX of the FPGA or ASIC) accordingly.

**4.2.2 Code Group Synchronization Error (8B/10B Encoding Specification Only)**

Per JESD204C Section 8, consecutive 8B/10B disparity error or Not-In-Table errors will cause loss of link synchronization. Upon link synchronization, the JESD204C link will go through code group synchronization (CGS) which involves the JESD204C RX IP to detect the handshaking CGS code, or /K/ or K28.5 code. If the JESD204C RX IP cannot recognize the code or unable to establish link synchronization, the error will occur. This error is cleared when the link has been re-established.

* Code group synchronization (CGS) is achieved when the lane has received four consecutive /K/ (K28.5) characters successfully after asserting a synchronization request (~SYNC) and then another four valid character (i.e. non-/K/ characters that are valid in the 8B/10B coding) s after de-asserting the synchronization request. Basically, the lane alignment is complete at this point and the data is being buffered until frame alignment completes.
* If three invalid characters are received within a certain amount of time, code group synchronization would be lost.
* This would trigger the code group synchronization error.

Error Handling:

* If error occurs, please check the JESD204C logic device at either FPGA or ASIC to see if the logic device is initialized correctly with proper CGS state machine running
* Probe the SerDes line with high speed scope to see if the actual /K/ are detected with sufficiently good eye opening.
* Run link layer testing to check for validity of the /K/ CGS patterns
* Check if the SRX of the AFE80xx are detecting any bit errors. Re-adapt the SRX of the AFE

**4.2.3 Elastic Buffer Mismatch (8B/10B Encoding Specification Only)**

Unexpected control character: after the code group synchronization with /K/, the first character received is not the expected /R/ character.

**DAC JESD Page**

|  |  |  |
| --- | --- | --- |
| **Register** **Address** | **Register** **Information** | **Register Description** |
| 0xE9, bit[6] | Match\_Specific | – If set to 1b’0, the JESD204C RX buffer will start buffering with the first non-/K/ value and ignore match control character. Programming match\_specific to 1b’0 should not be used unless for debugging purpose – If set to 1b’1, the JESD204C RX buffer will start buffering only with /R/ character, immediately followed by /K/ after the completion of CGS |
| 0xE9, bit[7] | Match\_CTRL | – When set to 1b'0 the match character is a DATA character. – When set to 1b'1 the match character is a CONTROL character (/R/) instead of a DATA character. |

Error Handling:

* If error occurs, please check the JESD204C logic device to see if it is set correctly to subclass 1 mode as oppose to unsupported subclass 0 mode.
* Check with high speed scope to see if the actual /R/ is detected after the /K/ characters in the CGS.
* Set match\_specific to 1b’0 to see if the link establishment can proceed.
* Check if the SRX are detecting any bit errors. Re-adapt and adjust the signal integrity settings accordingly.

**4.2.4 Elastic Buffer Overrun (Common Specification)**

This is the elastic buffer overflow within the JESD204C RX IP. This is either due to incorrect configuration of RBD or very large lane-skew beyond the buffer size.

**4.2.5 Link Configuration Error (8B/10B Encoding Specification Only)**

* The frame alignment block of the JESD204C RX IP performs the initial frame synchronization, verification of the link configuration parameters, and frame alignment monitoring.
* When the initial lane alignment sequence arrives in this block, the first non-/K/ character is marked as the first octet of the first frame. The link configuration data is expected to arrive in the second multiframe. This block verified that the JESD204C TX lanes are programmed with the same configuration as the JESD204C RX lane.
	+ Any mismatches in the configuration parameter would trigger the link configuration error.
	+ Link configuration data is expected to arrive on the second multiframe of the initial lane alignment sequence. Basically the second /R/ indicates the ILAS.
	+ Each lane should have unique lane ID that is tied to the physical lane.
	+ Correct programming of the ILAS configuration are needed for both side of the JESD204C link (i.e. ASIC/ FPGA and DAC logic) in order for the ILAS check to be successful.

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**Figure 4-5. Illustrating ILAS After /K/ and /R/ Characters (JESD204C Figure 5)**

Error Handling

* If link cannot be established, try to ignore ILAS check in SYNC\_REQUEST to check if the JESD204C link can be established properly.
* Check the ASIC/FPGA ILAS setting and sequence are set correctly. Both the DAC JESD204C RX IP parameters and the ASIC/FPGA parameters much be set the same.
* Probe the SerDes line with high speed scope to trigger on first non-K28.5 character to decode the ILAS sequence. Go through the sequence to see if the octets are properly replaced for ILAS.
* Run link layer test to test for ILAS sequence.

**4.2.6 Frame and Multiframe Alignment Error (8B/10B Encoding Specification Only)**

Section 8.4.4 of the JESD204C specification defines the frame and multiframe alignment errors.

*Frame alignment is monitored via alignment characters, which are inserted by the transmitter under certain conditions at the end of a frame. The receiver resynchronizes its frame to the alignment characters after checking that their reception is not likely to have been caused by a bit error on the lane.*

*Resynchronization will require repeated reception of a valid alignment character at the same unexpected position in the frame.*

*The alignment character shall be a frame alignment character /F/= /K28.7/. However, if both sides of the lane support lane alignment, the lane alignment character /A/= /K28.3/ shall be used in the last frame of a multiframe.*

The following errors are indications of frame and multiframe alignment mismatch.

1. Frame Alignment Error: /F/ received at the unexpected location

2. Multiframe/Lane Alignment Error: /A/ received at the unexpected location.

3. Frame Synchronization Error: Consecutive /K/ received during data mode.

These errors are cleared when the JESD204C link is reset.

The following process describes the relationship of frame, multiframe, local multiframe boundary, and the potential sources of errors:

* Frame (F): a set of consecutive octets in which the position of each octet can be identified by reference to a frame alignment signal.
* Multi-frame (K): a set of consecutive frames in which the position of each frame can be identified by reference to a multiframe alignment signal.
* Frame boundary is needed for both the JESD204C transmitter and JESD204C receiver to have predetermined way to “process” the bit packing and octet packing of the data octets. This is performed in the transport layer of the JESD204B specification.
* Multiframe boundary is needed such that the JESD204C transmitter and JESD204C receiver can perform logics in the data path using their own perspective “local clock”. This is the local multiframe clock (or LMFC), which defines the logical processing clock to process the data octets.
* The idea is that the LMFC of each perspective JESD204C block can have known, well-defined, and deterministic delay between the data source and data receiver. The clocks do not have to have absolute delay defined in order to simplify clocking solution.
* The deterministic delays can be absorbed by the release buffer (elastic buffer) in the JESD204C receiver. Multiframe and Frame Alignment Alarms
* Frame alignment monitoring is constantly performed by checking that replacement characters /F/ and /A/ arrive at expected positions in the frame and multiframe.
* When these characters are received, they are replaced with actual data.
* If they are consistently received at unexpected positions, then frame alignment error or the multiframe alignment error would be triggered to indicate the alignment has been lost.
* Frame alignment correction is \*not\* supported. Therefore, the host need to perform re-alignment and resynchronization of the JESD204C link based on alarm feedback
* The following sections of the JESD204C Standard highlights the Frame and Multiframe Alignment:
	+ 8.4.4 Frame alignment monitoring and correction.
	+ 8.4.4.1 Alignment characters.

Sources of Error:

* “Drift” of SYSREF reset of LMFC over time.
	+ SYSREF reset of LMFC change in the “periodic” time instance over time.
	+ The overall LMFC boundary changes and potentially cause alignment errors.
	+ “Drift” of the clock source to various logics.
	+ “Drift” of incoming data on the JESD204C transmitter over time.
* The incoming data are sufficiently periodic and not sufficiently random. The character replacement rules for the /A/ and /F/ characters are not exercised sufficiently, and hence the periodic frame and multi-frame are not checked frequently.
* Incorrect initialization of the logical block in the JESD204C TX. The JESD204C IP was not reset properly upon start-up. Glitch occurs after various temperature cycle.

**4.2.7 Sync Header Errors (64B/66B and 64B/80B Encoding Specification Only)**

For every multi-block (consisted of 32 blocks of octets), there are two bit sync headers of either 2b’01 or 2b’10 format to ensure continuous synchronization of the JESD204 ink. These sync headers are also used to construct the CRC3, CRC12, or the FEC coding for error detection. Depending on the number of Extended Multi-block setup (EMB), the error on EMB could also be triggered.

The following are the related errors reported related to Sync Header.

**CRC12/CRC3 Error or FEC uncorrectable Error:**

This occurs when the full frame reconstruction of CRC3, CRC12, or FEC coding received from the JESD204 TX logic is not matching the expected behavior within the JESD204 RX.

**Sync-header Invalid Error:**

The Sync Header need to be binary bit stream of either 2b’01 or 2b’10. This error is triggered when the JESD204 RX received the non-valid code of 2b’00 or 2b’11.

Encoding and decoding invalid error could occur for the general pilot signal, CRC header, FEC header, and CMD header.

**Table 4-2. SYNC Header Encoding**



**Table 4-3. SYNC Header Decoding**



**Sync-header Alignment loss (OR) EMB Alignment**

When this error occurs, the JESD204C link is lost and need to resynchronize. The sync-head alignment loss is defined as per JESD204C section 7.6.1 where event of SH\_Icounter equals Rx\_Thresh\_SH\_ERR in the sync header alignment state machine.

The EMB alignment loss is defined per JESD204C section 7.6.2 where event of EMB\_counter equals Rx\_Thresh\_EMB\_ERR in the EMB alignment state machine.

With these errors result link loss, the alarm is cleared when sync-header state machine goes to lock state.

**4.2.8 CMD parity Error in CRC12/CRC3 mode**

There are total of 6 CMD bits (6 SPI bits + 1 parity derived from the XOR of the 6 SPI bits). This parity check utilizes the CMD bits from the JESD204C transmitter (i.e. FPGA or ASIC) and check against the SPI bits. If the two do not match, the error will be flagged more immediately than the CRC errors. The default is set to zeros for the CMD data.

**Table 4-4. CMD Parity Error Programming**

**DAC JESD Page**

|  |  |
| --- | --- |
| **Register Address** | **Register Description** |
| 0xB0 | JESDC\_CMD\_DATA[7:0] |
| 0xB1 | JESDC\_CMD\_DATA[15:8] |
| 0xB2 | JESDC\_CMD\_DATA[17:16] |

**4.2.10 End of Multi-block and End of Extended Multiblock Error (64B/66B and 64B/80B Encoding Specification Only)**

1. EoMB Alignment Error: 5’b00001 not received at correct location in sync-header. Refer to JESD204C document, Table 4-7, bit[31:27] of the Sync word mapping for detail.
2. EoEMB Alignment Error: EoEMB not received at correct location in sync-header. Refer to JESD204C document, Table 4-7, bit[22] of the Sync word mapping.
3. EoEMB in the pilot signal is defined as: a. 1 if the current multiblock is the last multiblock of extended multiblock b. 0 if the current multiblock is not the last multiblock of the extended multiblock

**Table 4-6. Sync Word Mapping With Stand-Alone Command Channel**

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**Table 4-7. Meaning of the CMD Sync Word Fields**



**4.2.11 Pilot Signal Error Fixed Ones in pilot Signal Error:**

Fixed seven ones in CRC12/CRC3/FEC not received at correct location in sync-header.

Refer to JESD204C document, Table 4-7, bit[3], bit[7] , bit[11] , bit[15] , bit[19] , bit[21] , bit[23] , bit[31] of the Sync word mapping for detail.

**4.2.12 Error Rate Detection**

For a lane rate of 32.5Gbps, in a normal scenario the BER would be 10-15. This would be one error in 8.5 hours. This error rate detection can trigger if there are two or more errors in one minute (BER of 10-11). The error can trigger link reset and the associated alarm can be raised.

**4.3 Lane and Link Aggregation**

* For JESD204C 64B/66B and 64B/80B encoding, the link establishment is done autonomously in the JESD204C Receiver (DAC Downlink Direction) without SYNC line interaction.
* Therefore the link aggregation is based on the programming of the lanes and link within the JESD204 receiver. This is the sync muxing setting in the AFE products.
* Within the JESD204 receiver, the data buffer release of all the lanes in a single link happen at the same time.
* The release occurs when all lanes in a link passes frame alignment in 8b/10b protocol
* The release occurs when all lanes in a link passes Multi Block alignment in 64B/66B or 64B/80B protocol.
* Any lane error in JESD204C lane will force the entire link to re-initialize

Link Reset Functionality

1. Link-reset can be triggered through any of the above mentioned JESD204C lane errors[10:0] getting triggered.
2. Link-reset can also be triggered whenever any of the count of the individual lane errors[10:0] in the 4-bit Error Threshold Counters crosses a corresponding threshold set for that particular error.
3. Error Threshold Counters are reset on link-reset. Additionally, Error Threshold Counters can be reset periodically.
4. Each of the Error Threshold Counters can be independently read/cleared through SPI