

Pull TXENABLE LOW

Reset DAC(toggle RESETB pin low then high)

0x09 0x0000

0x01 0x1880

0x00 0x5820

0x09 0x0004

0x0B 0x0000

0x0C 0x2900

0x09 0x0000

0x00 0x5820

0x01 0x1880

0x02 0xFFFF

0x03 0xFFFF

0x04 0x0000

0x05 0x0000

//page4

0x09 0x0004

0x0A 0xfC03

0x0B 0x0000

0x0C 0x2900

0x0D 0x4000

0x1B 0x0000

0x23 0xFFFF

0x24 0xc002

0x31 0x0400

0x32 0x0708

0x33 0x623C

0x34 0x0000

0x35 0x0018

0x3B 0x9802

0x3C 0x8229

0x3D 0x0088

0x3E 0x0909

0x3F 0x0000

//page1

0x09 0x0001

0x0A 0x421c

0x0C 0x0402

0x0D 0x1f00

0x0E 0x00FF

0x0F 0xFFFF

0x10 0xFFFF

0x11 0xFFFF

0x17 0x0000

0x19 0x0001

0x1C 0x0000

0x1D 0x0000

0x1E 0x0000

0x1F 0x0000

0x20 0x0000

0x21 0x0000

0x22 0x0000

0x23 0x0000

0x24 0x0010

0x25 0x3200

0x27 0x8888

0x28 0x0230

0x29 0x0000

0x2A 0x0000

0x2B 0x0000

0x2C 0x0000

0x2D 0x1FFF

0x2E 0x1FFF

0x2F 0x0000

0x30 0x0000

0x32 0x8400

0x33 0x0400

0x46 0x0044

0x47 0x190A

0x48 0x31C3

0x4A 0x0F03

0x4B 0x1300

0x4C 0x1303

0x4D 0x0001

0x4E 0x0F4F

0x4F 0x1C60

0x50 0x0000

0x51 0x001F

0x52 0x00FF

0x53 0x0100

0x54 0x8E60

0x5C 0x0001

0x5E 0x0000

0x5F 0x0123

0x60 0x4567

0x64 0x0000

0x65 0x0000

0x66 0x0000

0x67 0x0000

0x68 0x0000

0x69 0x0000

0x6A 0x0000

0x6B 0x0000

0x6C 0x0000

0x6D 0x0000

0x6E 0x0000

//page2

0x09 0x0002

0x0A 0x421c

0x0C 0x0402

0x0D 0x1f00

0x0E 0x00FF

0x0F 0xFFFF

0x10 0xFFFF

0x11 0xFFFF

0x17 0x0000

0x19 0x0001

0x1C 0x0000

0x1D 0x0000

0x1E 0x0000

0x1F 0x0000

0x20 0x0000

0x21 0x0000

0x22 0x0000

0x23 0x0000

0x24 0x0010

0x25 0x3200

0x27 0x8888

0x28 0x0230

0x29 0x0000

0x2A 0x0000

0x2B 0x0000

0x2C 0x0000

0x2D 0x1FFF

0x2E 0x1FFF

0x2F 0x0000

0x30 0x0000

0x32 0x83f4

0x33 0x0400

0x46 0x0044

0x47 0x190A

0x48 0x31C3

0x4A 0xF003

0x4B 0x1300

0x4C 0x1303

0x4D 0x0001

0x4E 0x0F4F

0x4F 0x1C60

0x50 0x0000

0x51 0x001F

0x52 0x00FF

0x53 0x0100

0x54 0x8E60

0x5C 0x0001

0x5E 0x0000

0x5F 0x4567

0x60 0x0123

0x64 0x0000

0x65 0x0000

0x66 0x0000

0x67 0x0000

0x68 0x0000

0x69 0x0000

0x6A 0x0000

0x6B 0x0000

0x6C 0x0000

0x6D 0x0000

0x6E 0x0000

//reset

0x09 0x0003

0x24 0x0000

0x5C 0x0000

0x09 0x0004

0x0A 0xFC03

0x0A 0x7C03

0x09 0x0000

0x00 0x5821

0x00 0x5823

0x09 0x0001

0x24 0x0010

0x09 0x0002

0x24 0x0010

0x09 0x0001

0x5C 0x0001

0x09 0x0002

0x5C 0x0001

0x09 0x0000

0x00 0x5821

0x00 0x5820

0x09 0x0000

0x04 0x0000

0x05 0x0000

0x09 0x0003

0x64 0x0000

0x65 0x0000

0x66 0x0000

0x67 0x0000

0x68 0x0000

0x69 0x0000

0x6A 0x0000

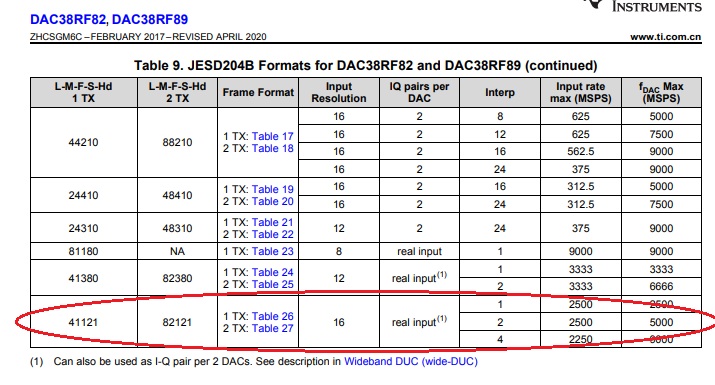
0x6B 0x0000

0x6C 0x0000

0x6D 0x0000

Pull TXENABLE HIGH

RESET FPGA JESD204B IP



Set the dac38rf82 in 82121 mode , and 4x Interpolation , 6.4G sample rate , 1.6Ghz data rate ,do not use NCO, PLL refclk is 200MHz. Configure those resgisters, the FPGA JESD READY is "1", but the DAC has no signal output, then stop sysref generation to DAC and start SYSREF generation. Only then dose DAC output normally. But sometimes I/Q signal have phase error.