I have run into a problem porting the zcu102\_64b66b reference design from a 8 lane design to a 2 lane design. The  TI xzcu102 64/66 bit reference design with 8 JESD lanes, for evaluation of the AFE7950 on the EVM7950 works reliably with 8 lanes as supplied but does not  work when reconfigured to work over 2 lanes. The 8 lane design works reliably. However the two lane design

The following is the capture when I try and convert the 8 channel 8 lane reference design supplied as your reference design on a zcu102 dev card to an 8 channel 2 lane design. The rx side in the FPGA is not delivering any data. The ila\_rx\_data\_valid stays low always. The TX from the FPGA side is outputting a tone. The changes I made were to decimate the data to allow lanes rates to remain the same as initial reference design supplied.



This design change was achieved by changing the variables in the original file : TI\_IP\_12Gbps\_8Lane\_ConfigLmk.py that control decimation of the data .Since I reduced my overall bandwidth by 4 is from 8 lanes to 2 therefore I adjusted the decimation params by 4 . So as you can see from the included script . The following parameters were adjusted to.

sysParams.ddcFactorRx = [16]\*4 # DDC decimation factor for RX A, B, C and D

sysParams.ddcFactorFb = [16]\*2

sysParams.ducFactorTx = [32]\*4

from

sysParams.ddcFactorRx = [4]\*4 # DDC decimation factor for RX A, B, C and D

sysParams.ddcFactorFb = [4]\*2

sysParams.ducFactorTx = [12]\*4

The LMFS were also changed to configure the JESD interface for 2 lane operation:

ysParams.LMFSHdRx =['14810', '14810', '14810', '14810']

 # The 2nd and 4th are valid only for jesdSystemMode values in (2,6,7,8). For other modes, select 4 converter modes for 1st and 3rd.

sysParams.LMFSHdFb = ["22210","22210"]

sysParams.LMFSHdTx = ["14810","14810","14810","14810"]

from

ysParams.LMFSHdRx =['44210', '44210', '44210', '44210']

 # The 2nd and 4th are valid only for jesdSystemMode values in (2,6,7,8). For other modes, select 4 converter modes for 1st and 3rd.

sysParams.LMFSHdFb = ["22210","22210"]

sysParams.LMFSHdTx = ["44210","44210","44210","44210"]

The changes on to FPGA code were limited to the following in the jesd\_links\_params.vh file:

To :

`define NUMBER\_OF\_RX\_LANES 2

`define NUMBER\_OF\_TX\_LANES 2

From

define NUMBER\_OF\_RX\_LANES 8

`define NUMBER\_OF\_TX\_LANES 8

To:

undef NUMBER\_OF\_QUADS

`define NUMBER\_OF\_QUADS 1

From

undef NUMBER\_OF\_QUADS

`define NUMBER\_OF\_QUADS 2

To:

undef LANE\_ADC\_TO\_GT\_MAP

`define LANE\_ADC\_TO\_GT\_MAP {2, 1}

`undef LANE\_DAC\_TO\_GT\_MAP

`define LANE\_DAC\_TO\_GT\_MAP {2, 1}

From:

undef LANE\_ADC\_TO\_GT\_MAP

`define LANE\_ADC\_TO\_GT\_MAP {5,4,6,7,3,0,2,1}

`undef LANE\_DAC\_TO\_GT\_MAP

`define LANE\_DAC\_TO\_GT\_MAP {4,5,6,7,3,0,2,1}

define RX\_F\_VAL 8

To

`undef TX\_F\_VAL

`define TX\_F\_VAL 8

From:

define RX\_F\_VAL 2

`undef TX\_F\_VAL

`define TX\_F\_VAL 2

*The following is report from VIO after I toggle the rx\_rst to 1 on the VIO*



***The following is the configuration of the LMK and other system params:***

Validation : AFE79xx Library Version

v1.67, v1.74

Case RX TX FB CLK Notes

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1 245.76Msps, 24410 491.52Msps, 44210 491.52Msps, 22210 FADC=2949.12M DAC in interleaved mode

SerDes=9830.4Mbps SerDes=9830.4Mbps SerDes=9830.4Mbps FDAC=8847.36M

PLL0, NCO=3500M PLL0, NCO=3500M NCO=3500M REF=491.52M

2 245.76Msps, 24410 491.52Msps, 44210 491.52Msps, 22210 FADC=2949.12M DAC in straight mode

SerDes=9830.4Mbps SerDes=9830.4Mbps SerDes=9830.4Mbps FDAC=8847.36M

PLL0, NCO=3500M PLL0, NCO=3500M NCO=3500M REF=491.52M

'''

setupParams.skipFpga = 1

sysParams = AFE.systemParams

setupParams.fpgaRefClk = 184.32

AFE.systemStatus.loadTrims = 1

sysParams.fbEnable = [False]\*2

sysParams.FRef = 491.52

sysParams.FadcRx = 2949.12

sysParams.FadcFb = 2949.12

sysParams.Fdac = 2949.12\*2

sysParams.enableDacInterleavedMode = False #DAC interleave mode to save power consumption. Fs/2 - Fin spur occurs

sysParams.modeTdd = 0

# 0- Single TDD Pin for all Channels

# 1- Separate Control for 2T/2R/1F

# 2- Separate Control for 1T/1R/1F

sysParams.topLevelSystemMode = 'StaticTDDMode'

sysParams.RRFMode = 0 #4T4R2F FDD mode

sysParams.jesdSystemMode = [3,3]

#SystemMode 0: 2R1F-FDD ; rx1-rx2-fb-fb

#SystemMode 1: 1R1F-FDD ; rx1-rx1-fb-fb

#SystemMode 2: 2R-FDD ; rx1-rx1-rx2-rx2

#SystemMode 3: 1R ; rx1-rx1-rx1-rx1

#SystemMode 4: 1F ; fb-fb-fb-fb

#SystemMode 5: 1R1F-TDD ; rx1/fb-rx1/fb-rx1/fb-rx1/fb

#SystemMode 8: 1R1F-TDD 1R-FDD (FB-2Lanes)(RX1 RX2 interchanged) ; rx2/fb-rx2/fb-rx1-rx1

sysParams.jesdLoopbackEn = 0 #Make it 1 to Enable the JESDTX to JESDRX internal loopback

sysParams.LMFSHdRx =['14810', '14810', '14810', '14810']

# The 2nd and 4th are valid only for jesdSystemMode values in (2,6,7,8). For other modes, select 4 converter modes for 1st and 3rd.

sysParams.LMFSHdFb = ["22210","22210"]

sysParams.LMFSHdTx = ["14810","14810","14810","14810"]

sysParams.jesdTxProtocol = [2,2] #64b/66b

sysParams.jesdRxProtocol = [2,2] #64b/66b

sysParams.serdesFirmware = True # If you want to lead any firmware, please speify the path here. Otherwise it will not write any firmware

sysParams.jesdTxLaneMux = [0,1,2,3,4,5,6,7]

# Enter which lanes you want in each location.

# Note that across 2T Mux is not possible in 0.5.

# For example, if you want to exchange the first two lines of each 2T, this should be [[1,0,2,3],[5,4,6,7]]

sysParams.jesdRxLaneMux = [0,1,2,3,4,5,6,7]

# Enter which lanes you want in each location.

# Note that across 2R Mux is not possible in 0.5.

# For example, if you want to exchange the first two lines of each 2R, this should be [[1,0,2,3],[5,4,6,7]]

sysParams.jesdRxRbd = [4, 4]

# scrambler is disabled

sysParams.rxJesdTxScr = [False]\*4

sysParams.fbJesdTxScr = [False]\*2

sysParams.jesdRxScr = [False]\*4

sysParams.rxJesdTxK = [1]\*4

sysParams.fbJesdTxK = [1]\*2

sysParams.jesdRxK = [1]\*4

sysParams.ncoFreqMode = "1KHz"

sysParams.txNco0 = [[5200,5200], #Band0, Band1 for TxA for NCO0

[5200,5200], #Band0, Band1 for TxB for NCO0

[5200,5200], #Band0, Band1 for TxC for NCO0

[5200,5200]] #Band0, Band1 for TxD for NCO0

sysParams.rxNco0 = [[5200,5200], #Band0, Band1 for RxA for NCO0

[5200,5200], #Band0, Band1 for RxB for NCO0

[5200,5200], #Band0, Band1 for RxC for NCO0

[5200,5200]] #Band0, Band1 for RxD for NCO0

sysParams.fbNco0 = [5200,5200] #FBA, FBC for NCO0

sysParams.numBandsRx = [0]\*4 # 0 for single, 1 for dual

sysParams.numBandsFb = [0,0]

sysParams.numBandsTx = [0,0,0,0]

sysParams.ddcFactorRx = [16]\*4 # DDC decimation factor for RX A, B, C and D

sysParams.ddcFactorFb = [16]\*2

sysParams.ducFactorTx = [32]\*4

AFE.systemStatus.loadTrims =1

## The following parameters sets up the LMK04828 clocking schemes

lmkParams.pllEn = True#False

lmkParams.inputClk = 1474.56#737.28

lmkParams.lmkFrefClk = True

## The following parameters sets up the register and macro dumps

logDumpInst.setFileName(ASTERIX\_DIR+DEVICES\_DIR+r"\Afe79xxPg1.txt")

logDumpInst.logFormat = 0x00

logDumpInst.rewriteFile = 1

logDumpInst.rewriteFileFormat4 = 1

device.optimizeWrites = 0

device.rawWriteLogEn = 1

## The following parameters sets up the SYNCIN and SYNCOUT to interface with the TSW14J57

sysParams.jesdABLvdsSync = 1

sysParams.jesdCDLvdsSync = 1

sysParams.rxJesdTxSyncMux = [0,0,0,0]

sysParams.fbJesdTxSyncMux = [0,0]

sysParams.jesdRxSyncMux = [0,0,0,0] #[0,0,1,1]

sysParams.syncLoopBack = True

# ## The following parameters sets up the AGC

# sysParams.agcParams[0].agcMode = 1 ##internal AGC

# sysParams.agcParams[0].gpioRstEnable = 0 ##disable GPIO based reset to AGC detector

# sysParams.agcParams[0].atken = [0, 1, 0] ##enable big and small step attack

# sysParams.agcParams[0].decayen = [0,1,0] ##enable big and small step decay

# sysParams.agcParams[0].atksize = [2,1,0] ## bigs step = 2dB, small step = 1dB

# sysParams.agcParams[0].decaysize = [2,1,0] ##big step = 2dB, small step = 1dB

# sysParams.agcParams[0].atkthreshold = [-1, -2, -14] ##attack threshold

# sysParams.agcParams[0].decaythreshold = [-14, -6, -20] ##decay threshold

# sysParams.agcParams[0].atkwinlength = [170, 170] ## detector time constant expressed inn absolute time in ns.

# sysParams.agcParams[0].decaywinlength = 87380 ##detector time constant expressed in absolute time in ns. All detectors use the same value for decay time constant

# sysParams.agcParams[0].atkNumHitsAbs = [8,8] ##absolute number of times signal crosses threshold. These crossing are with respect to the FADC/8 clock

# sysParams.agcParams[0].decayNumHitsAbs = [100,100] ##absolute number of times signal crosses threshold. These crossing are with respect to the FADC/8 clock

# sysParams.agcParams[0].minDsaAttn = 0 ##minimum DSA attenuation used by AGC

# sysParams.agcParams[0].maxDsaAttn = 22 ##maximum DSA attenuation used by AGC

# sysParams.agcParams[0].totalGainRange = 22 ##total gain range used by ALC for gain compensation

# sysParams.agcParams[0].minAttnAlc = 0 ##minimum attenuation used by ALC for compensation when useMinAttnAgc = 0

# sysParams.agcParams[0].useMinAttnAgc = 1 ##enable ALC to use minimum attenuation from AGC for which compensation is required.

# sysParams.agcParams[0].alcEn = 1

# sysParams.agcParams[0].alcMode = 0 ##floating point DGC

# sysParams.agcParams[0].fltPtMode = 0 ##if exponent > 0, dont send MSB

# sysParams.agcParams[0].fltPtFmt = 1 ##3 bit exponent

## The following parameters sets up the GPIOs

sysParams.gpioMapping={

'H8': 'ADC\_SYNC0',

'H7': 'ADC\_SYNC1',

'N8': 'ADC\_SYNC2',

'N7': 'ADC\_SYNC3',

'H9': 'DAC\_SYNC0',

'G9': 'DAC\_SYNC1',

'N9': 'DAC\_SYNC2',

'P9': 'DAC\_SYNC3',

'P14': 'GLOBAL\_PDN',

'K14': 'FBABTDD',

'R6': 'FBCDTDD',

'H15': ['TXATDD','TXBTDD'],

'V5': ['TXCTDD','TXDTDD'],

'E7': ['RXATDD','RXBTDD'],

'R15': ['RXCTDD','RXDTDD']}

#AFE.systemParams.papParams[0]['enable'] = True

#AFE.systemParams.papParams[1]['enable'] = True

#AFE.systemParams.papParams[2]['enable'] = True

#AFE.systemParams.papParams[3]['enable'] = True

## Initiates LMK04828 and AFE79xx Bring-up

setupParams.skipLmk = False

AFE.initializeConfig()

lmkParams.sysrefFreq = AFE.systemStatus.sysrefFreq

AFE.LMK.lmkConfig()

LOG as executing AFE7950/bringup/12Gbps\_2Lane\_ConfigLmk.py

Executing .. AFE7950/bringup/12Gbps\_2Lane\_ConfigLmk.py

#Start Time 2023-10-24 13:23:44.121000

The External Sysref Frequency should be an integer factor of: 1.92MHz

2T2R1F Number: 0

Valid Configuration: True

laneRateRx: 12165.12

laneRateFb: 12165.12

laneRateTx: 12165.12

2T2R1F Number: 1

Valid Configuration: True

laneRateRx: 12165.12

laneRateFb: 12165.12

laneRateTx: 12165.12

LMK Clock Divider - Device registers reset.

LMK Clock Divider - Device registers reset.

REFCLOCK is used from LMK source, ensure board connections are ok to do the same

#Done executing .. AFE7950/bringup/12Gbps\_2Lane\_ConfigLmk.py

#End Time 2023-10-24 13:23:44.793000

#Execution Time = 0.671999931335 s

#================ ERRORS:0, WARNINGS:1 ================#

Log as ConifgAFE.apy is run

#Executing .. AFE7950/bringup/TI\_IP\_ConfigAfe.py

#Start Time 2023-10-24 13:25:20.114000

The External Sysref Frequency should be an integer factor of: 1.92MHz

2T2R1F Number: 0

Valid Configuration: True

laneRateRx: 12165.12

laneRateFb: 12165.12

laneRateTx: 12165.12

2T2R1F Number: 1

Valid Configuration: True

laneRateRx: 12165.12

laneRateFb: 12165.12

laneRateTx: 12165.12

LMK and FPGA Configured.

DONOT\_OPEN\_Atharv\_FULL - Device registers reset.

chipType: 0xa

chipId: 0x78

chipVersion: 0x11

AFE Reset Done

Fuse farm load autoload done successful

No autload error

Fuse farm load autoload done successful

No autload error

//Firmware Version = 11000

//PG Version = 1

//Release Date [dd/mm/yy] = 10/7/19

patchSize=11697

//Patch Version = 165

//PG Version = 0

//Release Date [dd/mm/yy] = 27/11/21

AFE MCU Wake up done and patch loaded.

PLL Locked

AFE PLL Configured.

AFE SerDes Configured.

AFE Digital Chains configured.

AFE TX Analog configured.

AFE RX Analog configured.

AFE FB Analog configured.

AFE JESD configured.

AFE AGC configured.

AFE GPIO configured.

Sysref Read as expected

Setting RBD to: 40

Setting RBD to: 40

cpldRegProg.\_writePacket : write failed.

cpldRegProg.\_writePacket : write failed.

cpldRegProg.\_writePacket : write failed.

cpldRegProg.\_writePacket : write failed.

###########Device DAC JESD-RX 0 Link Status###########

CS State TX0: 0b00000010 . It is expected to be 0b00000010

BUF State TX0: 0b00000011 . It is expected to be 0b00000011

Could get the link up for device RX: 0

###################################

###########Device DAC JESD-RX 1 Link Status###########

CS State TX0: 0b00000010 . It is expected to be 0b00000010

BUF State TX0: 0b00000011 . It is expected to be 0b00000011

Could get the link up for device RX: 1

###################################

AFE Configuration Complete

#Done executing .. AFE7950/bringup/TI\_IP\_ConfigAfe.py

#End Time 2023-10-24 13:27:19.420000

#Execution Time = 119.305999994 s

#================ ERRORS:0, WARNINGS:4 ================#