

Read me

#In HSDC Pro DAC tab, Select AFE79xx_1x2TX_44210; Data Rate = 491.52M

#In HSDC Pro ADC tab, Select AFE79xx_1x2RX_44210; Data Rate = 491.52M

sysParams=AFE.systemParams

sysParams.__init__();sysParams.chipVersion=chipVersion

setupParams.skipFpga = 1 # setup FPGA (TSW14J56) using HSDC Pro

Top Level

sysParams.FRef = 491.52

sysParams.FadcRx = 2949.12

sysParams.FadcFb = 2949.12

sysParams.Fdac = 2949.12*3

sysParams.externalClockRx=False

sysParams.externalClockTx=False

Digital Chain

RX

sysParams.rxEnable = [True,True,True,True]

sysParams.ddcFactorRx = [6,6,6,6] #DDC decimation factor for RX A, B, C and D

sysParams.rxNco0 = [[5400,5400], #Band0, Band1 for RxA

[500,500], #Band0, Band1 for RXB

[2500,2500], #Band0, Band1 for RXC

[1800,1800]] #Band0, Band1 for RXD

FB

sysParams.fbEnable = [False]*2

sysParams.ddcFactorFb = [6,6] #DDC decimation factor for FB 1 and 2

sysParams.fbNco0 = [500,1800] #Band0 for FB1 and FB2

TX

sysParams.txEnable = [True,True,True,True]

sysParams.ducFactorTx = [18,18,18,18] #DDC decimation factor for TX A, B, C and D

sysParams.txNco0 = [[5400,5400], #Band0, Band1 for TXA

[500,500], #Band0, Band1 for TXB

[2500,2500], #Band0, Band1 for TXC

[1800,1800]] #Band0, Band1 for TXD

JESD

ADC-JESD

sysParams.jesdSystemMode= [3,3]

#SystemMode 0: 2R1F-FDD ; rx1-rx2-fb -fb

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#SystemMode 1: 1R1F-FDD ; rx -rx -fb -fb
#SystemMode 2: 2R-FDD ; rx1-rx1-rx2-rx2
#SystemMode 3: 1R ; rx -rx -rx -rx
#SystemMode 4: 1F ; fb -fb- fb -fb
#SystemMode 5: 1R1F-TDD ; rx/fb-rx/fb-rx/fb-rx/fb
sysParams.jesdTxDProtocol= [0,0] # 0 - 8b/10b encoding; 2 - 64b/66b encoding
sysParams.LMFSHdRx = ["44210","44210","44210","44210"]
# The 2nd and 4th are valid only for jesdSystemMode values in (0,2).
# For other modes, select 4 converter modes for 1st and 3rd.
sysParams.LMFSHdFb = ["22210","22210"]

sysParams.rxJesdTxDScr = [True,True,True,True]
sysParams.fbJesdTxDScr = [True,True]

sysParams.rxJesdTxDK = [16,16,16,16]
sysParams.fbJesdTxDK = [16,16]

#sysParams.rxDataMux = [0,1,4,5,2,3,6,7]
sysParams.jesdTxDLaneMux = [0,1,2,3,4,5,6,7] # Enter which lanes you want in each location.
# For example, if you want to exchange the first two lines of each 2T,
# this should be [[1,0,2,3],[5,4,6,7]]

##### DAC-JESD #####
sysParams.jesdRxProtocol= [0,0]
sysParams.LMFSHdTx = ["44210","44210","44210","44210"]
#sysParams.txDataMux = [6,7,2,3,4,5,0,1]
sysParams.jesdRxLaneMux = [0,1,2,3,4,5,6,7] # Enter which lanes you want in each location.
# For example, if you want to exchange the first two lines of each 2R
# this should be [[1,0,2,3],[5,4,6,7]]
sysParams.jesdRxRbd = [4, 4]
sysParams.jesdRxScr = [True,True,True,True]
sysParams.jesdRxK = [16,16,16,16]

##### JESD Common #####
sysParams.jesdABLvdsSync= True
sysParams.jesdCDLvdsSync= True
sysParams.syncLoopBack = True #JESD Sync signal is connected to FPGA

##### GPIO #####
sysParams.gpioMapping = {
'H8': 'ADC_SYNC0',
'H7': 'ADC_SYNC1',
'N8': 'ADC_SYNC2',
'N7': 'ADC_SYNC3',
'H9': 'DAC_SYNC0',
'G9': 'DAC_SYNC1',

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```
'N9': 'DAC_SYNC2',
'P9': 'DAC_SYNC3',
'P14': 'GLOBAL_PDN',
'K14': 'FBABTDD',
'R6': 'FBCDTDD',
'H15': ['TXATDD','TXBTDD'],
'V5': ['TXCTDD','TXDTDD'],
'E7': ['RXATDD','RXBTDD'],
'R15': ['RXCTDD','RXDTDD']}]}
```

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##### LMK Params #####
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lmkParams.pllEn = True
lmkParams.inputClk = 983.04 # Valid only when lmkParams.pllEn = False
lmkParams.lmkFrefClk = True
setupParams.fpgaRefClk = 245.76 # Should be equal to LaneRate/40 for TSW14J56
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##### Logging #####
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logDumpInst.setFileName(ASTERIX_DIR+DEVICES_DIR+r"\Afe79xxPg1.txt")
logDumpInst.logFormat=0x0 #Modify to 0x1 to save register ssequence to log file. Script takes
more time to execute.
logDumpInst.rewriteFile=1
logDumpInst.rewriteFileFormat4=1
device.optimizeWrites=0
device.rawWriteLogEn=1
```

```
device.delay_time = 0
```

```
#-----#
AFE.deviceBringup()
```

```
AFE.TOP.overrideTdd(1,0,1) # bit-wise; 4R,0F,4T
```