LMH 9226 Electrical Characteristics

Parameter	**Unit**	**Test condition**	**Supplier item Supplier**		
			min	**type**	**max**
Functional Requirements	Support TDD	/		Yes	
	Support Bypass	/		No	
Operating Frequency Ranges	MHz		2300		2900
Gain	dB	LNA On state		17	
		LNA Off state			
Insertion loss (Bypass on)	dB	Bypass On			
In-band ripple / any 100M	dB	/			1
Out Band Gain	dB	LNA On state			
Supply Current	A	LNA On state		0.084	0.1
		LNA Off state			0.01
Supply Voltage	V	LNA On state	3.15	3.3	3.45
		LNA Off state			
Input Power	dBm	LNA On state			25
		LNA Off state			25
Input Return Loss	dB	LNA On state, PVT		-11	
		LNA Off state, PVT			
		Bypass On, PVT			
Output Return Loss	dB	LNA On state, PVT		-12	
		LNA Off state, PVT			
		Bypass On, PVT			

Noise Factor	dB	25℃/ PVT		3	
Output P1dB	dBm	LNA On state, PVT		17.5	
		Bypass On, PVT			
Output IP3	dBm	LNA On state, PVT		35	
		Bypass On, PVT			
Shutdown isolation（Pin≤20dBm）Isolation	dB	LNA Off state, PVT		3	
Differential output gain imbalance	dB	LNA On state, PVT		0.5	
Differential output phase imbalance	Deg	LNA On state, PV		4	
Reverse isolation	dB	LNA On state, PVT		35	
Enable Voltage	V	LNA On state, PVT			0.5
		LNA Off state, PVT	1.4		
		Bypass On, PVT			
		Bypass Off, PVT			
Enable Current	mA				0.06
Switch time（Vctrol 50%->90% RF out）	us	LNA off to LNA on,PVT		0.5	
		Bypass on to LNA on,PVT			
		LNA on to Bypass on ,PVT			
Switch time（Vctrol 50%->99% RF out）	us	LNA off to LNA on,PVT			1

		Bypass on to LNA on,PVT			
		LNA on to Bypass on ,PVT			
Switch time （Vctrol 50%->10% RF out）	us	LNA on to LNA off,PVT		0.2	
Switch time （Vctrol 50%->1% RF out）	us	LNA on to LNA off,PVT			
Control Voltage True Table			0~0.5V on 1.4V~VDD off		
Maximum input power	dBm	PVT	25		
Absolutely stable below 12G (that is, no self-excitation regardless of application circuit and PCB design)	-	PVT		Yes	
Spur during on or off state	dBm	PVT			-30
VSWR	/				
maximum Junction Temperature	℃	PV	125 (150 for absolute maximum Junction Temperature)		
Operating Temperature Range	℃	PV	-40~105		
Storage Temperature Range	℃	P	-65~150		
θ jc	℃	PV	14.2 (junction to bottom)		
Lifetime at max. Tj	Years	PVT，on state，off state	>=10 Year		

ESD-HBM, for all pin	V	PVT,need 500V	+-1000V
ESD-CDM	V	PVT,need 250V	+-500V
MSL, Moisture Sensitive Level	/	PVT, ≤MSL3	2
Package size	mm*mm		2*2
Stress for device	N	Refer to basestation production spec Including top pressure and side pressure	
Reflow Requirement SMD package should do reflow(profile refer to J-STD-020D) before ATE If the chip has done reflow during the assembly process, don't need to add reflow again			Follow JEDEC
Independent power and control signals, no power-on and power-off timing requirements			Yes

Parameters	**Test or No**	Supplier feedback
Frequency Range	must	Device is tested at the band center in production
current leakage for power pin	must	Yes
Gain	must	Covered for outliers
NF	must	No
Stability	must	Yes, large signal oscillations in band is covered
VSWR	must	No
OIP3	must	IMD3 Covered for outliers
OP-1dB	must	No

Parameter	Unit	Requirement	Supplier's spec
IFR Intrinsic Failure Rate	Fit	Maximum：25@Tjuse	
		Typical：10@Tjuse	5