AN-2064 LMH2120 Evaluation Board

User's Guide

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The LMH2120 is a 40 dB Linear RMS power detector particularly suited for accurate power measurement of modulated RF signals that exhibit large peak-to-average ratios; i.e., large variations of the signal envelope. Such signals are encountered in W-CDMA and LTE cell phones. The RMS measurement topology inherently ensures a modulation insensitive measurement.

1 General Description

The LMH2120 is a 40 dB Linear RMS power detector particularly suited for accurate power measurement of modulated RF signals that exhibit large peak-to-average ratios; i.e., large variations of the signal envelope. Such signals are encountered in W-CDMA and LTE cell phones. The RMS measurement topology inherently ensures a modulation insensitive measurement.

The device has an RF frequency range from 50 MHz to 6GHz. It provides an accurate temperature- and supply- insensitive output voltage that relates linearly to the RF input power (see Figure 5). The LMH2120's excellent conformance to a linear response enables an easy integration by using slope and intercept only, reducing calibration effort significantly. The device operates with a single supply from 2.7V to 5V. The LMH2120 has an RF power detection range from -35 dBm to 5dBm and is ideally suited for use in combination with a directional coupler. Alternatively, a resistive divider can be used.

The device is active for EN=High − otherwise it is in a low power-consumption shutdown mode. To save power and prevent discharge of an external filter capacitance, the output (OUT) is high impedance during shutdown.

The LMH2120 power detector is offered in a tiny 6-bump microSMD package.

Figure 1 shows the LMH2120 Evaluation Board.

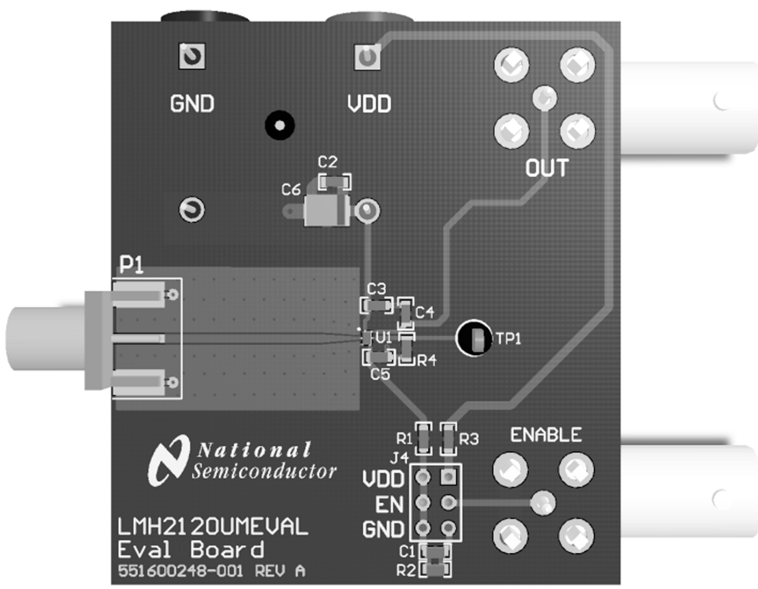

Figure 1. LMH2120 Evaluation Board

2 Basic Operation

The circuit operates with a single supply form 2.7V to 5V and has an RF power detection range from −35 dBm to 5dBm. The board consist of a single LMH2120 along with external components soldered on a printed circuit board. External supply voltages and input signals can be applied to the on-board connectors. The supply voltage is applied with connectors P21 (VDD) and P22 (GND). The RF input signal is applied by SMA connector P1. This RF signal is applied through an RF generator and is connected with a 50Ω SMA cable. The detector output can be measured via BNC connector P3.

3 Configuration

The LMH2120 evaluation board can be configured via jumper settings. The device is active when EN = High. This can be accomplished by setting the jumper J4 to VDD or by using external control on P4 by setting the jumper J4 to EN. Since the device has an internal operating voltage of 2.5V, the voltage level on the enable should not be higher than 3V to prevent damage to the device. Also enable voltage levels lower than 400 mV below GND should be prevented. In both cases the ESD devices start to conduct when the enable voltage range is exceeded and excessive current will be drawn. To guarantee a correct operation, a voltage divider formed by R2 and R3 is present on the evaluation board. The absolute maximum ratings are also exceeded when the enable (EN) is switched to HIGH (from shutdown to active mode) while the supply voltage is switched off. This situation should be prevented at all times. A solution to protect the device is the resistor R1 of 1kΩ in series with the enable input to limit the current.

An overview of the various jumper positions on the board is given in Figure 2. The settings of these jumpers and their functions are listed in Table 1.

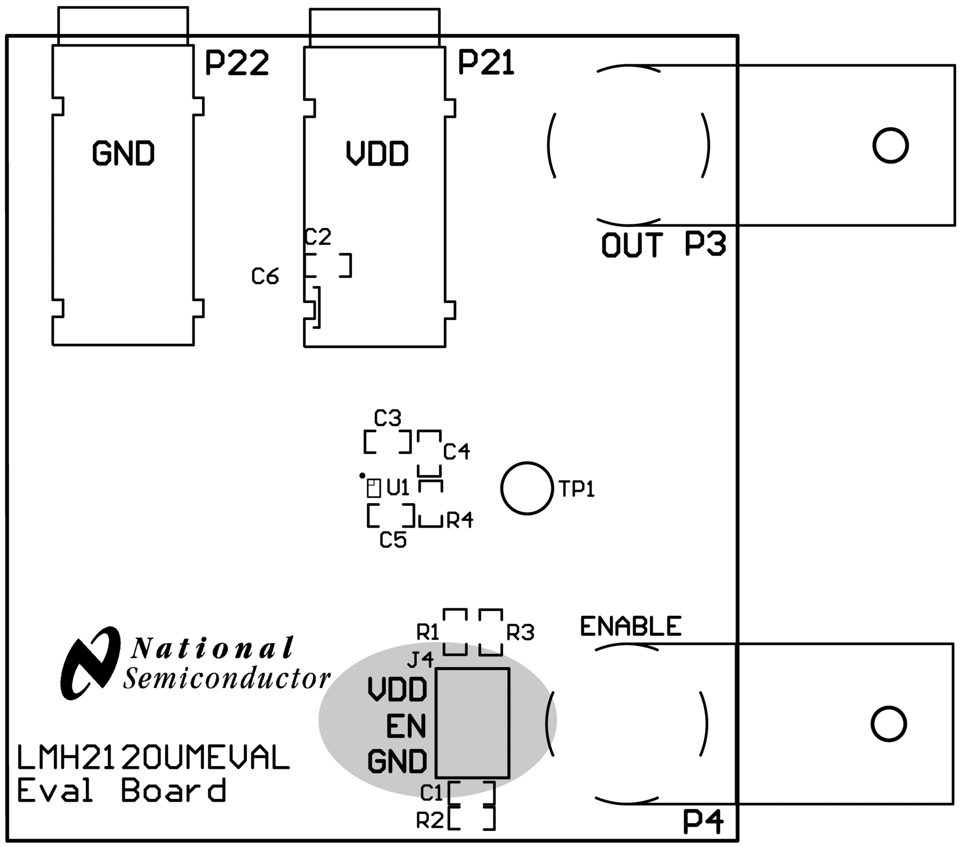

Figure 2. Jumper Positions

Table 1. Jumper and Header Overview [(1)]

Jumper	Function	Jumper Position	Description
J4	Enable	**1–2**	**Active, Connects Enable Pin to VDD**
		3–4	External Control, Connects Enable Pin to Enable P4
		5-6	Shutdown, Connects Enable Pin to GND

(1) Bold face jumper settings refer to the factory default configuration.

4 Measurement Setup

The performance of the LMH2120 can be measured with the setup shown in Figure 3.

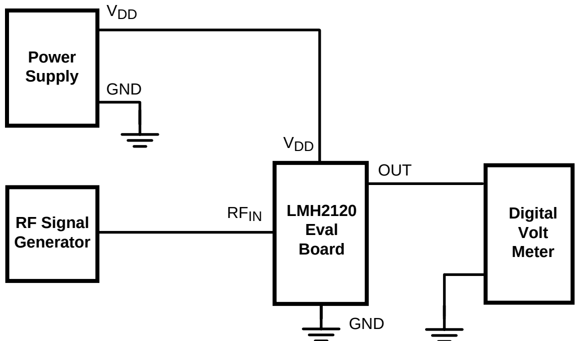

Figure 3. Measurement Setup

An external power supply provides a voltage of 2.7V to 5V to the evaluation board. An accurate and stable RF Signal Generator is used to produce the test signal. Use of low loss cables is recommended to ensure reliable measurement data. The detected output voltage can be measured with a Digital Voltage Meter (DVM).

Figure 4 depicts the output voltage versus frequency for various power levels on RF_{IN}. The frequency range is from 10 MHz to 10 GHz. Figure 5 depicts the output voltage versus RF input power for various frequencies.

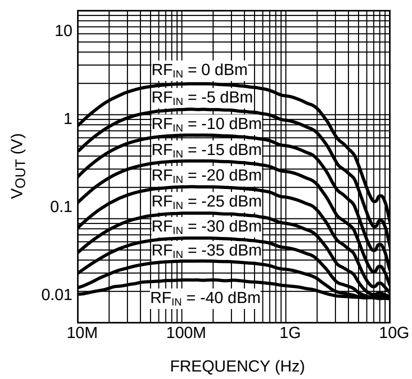

Figure 4. Output Voltage vs. Freqency

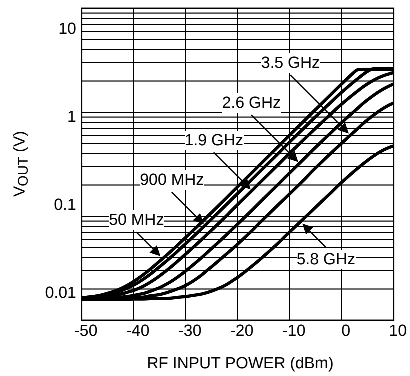

Figure 5. Output Voltage vs. RF Input Power

5 Schematic

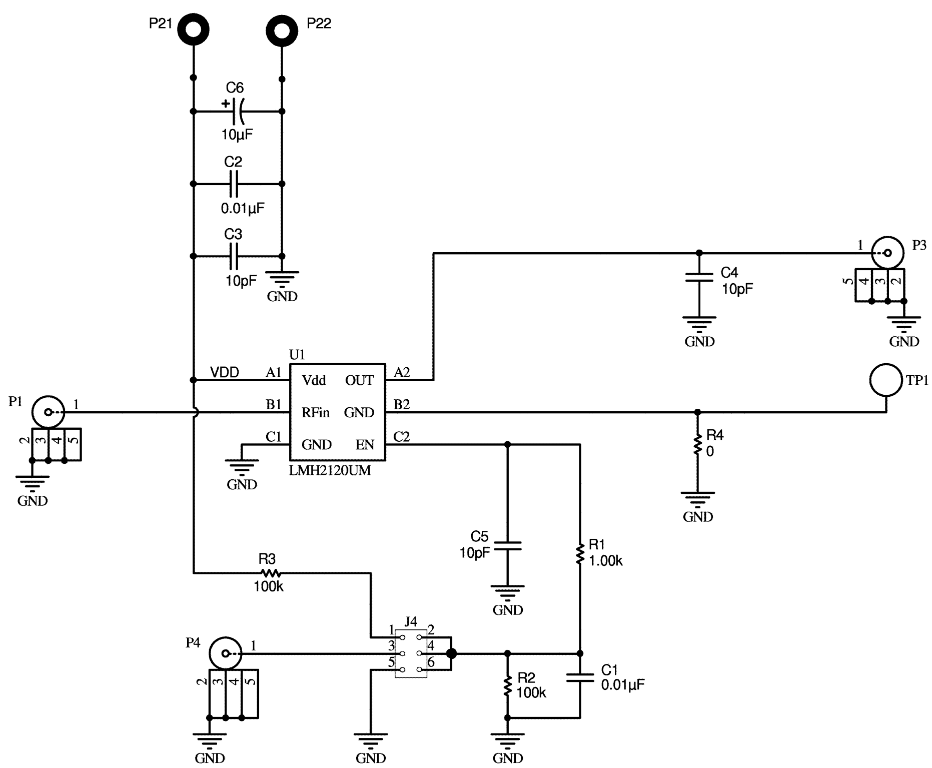

Figure 6. Evaluation Board Schematic

6 Bill of Material

The Bill of Material (BOM) of the evaluation board is given in Table 2.

Table 2. Bill of Material

Designator	Description	Comment
C1, C2	0603 Capacitor	10 nF
C3, C4, C5	0603 Capacitor	10 pF
C6	0603 Capacitor	10 µF
J4	Header	2x3
P1	Connector	SMA
P21, P22	Connector	Banana
P3, P4	Connector	BNC
R1	0603 Resisitor	1 kΩ
R2, R3	0603 Resistor	100 kΩ
R4	0603 Resisitor	0Ω
TP1	Test Point	GND
U1	µSMD	LMH2120UM

7 Board Layout

As with any other RF device, careful attention must be paid to the board layout. If the board layout isn't properly designed, performance might be less than can be expected for the application. The LMH2120 is designed to be used in RF applications, having a characteristic impedance of 50Ω. To achieve this impedance, the input of the LMH2120 needs to be connected via a 50Ω transmission line. Transmission lines can be created on PCBs using microstrip or (grounded) coplanar waveguide (GCPW) configurations. In order to minimize injection of RF interference into the LMH2120 through the supply lines, the PCB traces for VDD and GND should be minimized for RF signals. This can be done by placing a small decoupling capacitor between the VDD and GND. It should be placed as close as possible to the VDD and GND pins of the LMH2120.

Figure 7 shows the component locations of the LMH2120 evaluation board, and Figure 8 shows the board layout of the LMH2120 evaluation board.

8 LMH2120 Evaluation Board

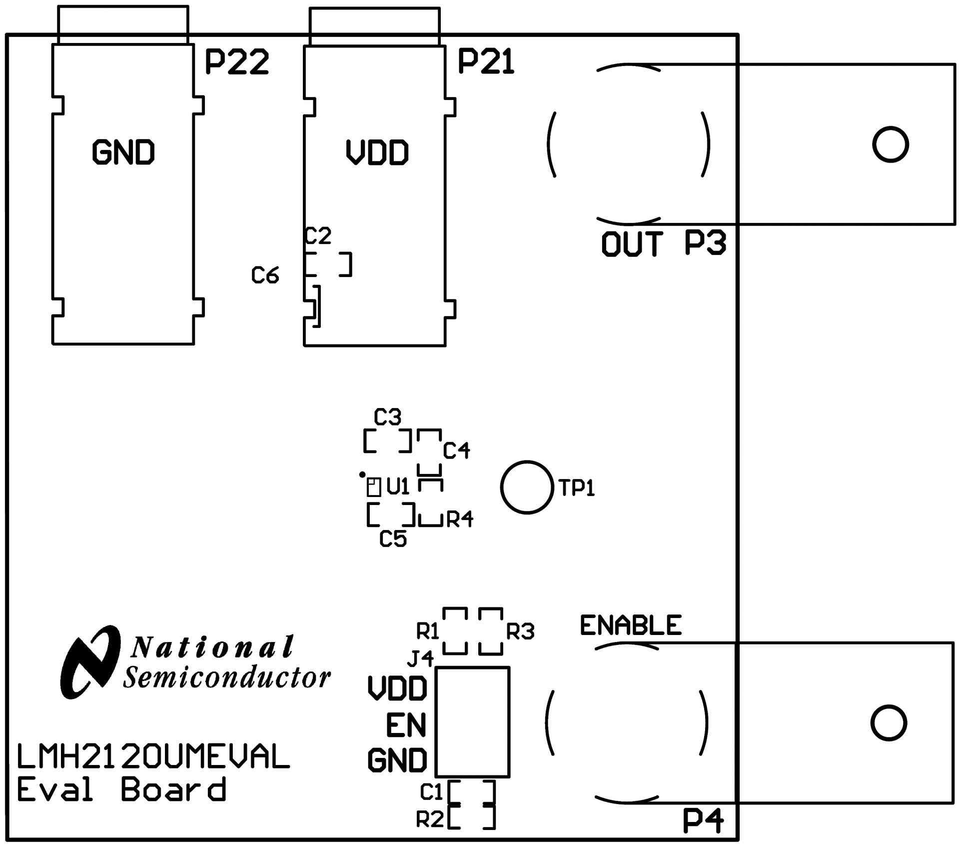

Figure 7. Component Locations of Evaluation Board

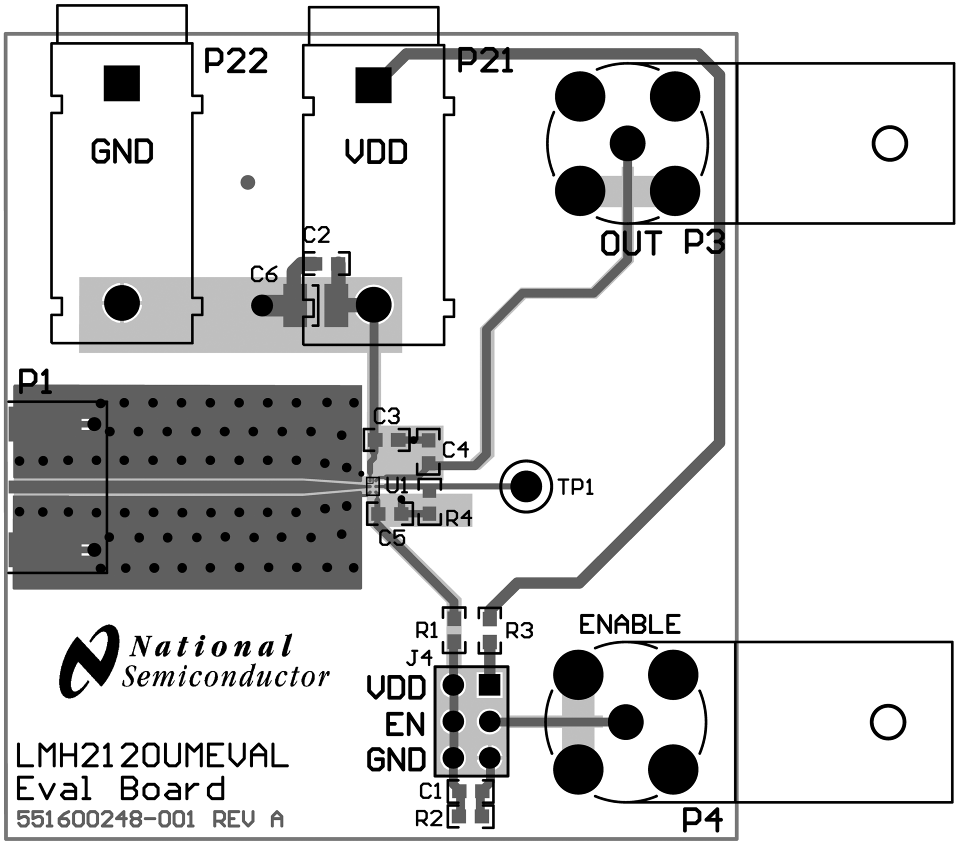

Figure 8. Board Layout of Evaluation Board

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