SN9226 Single-Ended to Differential 2.3 - 2.9 GHz RF Amplifier with Integrated Balun

1 Features

- Single-channel, single-ended input to differential output RF gain block amplifier
- SN9226 supports 2.6 GHz center frequency with 500 MHz 1-dB BW
- 16.5-dB typical gain when driving differential R_{LOAD} = 50-Ω
- 3 dB Noise figure in 1-dB bandwidth
- 33 dBm OIP3 at $P_{OUT/TONE}$ = 2 dBm
- 18-dBm output P1dB into 50-Ω load
- Power consumption < 300 mW on +3.3-V single supply
- Up to 105°C operating temperature

2 Applications

- 5G active antenna systems
- Small cell base stations
- Low-cost radios
- Cellular base station
- Single-ended to differential conversions
- Balun alternatives
- RF gain blocks
- Differential driver for high GSPS ADCs

3 Description

The SN9226 is high-performance, single-channel, single ended input to differential output RF gain block amplifier supporting 2.6 GHz center frequency band with 500 MHz 1-dB Bandwidth (BW). The device is well suited to support requirements for the next generation 5G Active Antenna Systems (AAS) or Small Cell applications where LNA gain is not sufficient to drive full-scale of an analog front-end (AFE). The RF amplifier provides 16.5 dB typical gain with good linearity performance of +33 dBm Output IP3, while maintaining less than 3 dB noise figure across the whole 1dB Bandwidth. The device is internally matched for 50-Ω impedance at the single-ended input. The differential output easily interfaces to a TI transceiver with Zero-IF analog front-end (AFE).

Operating on a single 3.3 V supply, the device consumes about 275 mW of stand-by power making it suitable for high-density 5G massive MIMO applications. Also, the device is available in a space saving 2mm x 2mm, 12-pin WQFN package. The device is rated for an operating temperature of up to 105°C providing a robust system design. There is a 1.8-V JEDEC compliant power down pin available for fast power down and power up of the device suitable for time division duplex (TDD) systems.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN9226	WQFN (12)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

PRODUCT PREVIEW

Single Ended to Differential Amplifier

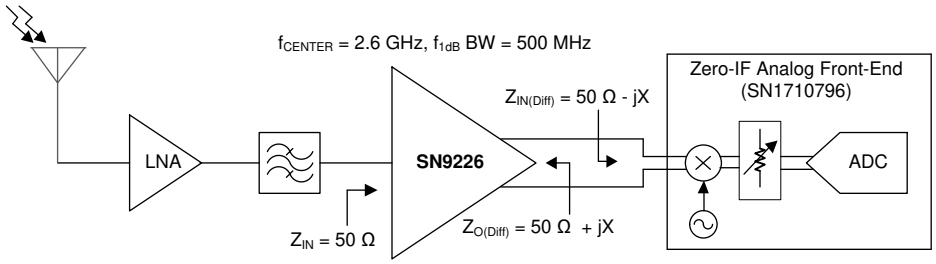


Table of Contents

4 Revision History

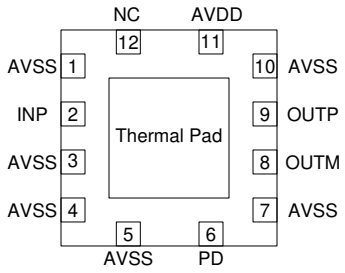
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
TBD	*	Initial release.

PRODUCT PREVIEW

5 Pin Configuration and Functions

RRL Package
12-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	AVSS	Power	Ground
2	INP	Input	RF single-ended input into amplifier
3	AVSS	Power	Ground
4	AVSS	Power	Ground
5	AVSS	Power	Ground
6	PD	Input	Power down connection. PD = 0 V = normal operation; PD = 1.8 V = power off mode.
7	AVSS	Power	Ground
8	OUTM	Output	RF differential output negative
9	OUTP	Output	RF differential output positive
10	AVSS	Power	Ground
11	AVDD	Power	Positive supply voltage (3.3 V)
12	NC	—	Do not connect this pin
Thermal Pad		—	Connect the thermal pad to Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3		V
RF Pins	RFIN, RFOUT+, RFOUT-	–0.3		V
Digital Input PIN	EN	–0.3		V
T_J	Junction temperature			°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins (1)	±TBD	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins (2)	±TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 500-V HBM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ±WWW V and/or ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 250-V CDM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ±YYY V and/or ±ZZZ V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	3.15	3.3	3.45	V
T_A	Ambient temperature	–40		105	°C
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		DEVICE PKG DES (PKG FAM) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_A = +25°C, VDD=3.3V, Center Frequency (F_{in}) = 2.6 GHz, Single-Ended Input Impedance (R_{IN}) = 50 Ω, Differential Output Load (R_{LOAD}) = 50 Ω, $P_{OUT(TOTAL)}$ = 8 dBm (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF PERFORMANCE - SN9226						
F_{RF}	RF frequency range		2350		2850	MHz
BW_{1dB}	1dB Bandwidth	Center Frequency (F_{in}) = 2.6 GHz		500		MHz
S21	Gain	F_{in} = 2.6 GHz		16.5		dB
NF	Noise Figure	F_{in} = 2.6 GHz, R_S = 50 Ω		3		dB
OIP1	Output P1dB	F_{in} = 2.6 GHz, R_{LOAD} = 50 Ω		18.2		dBm
OIP3	Output IP3	F_{in} = 2.6 GHz ± 10 MHz Spacing, $P_{OUT/TONE}$ = 2 dBm		33		dBm
	Differential output Gain Imbalance (1)			±0.5		dB
	Differential output Phase Imbalance (1)			±4		degree
S11	Input return loss	F_{in} = 2.6 GHz, BW = 400 MHz		–9.2		dB
	Single Ended Input Reference Impedance			50		Ω
S22	Differential output return loss	F_{in} = 2.6 GHz, BW = 400 MHz		–9.5		dB
	Differential Ouput Reference Impedance			n/a		Ω

(1) Measured at F_{in}= 2.6GHz, over the BW_{1dB}

PRODUCT PREVIEW

Electrical Characteristics (continued)

T_A = +25°C, VDD=3.3V, Center Frequency (F_{in}) = 2.6 GHz, Single-Ended Input Impedance (R_{IN}) = 50 Ω, Differential Output Load (R_{LOAD}) = 50 Ω, $P_{OUT(TOTAL)}$ = 8 dBm (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
S12	Reverse isolation	F_{in} = 2.6 GHz		–25		dB
CMRR	Common Mode Rejection Ratio (2)			28		dB
Switching and Digital input characteristics						
	Fast Turnon-time			0.5		µs
V_{IH}	High-Level Input Voltage	EN pin	1.4			V
V_{IL}	Low-Level Input Voltage	EN pin			0.5	V
I_{IH}	High-Level Input Current	EN pin		50	250	µA
I_{IL}	Low-Level Input Current	EN pin		2	5	µA
DC current and Power Consumption						
I_{VDD_ON}	Supply Current			84		mA
I_{VDD_PD}	Power Down Current			10		mA
P_{dis}	Power Dissipation on 3.3 V Supply			275		mW

(2) CMRR is calculated using (S21-S31)/(S21+S31) for Receive (1 is input port, 2 & 3 are differential output ports)

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7 Detailed Description

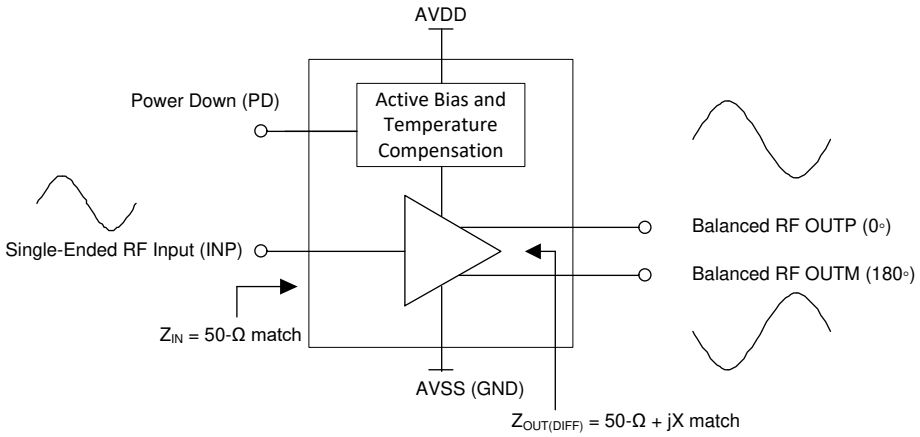
7.1 Overview

The SN9226 is a single-ended input to differential output RF gain block amplifier used in 5G active antenna systems (AAS) for TDD receive application. The device provides ~ 16.5 dB power gain with excellent linearity and noise performance at 2.6 GHz center frequency across the 1dB bandwidth of 500 MHz. The device is internally matched for 50-Ω input impedance. The device differential output matches to a TI transceiver impedance which has Zero-IF analog front end, as shown in Application and Implementation.

The SN9226 has an on-chip active bias circuitry to maintain device performance over a wide temperature and supply voltage range. The included power down function allows the amplifier to shut down and saving power when the amplifier is not needed. Fast shut down and start up enable the amplifier to be used in a host of time division duplex (TDD) applications.

Operating on a single 3.3 V supply and consuming 84 mA of typical supply current, the devices are available in a 2 mm x 2mm 12-pin QFN package.

7.2 Functional Block Diagram



7.3 Feature Description

The SN9226 device is single-ended input to differential output RF amplifier operating at 2.6 GHz to provide active balun functionality. The device integrates the functionality of a single-ended RF amplifier and passive balun in traditional receive applications achieving small form factor with comparable linearity and noise performance, as shown in Figure 1.

The active balun implementation coupled with higher operating temperature of 105°C allows for more robust receiver system implementation compared to passive balun that is prone to reliability failures at high temperatures. The high temperature operation is achieved by the on-chip active bias circuitry which maintains device performance over a wide temperature and supply voltage range.

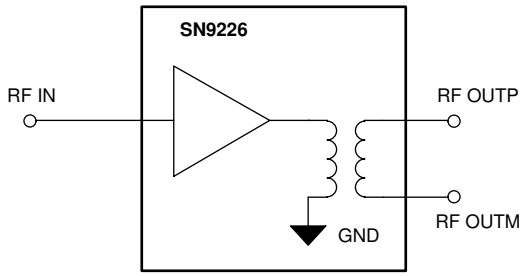


Figure 1. Single-Ended Input to Differential Output, Active Balun Implementation

PRODUCT PREVIEW

7.4 Device Functional Modes

The SN9226 features a PD pin which should be connected to GND for normal operation. For power off mode, connect the PD pin to a logic high voltage of 1.8V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN9226 is a single-ended input to differential output RF gain block amplifier, used in the receive path of a 2.6 GHz center frequency 5G wireless base station. The device replaces the traditional single ended RF amplifier and passive balun offering a smaller foot-print solution to the customer. It is recommended to follow good RF layout and grounding techniques to maximize the device performance.

8.2 Typical Application

The SN9226 is typically used in a four transmit and four receive (4T/4R) array of active antenna system for 5G TDD wireless base station applications. A single receive channel of such a system (see Figure 2) consists of a low noise amplifier (LNA) that sits close to the antenna and drives the signal into a long single-ended 50 Ω coaxial cable. The SN9226 converts this single ended RF signal received from the coax into differential signal offering low noise and distortion performance while interfacing with the receiver analog front-end (AFE).

It is important that the SN9226 input impedance is matched to 50 Ω to prevent any signal reflections due to the long coax cable. The device differential output interfaces directly with the differential input of TI Zero-IF analog front end without the need of any external matching components. The matching is optimized for 2.6 GHz center frequency with 500MHz of 1dB Bandwidth.

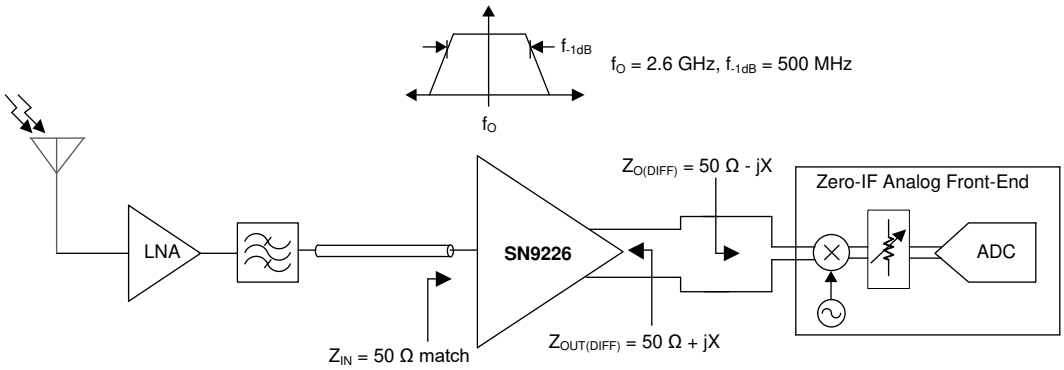


Figure 2. SN9226 in Receive application driving an Analog Front-End

PRODUCT PREVIEW

Typical Application (continued)

8.2.1 Design Requirements

8.2.2 Detailed Design Procedure

8.2.3 Application Curves

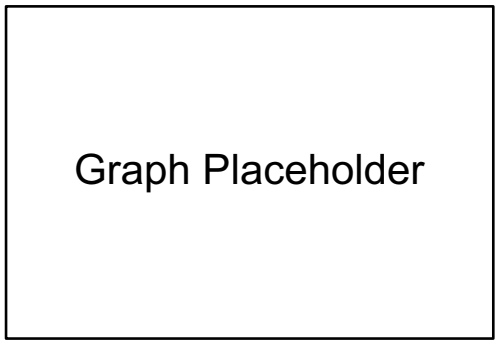


Figure 3.

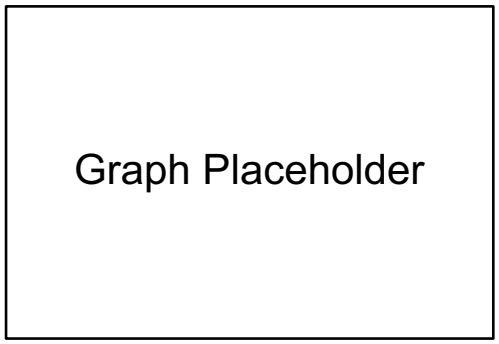


Figure 4.

9 Power Supply Recommendations

The SN9226 device operates on a common nominal 3.3 V supply voltage. It is recommended to isolate the supply voltage through decoupling capacitors placed close to the device. Select capacitors with self-resonant frequency near the application frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device.

10 Layout

10.1 Layout Guidelines

10.2 Layout Example

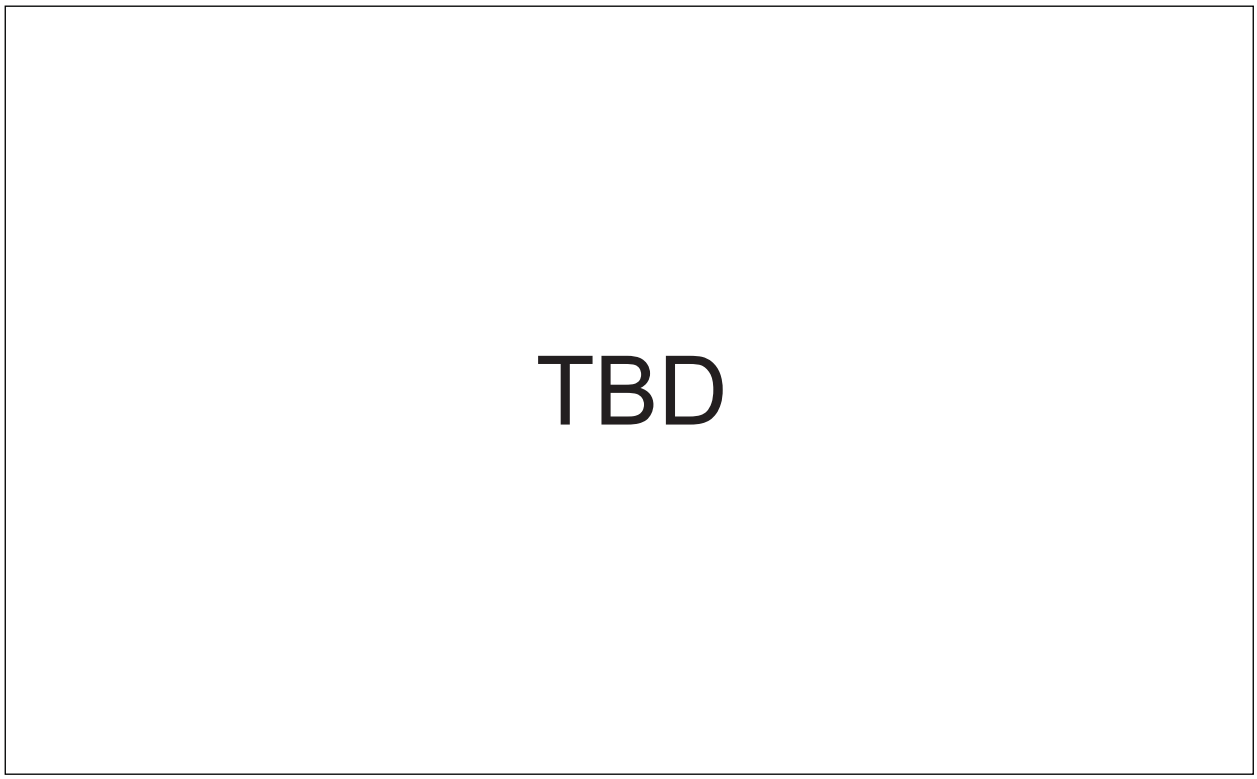


Figure 5.

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

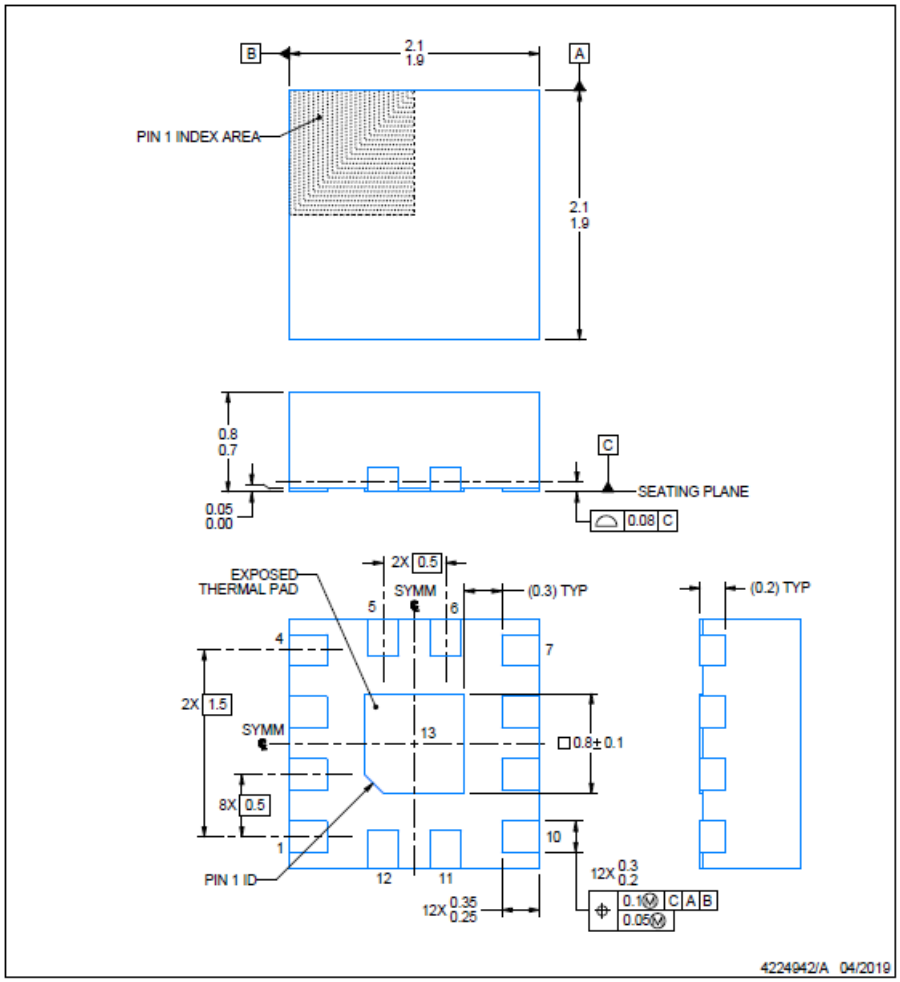
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RRL0012A **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

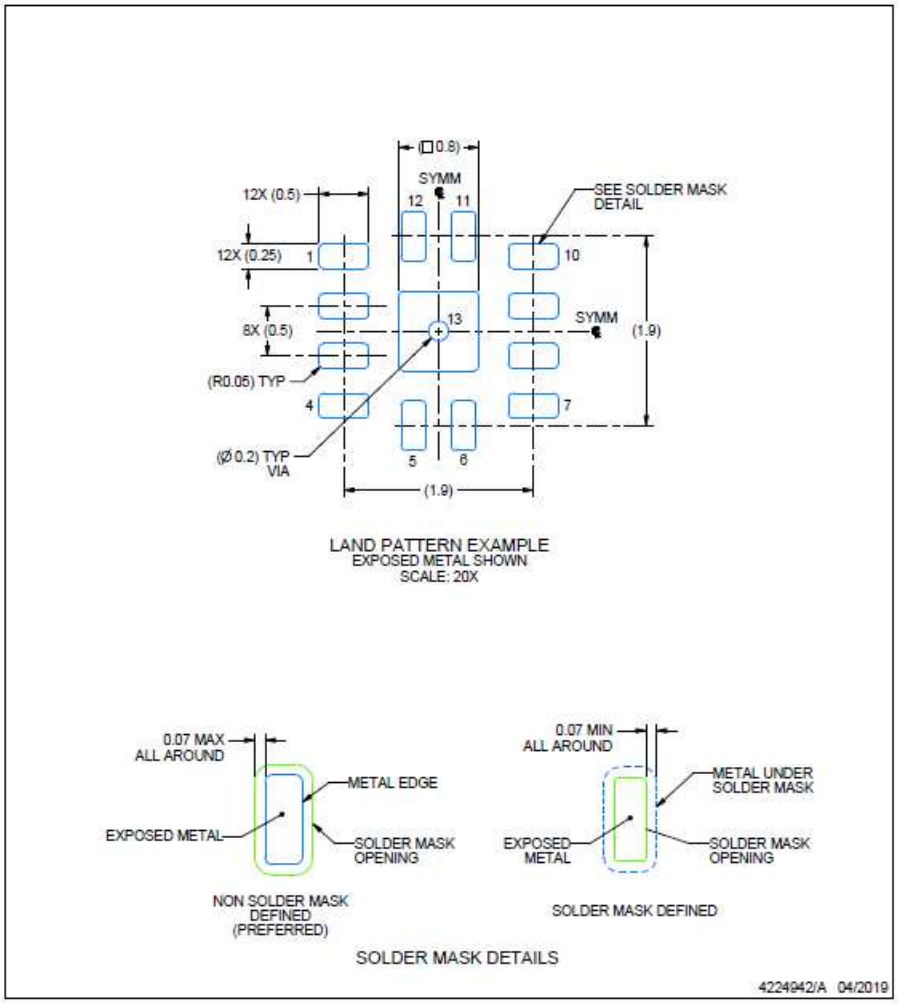
TEXAS INSTRUMENTS
www.ti.com

PRODUCT PREVIEW

EXAMPLE BOARD LAYOUT

RRL0012A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



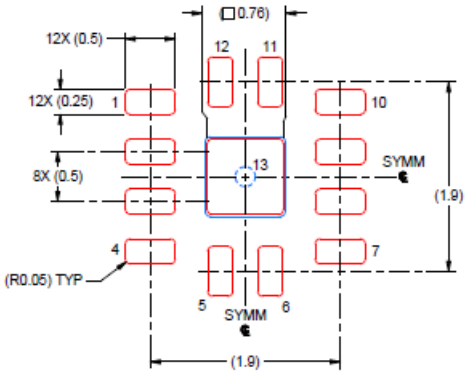
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RRL0012A **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 13
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224942/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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