

SN9226 Single-Ended to Differential 2.3 - 2.9 GHz ADC Driver with Integrated Balun

1 Features

- Single Channel, Single Ended 50 Ω Input to Differential 50/100 Ω Output RF Gain Block Amplifier
- Internally Matched to Drive TI's AFE77xx Family of AFE Devices Without External Matching Components
- SN9226 Supports 2.6 GHz Center Frequency With 700 MHz 1 dB BW
- 16.5 dB Typical Gain
- 3 dB Noise Figure in 1 dB Bandwidth
- 35 dBm OIP3 at P_{OUT/TONE} = 2 dBm
- 17.5 dBm Output P1dB
- 275 mW Power Consumption on +3.3 V Single Supply
- Up to T_A = 105°C Operating Temperature

2 Applications

- 5G m-MIMO TDD Systems
- Small Cell Base Stations
- · Low-cost Radios
- Cellular Base Station
- · Single-ended to Differential Conversions
- Balun Alternatives
- RF Gain Blocks
- Differential Driver for High GSPS ADCs

3 Description

The SN9226 is a high performance, single channel, single ended 50 Ω input to differential 50 Ω or 100 Ω output RF gain block amplifier supporting 2.6 GHz center frequency band with more than 400 MHz 1 dB Bandwidth (BW). It can drive Tl's AFE77xx family of AFE devices without any external matching components. The device is well suited to support requirements for the next generation 5G m-MIMO or Small Cell base station applications, where it is used as the last stage to drive the full-scale differential input of an analog front-end (AFE) or ADC.

The device provides 16.5 dB typical gain with good linearity performance of +35 dBm Output IP3 at 2.6 GHz. The noise figure of less than 3 dB is maintained across the whole 1 dB Bandwidth. The device is internally matched for 50 Ω impedance at the single-ended input.

Operating on a single 3.3 V supply, the device consumes about 275 mW of active power making it suitable for high-density 5G massive MIMO applications. Also, the device is available in a space saving 2.00 mm x 2.00 mm, 12-pin WQFN package. The device is rated for an operating temperature of up to $T_A = 105\,^{\circ}\text{C}$ providing a robust system design. There is a 1.8 V JEDEC compliant power down pin available for fast power down and power up of the device suitable for time division duplex (TDD) systems.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN9226	WQFN (12)	2.00 mm × 2.00 mm

 For all available packages, see the orderable addendum at the end of the data sheet.

SN9226: 2.3 to 2.9 GHz Single Ended Input to Differential Output RF Gain Block Amplifier

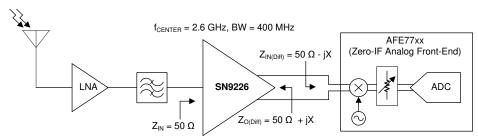




Table of Contents

1	Features 1	7.3 Feature Description
2	Applications 1	7.4 Device Functional Modes10
3	Description 1	8 Application and Implementation 11
4	Revision History2	8.1 Application Information11
5	Pin Configuration and Functions	8.2 Typical Application11
6	Specifications	9 Power Supply Recommendations 14
•	6.1 Absolute Maximum Ratings	10 Layout 15
	6.2 ESD Ratings	10.1 Layout Guidelines
	6.3 Recommended Operating Conditions	10.2 Layout Example
	6.4 Thermal Information	11 Device and Documentation Support 16
	6.5 Electrical Characteristics	11.1 Receiving Notification of Documentation Updates 16
	6.6 Typical Characteristics	11.2 Trademarks
7	Detailed Description 9	11.3 Electrostatic Discharge Caution
-	7.1 Overview	12 Mechanical, Packaging, and Orderable
	7.2 Functional Block Diagram	Information 16
		12.1 Package Option Addendum20

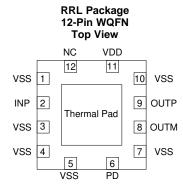
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2020	*	Initial Release



5 Pin Configuration and Functions



Pin Functions

	PIN I/O		DESCRIPTION	
NO.	NAME	1/0	DESCRIPTION	
1	VSS	Power	Analog Ground	
2	INP	Input	RF single-ended input into amplifier	
3	VSS	Power	Analog Ground	
4	VSS	Power	Analog Ground	
5	VSS	Power	Analog Ground	
6	PD	Input	Power down connection. PD = 0 V = normal operation; PD = 1.8 V = power off mode.	
7	VSS	Power	Analog Ground	
8	OUTM	Output	RF differential output negative	
9	OUTP	Output	RF differential output positive	
10	VSS	Power	Ground	
11	VDD	Power	Positive supply voltage (3.3 V)	
12	NC	_	Do not connect this pin	
13	Thermal Pad	_	Connect the thermal pad to Ground (VSS)	



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VDD	-0.3		V
RF Pins	INP, OUTP, OUTM	-0.3	VDD	V
Digital Input PIN	PD	-0.3	VDD	V
Continuous wave (CW) overload	f _{in} = 2.6 GHz at INP		25	dBm
Junction temperature	TJ		150	°C
Storage temperature	T _{stg}	-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
	Floatroatatia diaaharga	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins ⁽¹⁾	±1000	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins (2)	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	3.15	3.3	3.45	V
T _A	Ambient temperature	-40		105	°C
TJ	Junction temperature	-40		125	°C

6.4 Thermal Information

		SN9226	
	THERMAL METRIC ⁽¹⁾	RRL PKG	UNIT
		12-PIN WQFN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.2	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

STRUMENTS

 T_A = +25°C, VDD = 3.3 V, Center Frequency (f_{in}) = 2.6 GHz, Single-Ended Input Impedance (Z_{IN}) = 50 Ω , Differential Output Impedance (Z_{LOAD}) = Default (driving Tl's AFE77xx family of devices⁽¹⁾) , $P_{OUT(TOTAL)}$ = 8 dBm (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
RF PERF	ORMANCE				
f _{RF}	RF frequency range		2300	2900	MHz
BW _{1dB}	1dB Bandwidth	Center Frequency (f _{in}) = 2.6 GHz	700		MHz
S ₂₁	Gain	f_{in} = 2.6 GHz, Z_{LOAD} = Default or 100 Ω matched	16.5		dB
NF	Noise Figure	f_{in} = 2.6 GHz, Z_{SOURCE} = 50 Ω	2.9		dB
OP1dB	Output P1dB	f _{in} = 2.6 GHz, Z _{LOAD} = Default	17.5		dBm
OIP3	Output IP3	f _{in} = 2.6 GHz ± 10 MHz Spacing, P _{OUT/TONE} = 2 dBm	35		dBm
	Differential output Gain Imbalance	f _{in} = 2.6 GHz	±0.5		dB
	Differential output Phase Imbalance	f _{in} = 2.6 GHz	±4		degree
S ₁₁	Input return loss	f_{in} = 2.6 GHz, BW = 400 MHz, Z_{LOAD} = Default or 100 Ω matched	-9.2		dB
Z_{IN}	Single Ended Input Reference Impedance		50		Ω
0	Differential entertaint and an	f _{in} = 2.6 GHz, BW = 400 MHz, Z _{LOAD} = Default	-9.5		dB
S ₂₂	Differential output return loss	f_{in} = 2.6 GHz, BW = 400 MHz, Z_{LOAD} = 100 Ω matched	-10.0		dB
S ₁₂	Reverse isolation	f_{in} = 2.6 GHz, Z_{LOAD} = Default or 100 Ω	-35		dB
CMRR	Common Mode Rejection Ratio (2)		28		dB
Switchin	g and Digital input characteristics			•	
t _{ON}	Turn-on time	50% V _{PD} to 90% RF	0.5		μs
t _{OFF}	Turn-off time	50% V _{PD} to 10% RF	0.2		μs
V_{IH}	High-Level Input Voltage	PD pin	1.4		V
V _{IL}	Low-Level Input Voltage	PD pin		0.5	V
I _{IH}	High-Level Input Current	PD pin	50	250	μΑ
I _{IL}	Low-Level Input Current	PD pin	2	5	μA
DC curre	ent and Power Consumption				
I_{VDD_ON}	Supply Current - Active	$V_{PD} = 0 V$	80		mA
I_{VDD_PD}	Supply Current - Power Down	V _{PD} = 1.8 V	7		mA
P_{dis}	Power Dissipation - Active	VDD = 3.3 V	265		mW

Example: AFE7700, AFE7769, AFE7786, AFE7798, AFE7799

6.6 Typical Characteristics

At $T_A = 25$ °C, VDD = 3.3 V, Center Frequency (f_{IN}) = 2.6 GHz, Single-Ended input impedance (Z_{IN}) = 50 Ω , Differential Output impedance (Z_{LOAD}) Default (driving TI's AFE77xx family of devices) and $P_{OUT(TOTAL)} = 8$ dBm into Z_{LOAD} (unless otherwise

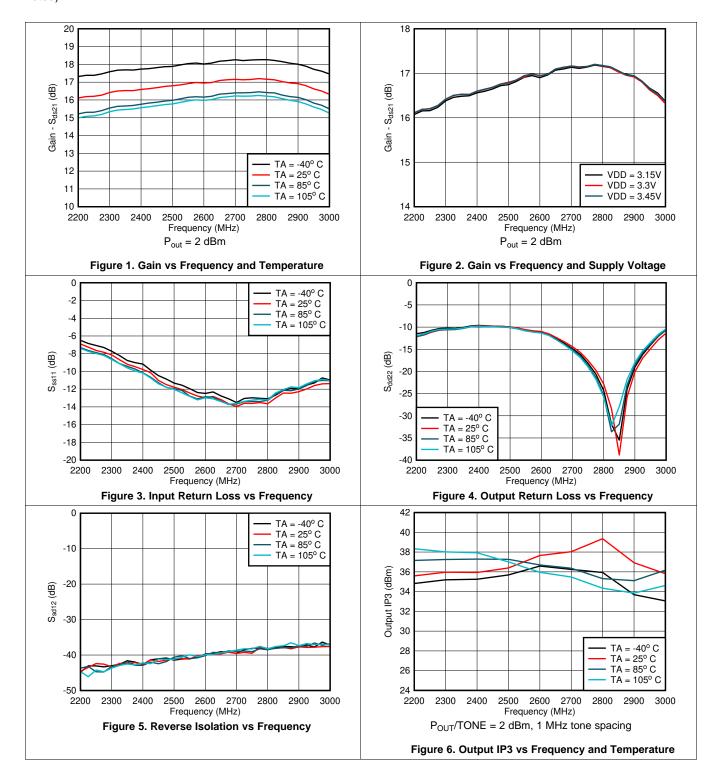
CMRR is calculated using (S₂₁-S₃₁)/(S₂₁+S₃₁) for Receive (1 is input port, 2 & 3 are differential output ports)



Typical Characteristics (continued)

At T_A = 25°C, VDD = 3.3 V, Center Frequency (f_{IN}) = 2.6 GHz, Single-Ended input impedance (Z_{IN}) = 50 Ω , Differential Output impedance (Z_{LOAD}) Default (driving TI's AFE77xx family of devices) and $P_{OUT(TOTAL)}$ = 8 dBm into Z_{LOAD} (unless otherwise noted).

noted).

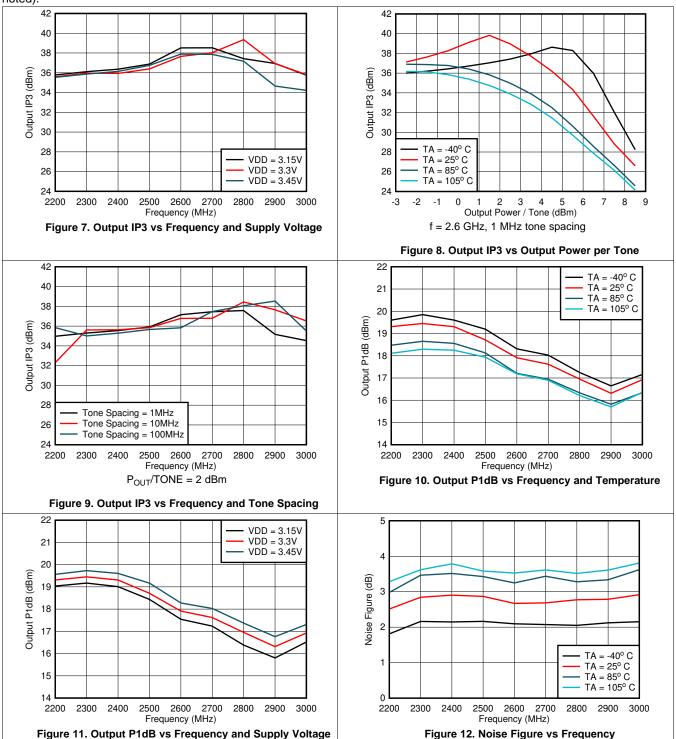




www.ti.com

Typical Characteristics (continued)

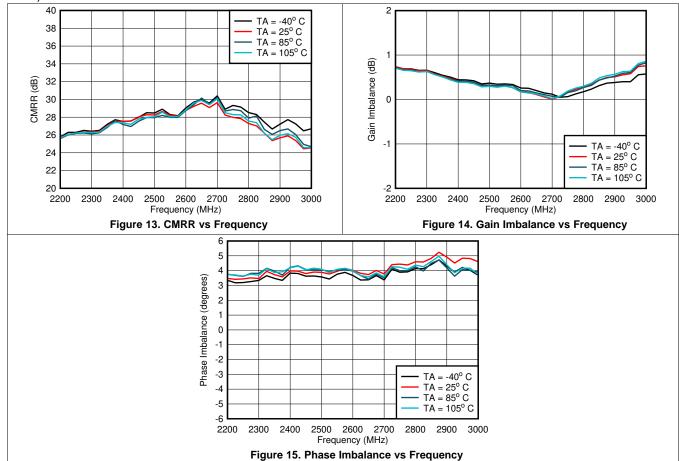
At $T_A = 25^{\circ}\text{C}$, VDD = 3.3 V, Center Frequency (f_{IN}) = 2.6 GHz, Single-Ended input impedance (Z_{IN}) = 50 Ω , Differential Output impedance (Z_{LOAD}) Default (driving Tl's AFE77xx family of devices) and $P_{\text{OUT}(\text{TOTAL})} = 8$ dBm into Z_{LOAD} (unless otherwise noted).





Typical Characteristics (continued)

At T_A = 25°C, VDD = 3.3 V, Center Frequency (f_{IN}) = 2.6 GHz, Single-Ended input impedance (Z_{IN}) = 50 Ω , Differential Output impedance (Z_{LOAD}) Default (driving TI's AFE77xx family of devices) and $P_{OUT(TOTAL)}$ = 8 dBm into Z_{LOAD} (unless otherwise noted).





7 Detailed Description

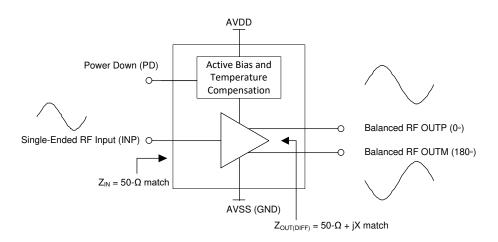
7.1 Overview

The SN9226 is a single-ended 50 Ω input to differential 50 Ω or 100 Ω output RF gain block amplifier used in 5G m-MIMO base station for TDD receive application. The device provides \approx 16.5 dB power gain with excellent linearity and noise performance at 2.6 GHz center frequency across the bandwidth of 400 MHz. The device is internally matched to drive Tl's AFE77xx family of AFE devices. The device's differential output impedance matches to the input impedance of AFE77xx transceiver which has Zero-IF analog front end, as shown in Application and Implementation. The differential output can interface to standard 50 Ω or 100 Ω impedance with external matching circuitry at 2.6 GHz. See Typical Application for differential 50 Ω or 100 Ω output matching interface information.

The SN9226 has an on-chip active bias circuitry to maintain device performance over a wide temperature and supply voltage range. The included power down function allows the amplifier to shut down and save power when the amplifier is not needed. Fast shut down and start up enables the amplifier to be used in a host of time division duplex (TDD) applications.

Operating on a single 3.3 V supply and consuming 84 mA of typical supply current, the devices are available in a 2 mm x 2 mm 12-pin QFN package.

7.2 Functional Block Diagram



7.3 Feature Description

The SN9226 device is a single-ended 50 Ω input to differential 50 Ω or 100 Ω output RF gain block amplifier operating at 2.6 GHz to provide active balun functionality. The device integrates the functionality of a single-ended RF amplifier and passive balun in traditional receive applications achieving small form factor with comparable linearity and noise performance, as shown in Figure 16.

The active balun implementation coupled with higher operating temperature of 105°C allows for more robust receiver system implementation compared to passive balun that is prone to reliability failures at high temperatures. The high temperature operation is achieved by the on-chip active bias circuitry which maintains device performance over a wide temperature and supply voltage range.



Feature Description (continued)

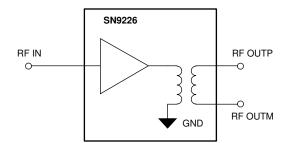


Figure 16. Single-Ended Input to Differential Output, Active Balun Implementation

7.4 Device Functional Modes

The SN9226 features a PD pin which should be connected to GND for normal operation. For power off mode, connect the PD pin to a logic high voltage of 1.8 V.



8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN9226 is a single-ended 50 Ω input to differential 50 Ω or 100 Ω output RF gain block amplifier, used in the receive path of a 2.6 GHz center frequency 5G wireless base station. The device replaces the traditional single ended RF amplifier and passive balun offering a smaller foot-print solution to the customer. It is recommended to follow good RF layout and grounding techniques to maximize the device performance.

8.2 Typical Application

The SN9226 is typically used in a four transmit and four receive (4T/4R) array of active antenna system for 5G TDD m-MIMO or Small cell base station applications. A single receive channel of such a system (see Figure 17) consists of a low noise amplifier (LNA) that sits close to the antenna and drives the signal into a long single-ended 50 Ω coaxial cable. The SN9226 converts this single ended RF signal into differential signal offering low noise and distortion performance while interfacing with the receiver analog front-end (AFE).

It is important that the SN9226 input impedance is matched to 50 Ω to prevent any signal reflections due to the long coax cable. The device differential output interfaces directly with the differential input of AFE77xx device (Tl's Zero-IF analog front end) without the need of any external matching components (see Figure 17). The matching is optimized for 2.6 GHz center frequency with 400 MHz of Bandwidth.

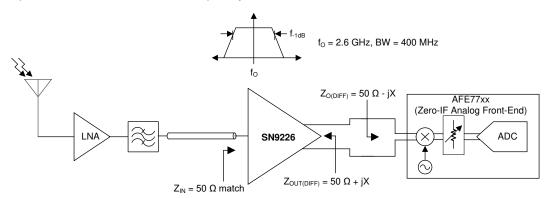


Figure 17. SN9226 in Receive application driving a TI Analog Front-End

For interfacing with 100 Ω differential input analog front-end, an external matching circuitry can be used close to the SN9226 output as shown in Figure 18. Table 1 shows example recommended component values while transforming the SN9226 output impedance from 50 Ω to 100 Ω . The component values for 100 Ω matching scenario will need to be tweaked on board depending upon the trace length between the matching circuitry and the analog front end input. It is important to select LC component values with Q (min) > 30 and that have the self resonant frequency (SRF) sufficiently higher than the desired frequency of operation. The graphs in the section Application Curves give the performance of SN9226 device with different terminations. When driving TI's AFE77xx devices, SN9226 gives slightly higher gain (approximately 0.5 dB) than when driving a 100 Ω matched load.



Typical Application (continued)

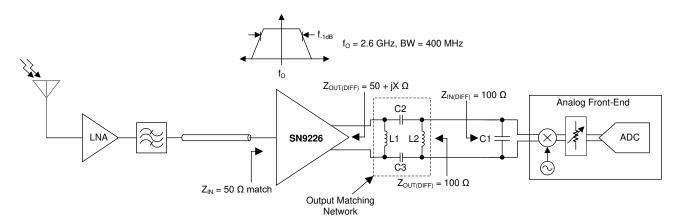


Figure 18. SN9226 in Receive application with 100 Ω matching

Table 1. Recommended Component values for 100 Ω matching

Component	Values
L1	3.4 nH
L2	4.3 nH
C2, C3	2.4 pF

8.2.1 Design Requirements

Table 2 shows example design requirements for an RF amplifier in a typical 5G, active antenna TDD system. The SN9226 meets these requirements.

Table 2. Design Parameters

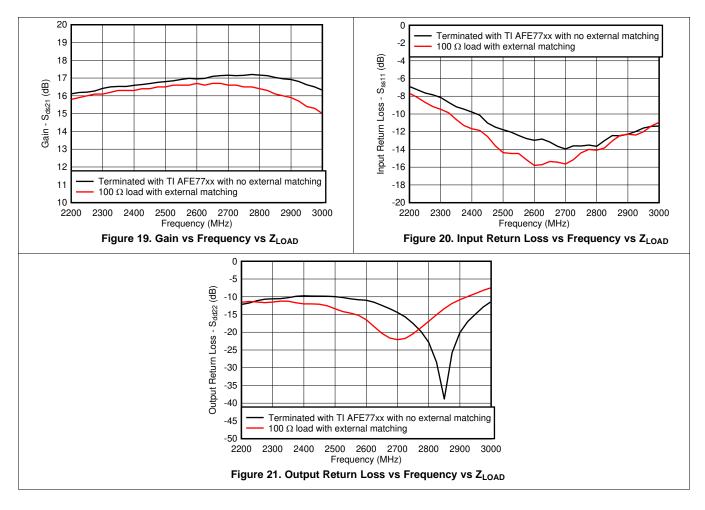
DESIGN PARAMETERS	EXAMPLE VALUE
Frequency range and 1-dB BW	2300 MHz to 2900 MHz with 400 MHz of 1-dB BW
Configuration	Single-ended 50- Ω input to differential 50- Ω output
Power gain	> 15 dB
Output IP3 at P _{OUT/TONE} = 2 dBm	> 32 dBm
Noise figure at $Zin = 50 \Omega$	< 4 dB
Output P1dB	< 17 dBm
Power consumption	< 350 mW
Turn-on time	< 1 µs
Package size	2 mm × 2 mm ²



www.ti.com

8.2.2 Application Curves

Given below are the gain and return loss curves for different output terminations.





9 Power Supply Recommendations

The SN9226 device operates on a common nominal 3.3 V supply voltage. It is recommended to isolate the supply voltage through decoupling capacitors placed close to the device. Select capacitors with self-resonant frequency near the application frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device.



10 Layout

10.1 Layout Guidelines

When dealing with an RF amplifier with relatively high gain and a center frequency of 2.6 GHz, certain board layout precautions must be taken to ensure stability and optimum performance. TI recommends that the SN9226 board be multi-layered to improve thermal performance, grounding, and power-supply decoupling. Figure 22 shows a good layout example. In Figure 22, only the top signal layer and its adjacent ground reference plane are shown.

- Excellent electrical connection from the thermal pad to the board ground is essential. Use the recommended footprint, solder the pad to the board, and do not include a solder mask under the pad.
- Connect the pad ground to the device terminal ground on the top board layer.
- Verify that the return DC and RF current path have a low impedance ground plane directly under the package and that the RF signal traces into and out of the amplifier.
- Ensure that ground planes on the top and any internal layers are well stitched with vias.
- Do not route RF signal lines over breaks in the reference ground plane.
- · Avoid routing clocks and digital control lines near RF signal lines.
- Do not route RF or DC signal lines over noisy power planes. Ground is the best reference, although clean power planes can also serve where necessary.
- Place supply decoupling close to the device.
- The differential output traces must be symmetrical in order to achieve the best linearity performance.

A board layout software package can simplify the trace width design to maintain impedances for controlled impedance signals. To isolate the affect of board parasitic on frequency response, TI recommends placing the external output matching resistors close to the amplifier output pins. See the *LMH9226 Evaluation Module* user guide for more details on board layout and design. SN9226 device is pin compatible and functionally identical to LMH9226. The difference is that SN9226 device does not need external matching components when interfacing with TI's AFE77xx transceiver chips.

10.2 Layout Example

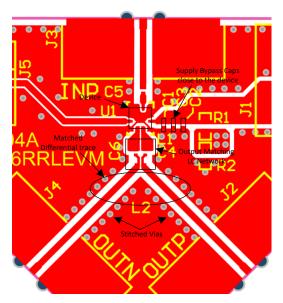


Figure 22. Supply Bypass and Output Matching



11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



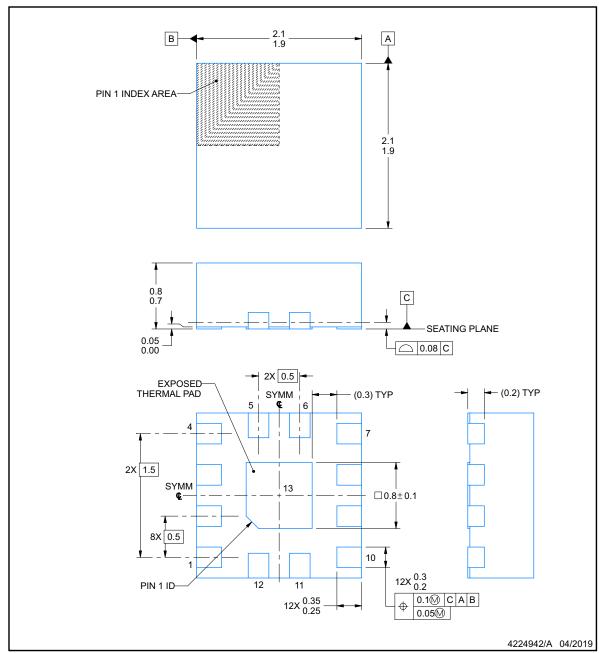
RRL0012A



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



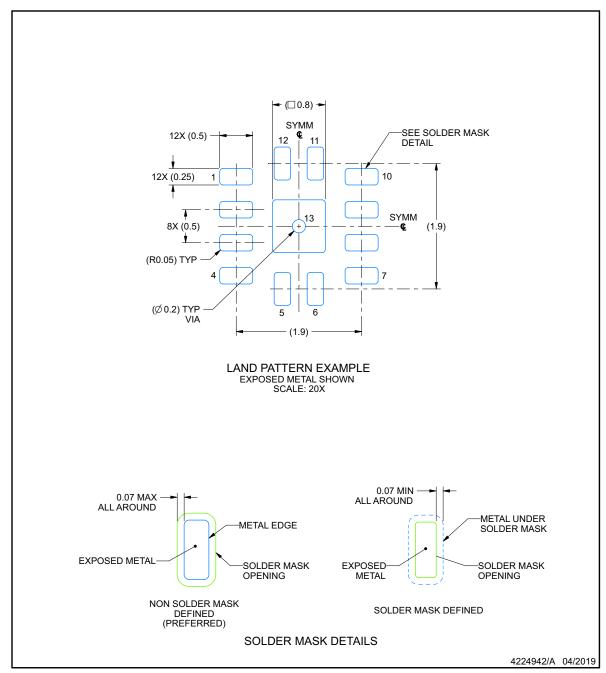


EXAMPLE BOARD LAYOUT

RRL0012A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



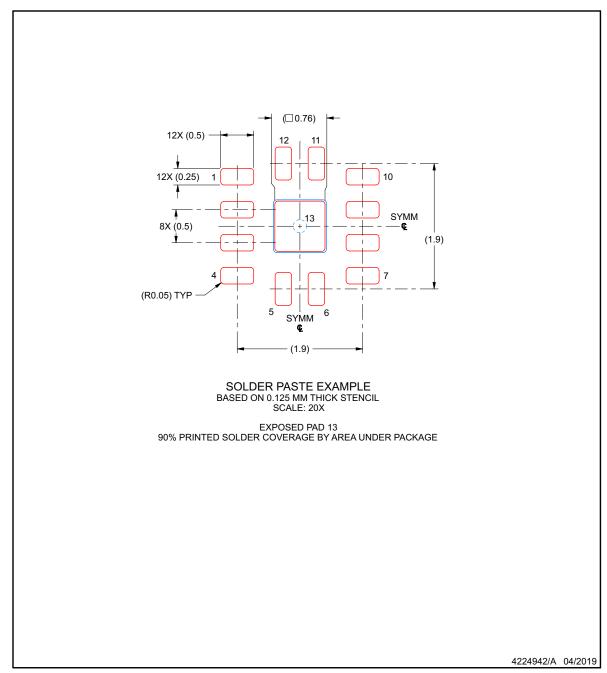


EXAMPLE STENCIL DESIGN

RRL0012A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





12.1 Package Option Addendum

12.1.1 Packaging Information

Package Package Package Lead/Ball Eco Plan (2) **Orderable Device** Status (1) Pins MSL Peak Temp (4) Op Temp (°C) Device Marking (5)(6) Finish (3) Type Drawing Qty Green (RoHS Level-2-260C-1 SN9226IRRLR **ACTIVE** RRI **CU NIPDAU** WQFN 12 3000 -40 to 125 26AO & no Sb/Br) YEAR

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

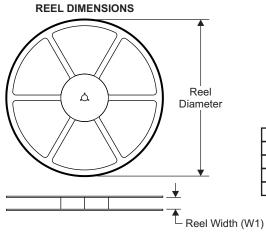
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



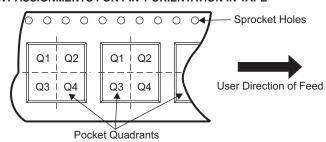
www.ti.com

12.1.2 Tape and Reel Information



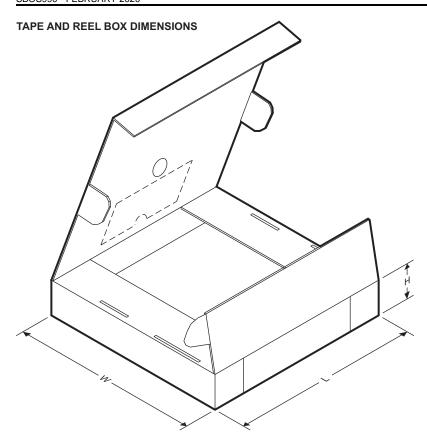
A0	Dimension designed to accommodate the component width
В0	
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN9226IRRLR	WQFN	RRL	12	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2





Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN9226IRRLR	WQFN	RRL	12	3000	195	200	45	

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Tl's products are provided subject to Tl's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such Tl products. Tl's provision of these resources does not expand or otherwise alter Tl's applicable warranties or warranty disclaimers for Tl products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2020, Texas Instruments Incorporated