RF Rx 2.6ghz Balun: Electrical Characteristics

Parameter	Unit	Test condition	RF Rx 2.6ghz Balun		
			Min	Typ	Max
Feature	TDD	/		Yes	
	Bypass	/		Yes	
★ Operating Frequency Ranges	MHz		2300		2900
★ Gain	dB	LNA On state		16.5	
		LNA Off state			
★ (Bypass on)	dB	Bypass On			
In band ripple/ every 100M	dB	/		0.5	
★Out Band Gain	dB	LNA On state			
★ Supply Current	A	LNA On state		0.084	
		LNA Off state		0.01	
★Supply Voltage	V	LNA On state	3.15	3.3	3.45
		LNA Off state			
★ Input Power	dBm	LNA On state			25
		LNA Off state			
★Input Return Loss	dB	LNA On state, PVT		-9.2	
		LNA Off state, PVT			
		Bypass On, PVT			
★Output Return Loss	dB	LNA On state, PVT		-9.5	
		LNA Off state, PVT			
		Bypass On, PVT			
★ Noise Factor	dB	25℃/ PVT		3	
★ Output P1dB	dBm	LNA On state, PVT		17.5	
		Bypass On, PVT			
★Output IP3	dBm	LNA On state, PVT		33	
		Bypass On, PVT			
Isolation（Pin≤20dBm）	dB	LNA Off state, PVT			
Amplitude imbalance	dB	LNA On state, PVT		0.5	
Phase imbalance	Deg	LNA On state, PV		4	

Reverse isolation	dB	LNA On state, PVT		30	
Enable Voltage	V	LNA On state, PVT			0.5
		LNA Off state, PVT	1.4		
		Bypass On, PVT			
		Bypass Off, PVT			
Enable Current	mA			0.05	0.25
Turn on time （Vctrol 50%->90% RF out）	us	LNA off to LNA on,PVT		0.5	
		Bypass on to LNA on,PVT			
		LNA on to Bypass on ,PVT			
Turn on time （Vctrol 50%->99% RF out）	us	LNA off to LNA on,PVT		1	
		Bypass on to LNA on,PVT			
		LNA on to Bypass on ,PVT			
Turn off time （Vctrol 50%->10% RF out）	us	LNA on to LNA off,PVT		0.1	
Turn off time （Vctrol 50%->1% RF out）	us	LNA on to LNA off,PVT		0.15	
Control Voltage True Table			0~0.5V on 1.4V~VDD off		
Maximum input power	dBm	PVT	25		
< 12G No oscillation	-	PVT		Yes	
Spur during on or off state.	dBm	PVT		No glitch	
VSWR	/				
maximum Junction Temperature	℃	PV	150		
★Operating Temperature Range	℃	PV	-40~105		
★ Storage Temperature Range	℃	P	-60~150		
θ jc	℃	PV	14.2°C/W		
★ Lifetime at max. Tj	Years	PVT，on state，offs tate	10		
★ESD-HBM, for all pin	V	PVT, 500V	1000V		
ESD-CDM	V	PVT, 250V	500V		

★ MSL, Moisture Sensitive Level	/	PVT, ≤MSL3	MSL2
Package	mm*mm		2.1*2.1
Stress for device	N	Refer to basestation production spec Including top pressure and side pressure	
★ Reflow Requirement SMD package should do reflow(profile refer to J-STD-020D) before ATE If the chip has done reflow during the assembly process, don't need to add reflow again			TI doesn't reflow in the assembly flow before ATE. Please follow J-STD_020D.
No power up sequence rqmt			Yes

Parameters	**Test or No**	**TI feedback**
Frequency Range	must	No
（current leakage for power pin）	must	Yes
Gain	must	Covered for outliers
NF	must	No
Stability	must	Yes, large signal oscillations in band is covered
VSWR	must	No
OIP3	must	IMD3 Covered for outliers
OP-1dB	must	No