**TI204c Capture Setup for AFE79xx (8 Tx and 8 Rx lanes @ 9.8304 Gbps)**

**The following steps outline the high level flow for the data capture**

1. **Launch and configure the Latte GUI first**
2. **Configure LMK04828 clocking device on AFE EVM**
3. **Launch and configure the FPGA through Vivado**
4. **Configure AFE through Latte GUI**
5. **Release Rx reset and capture Rx data through Vivado**
6. **Launch HSDC Pro and the Dynamic Refresh Control GUI for displaying and Rx analyzing data**

**Please follow the rest of the document in order.**

**Hardware connections:**

AFE7900EVM:

Mode:

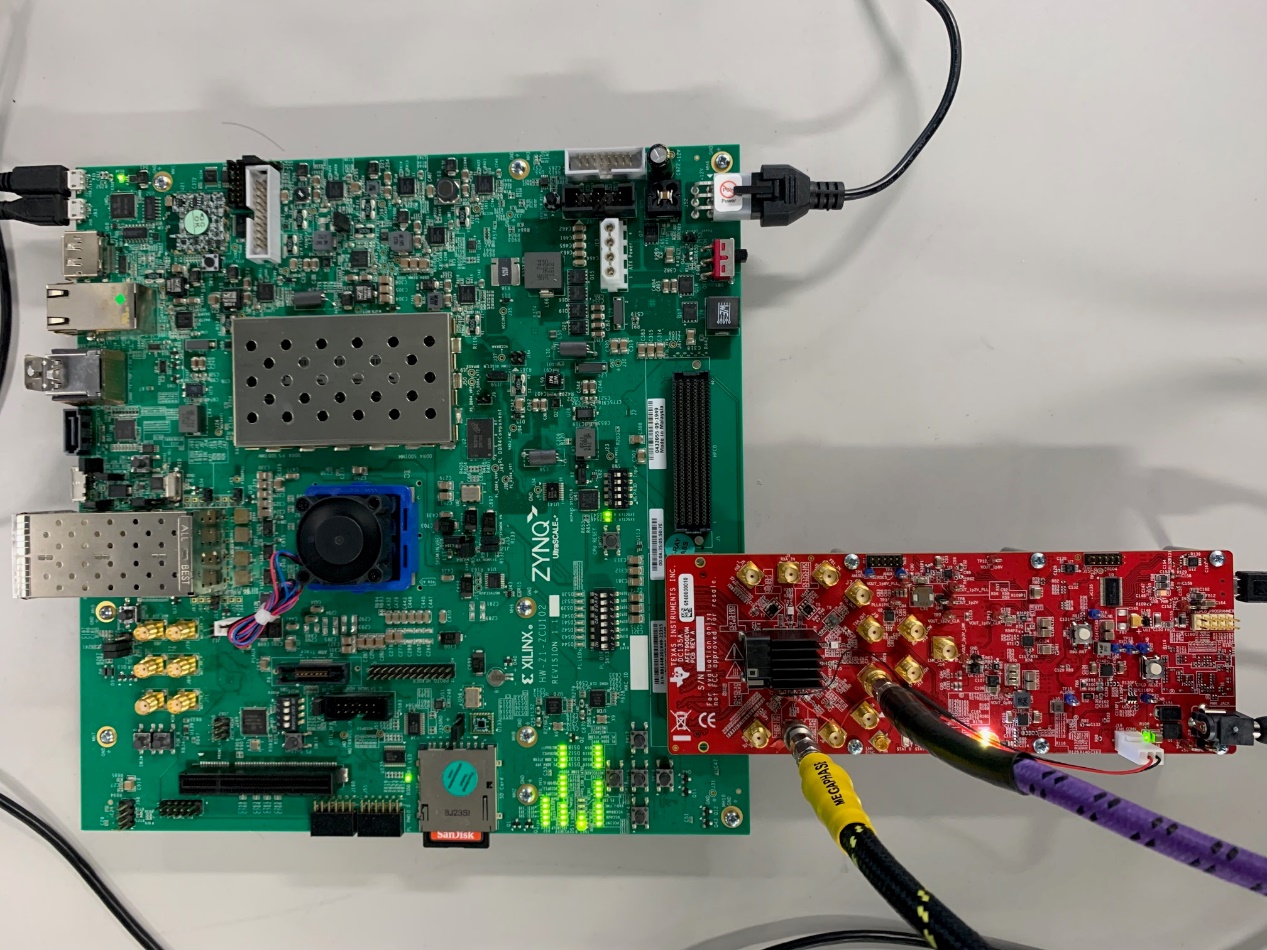
RX: Fs = 2.94912 GSPS, decimate-by-4 complex,

TX: Fs = 8.84736 GSPS, interpolate-by-12 complex

1. Connect a 5V, 5A power supply to power jack J18. Do not use a supply that is rated less than 5A.
2. Connect a USB cable to the USB connector (J19 on the bottom side of board).
3. Connect an analog RF signal set to 1830MHz and -5dBm from a signal source to the RXD\_IN SMA (J2).
4. Connect TXD\_OUT SMA (J8) to a spectrum analyzer.

ZCU102:

1. Connect Xilinx supplied power adapter.
2. Connect both JTAG and UART USBs to PC.
3. Connect FMC connector J4, HPC1, of ZCU102 to FMC connector of AFE79xxEVM.



AFE7900EVM connected to ZCU102

**Software installation:**

1. Download and install HSDC Pro software from:

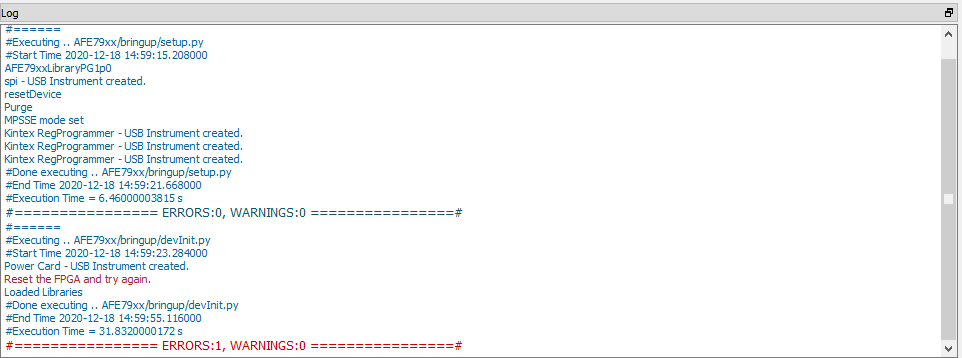
https://www.ti.com/tool/DATACONVERTERPRO-SW

1. Download and install Latte software from AFE79xx secure folder: ti.com/mysecureSoftware. (Read section 1 of “AFE79XX\_Latte\_UserGuide.pdf” in secure folder. It’s a short introduction to latte.)
2. Copy “bringup” folder in ‘AFE config files’ to C:\Users\<User\_name>\Documents\Texas Instruments\Latte\projects\AFE79xx
3. **Launch and configure the Latte GUI first**

Launch Latte. Run setup.py and devInit.py respectively.

Ignore below error in log when devInit.py is run:

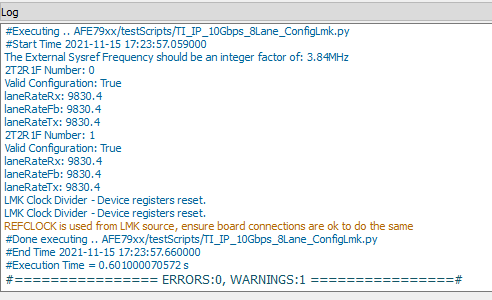
“Reset the FPGA and try again.”



Latte log

1. **Configure LMK04828 clocking device on AFE EVM**

Run TI\_IP\_12Gbps\_8Lane\_ConfigLmk.py.

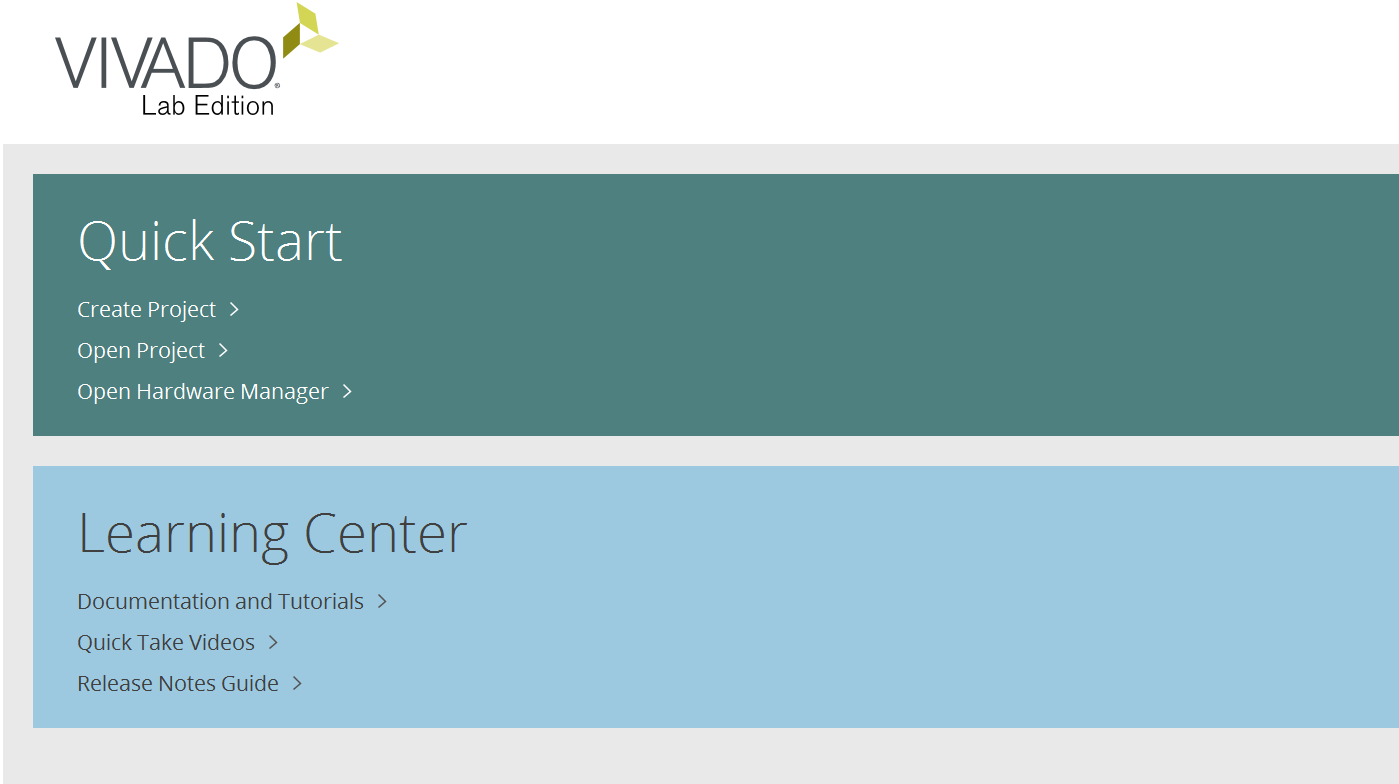


Latte Log

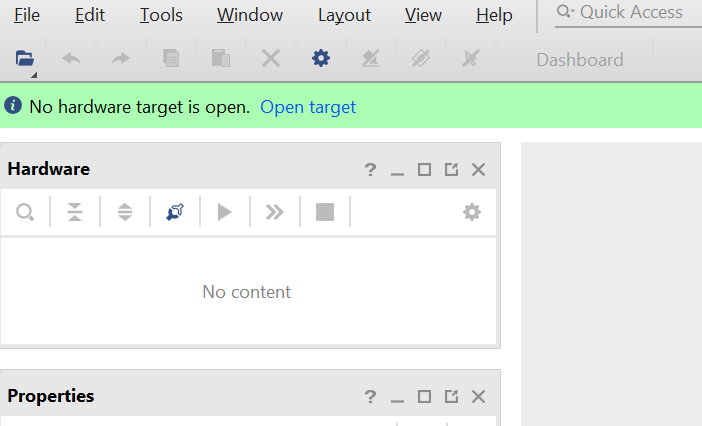
We will now switch to the Vivado setup.

1. **Launch and configure the FPGA through Vivado**

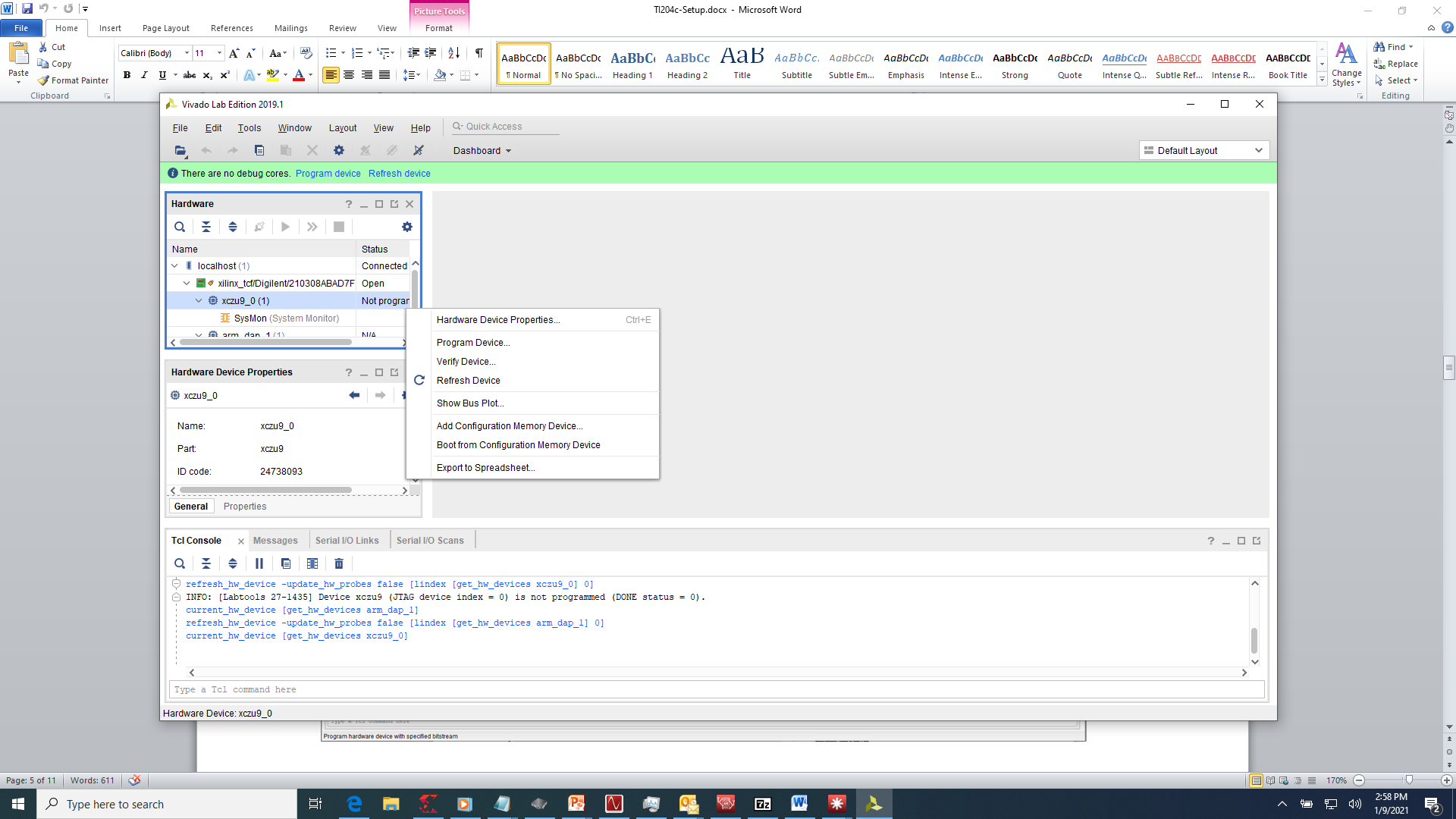
Launch Vivado 2019.1 and open Hardware Manager



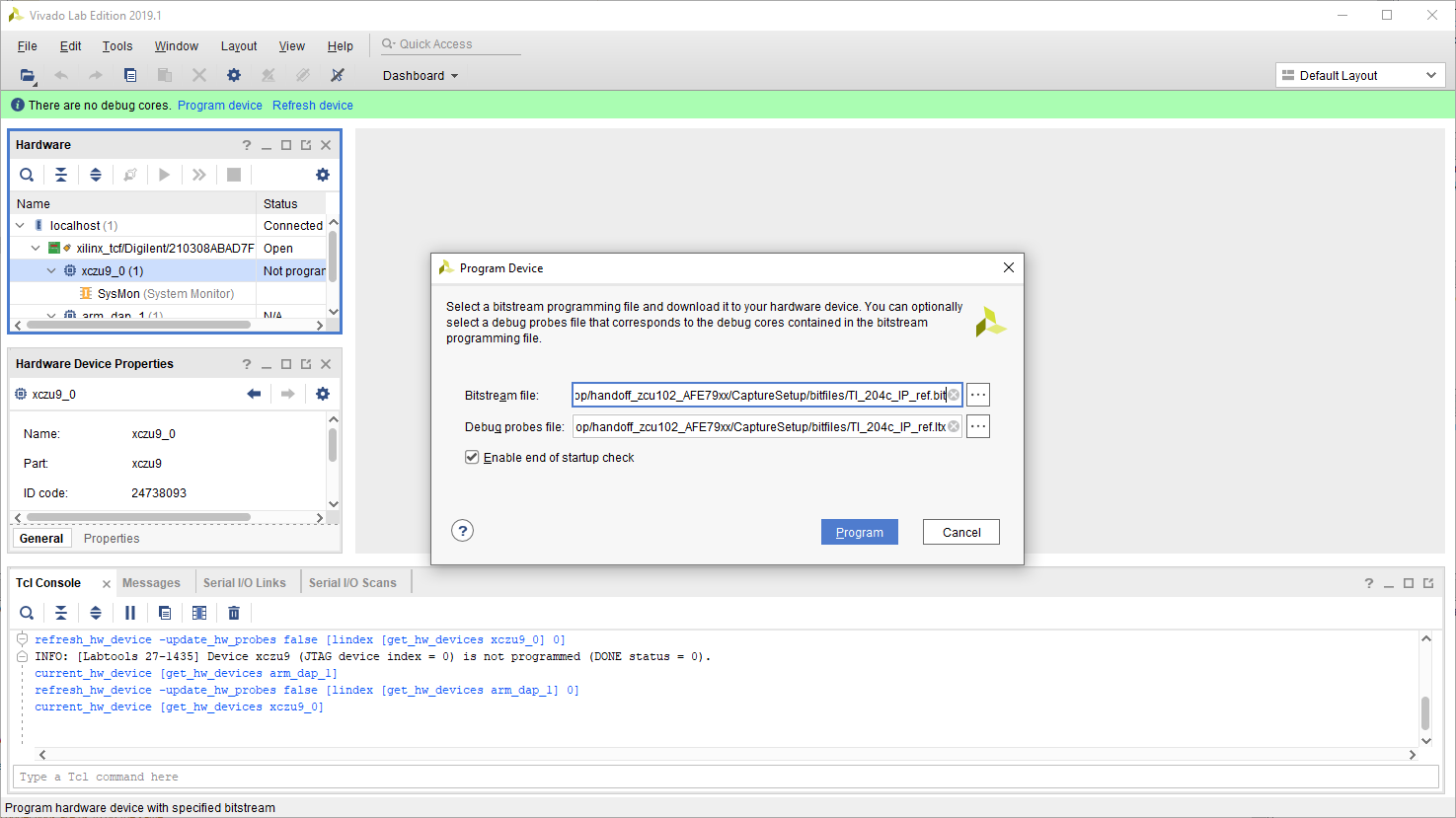
Select “Open Target”, and then select “Auto Connect”



Right Click on the xczu9\_0… device and select “Program Device”



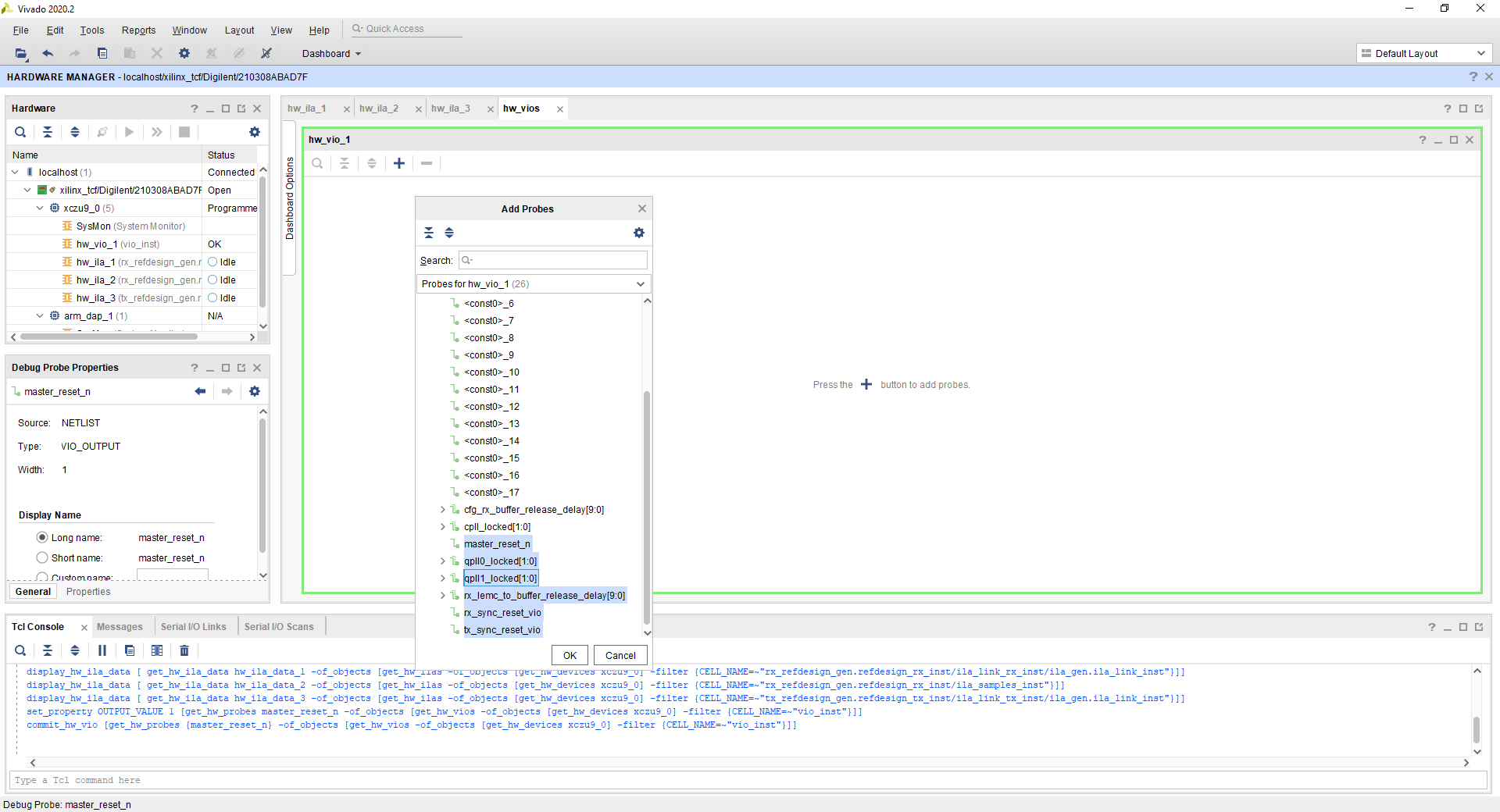
Navigate to the bitfiles sub-folder in the TI204c Capture Setup folder and select the bitfile



Click on Program to complete the FPGA configuration with the bitfile

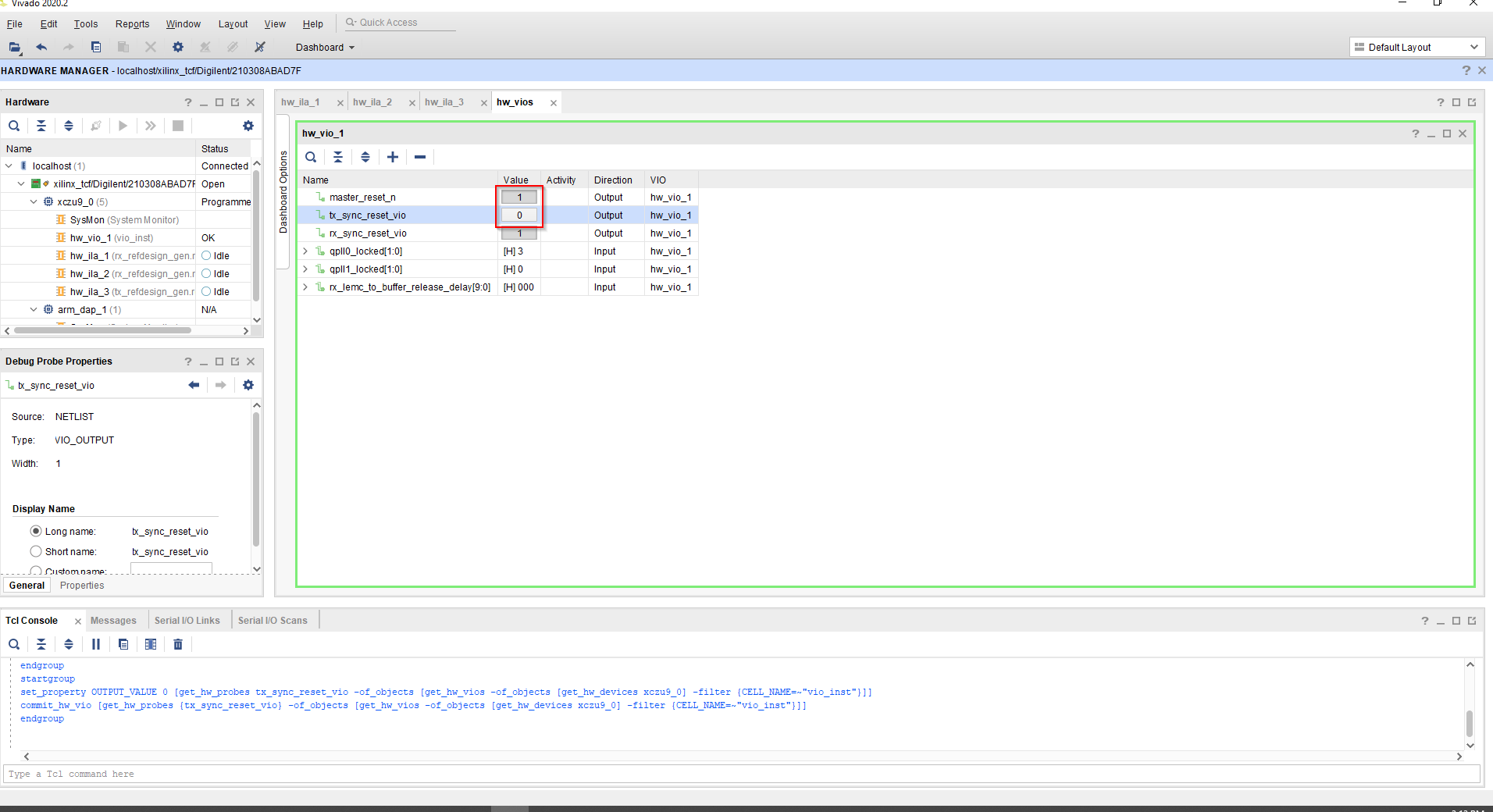
In the Vivado, open the hw\_vios tab and add probes for the following parameters:

* Master\_reset\_n
* Tx\_sync\_reset\_vio
* Rx\_sync\_reset\_vio
* Qpll0\_locked[1:0]
* Qpll1\_locked[1:0]
* Rx\_lemc\_to\_buffer\_release\_delay[9:0]



In order to set up the FPGA to send Tx data out on the JESD lanes we first need to follow these steps:

1. Take the master reset out of reset (Set master\_reset\_n to 1)
   1. When the master reset is 1 the qpll should lock, indicated by a value of 3.
2. Take the Tx sync out of reset (Set tx\_sync\_reset\_vio to 0)

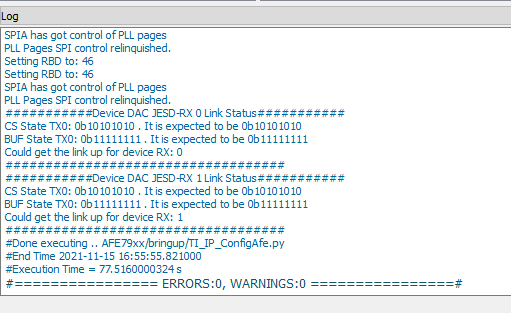


The FPGA is now set up to send Tx data out on JESD lanes.

1. **Configure AFE through Latte GUI**

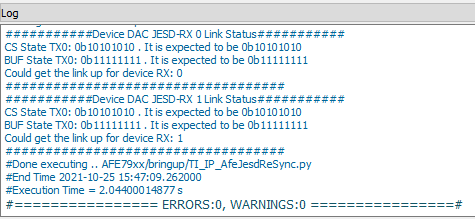
Run TI\_IP\_ConfigAfe.py in latte.

This takes about 100 seconds to run. Latte log confirms status of DAC JESD link.



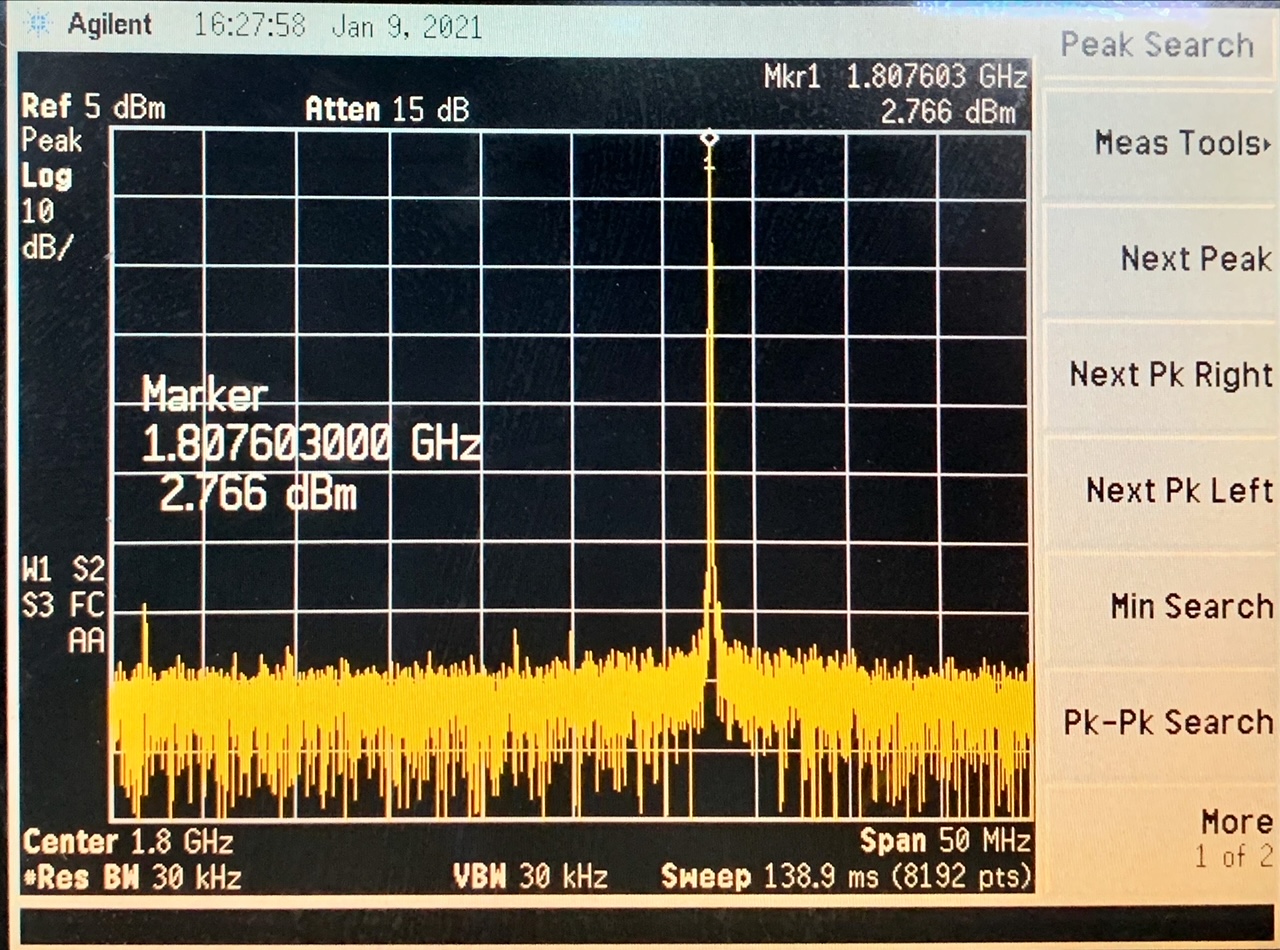
Latte log

If the DAC JESD link is not established at this point, run script *TI\_IP\_AfeJesdReSync.py* in latte.



Latte Log

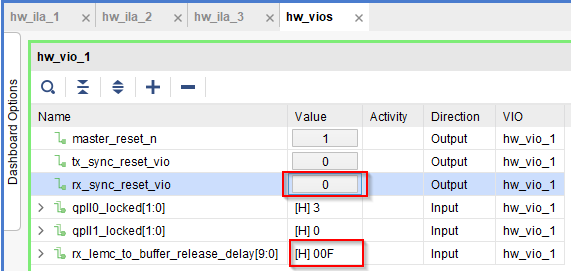
A 64 point complex single tone is sent as TX data from FPGA. So, TX should output a single tone at NCO frequency + (491.52/64) = (NCO + 7.68) MHz



TX single tone output (NCO set to 1800MHz)

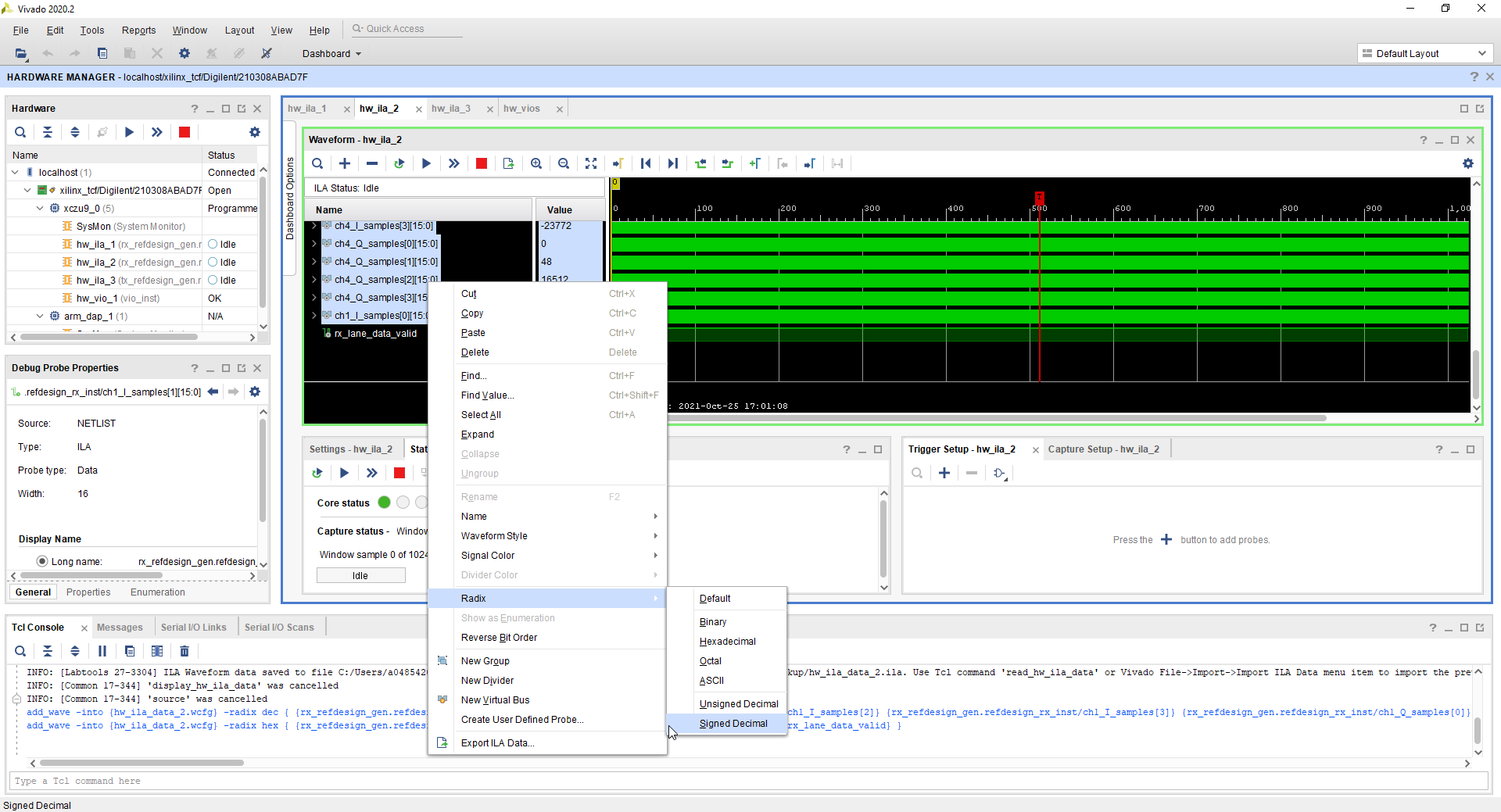
1. **Release Rx reset and capture data through Vivado**

In the Vivado hw\_vios tab set rx\_sync\_reset\_vio to 0. A successful Rx link will be indicated by the ‘rx\_lemc\_to\_buffer\_release\_delay’ parameter updating.



Rx Sync Reset Released

Once the Rx link is established you can now work on capturing data. To do this you first need to open the hw\_ila\_2 debug core. Select all samples and change their Radix to Signed Decimal



To continuously capture the Rx data, follow the steps below:

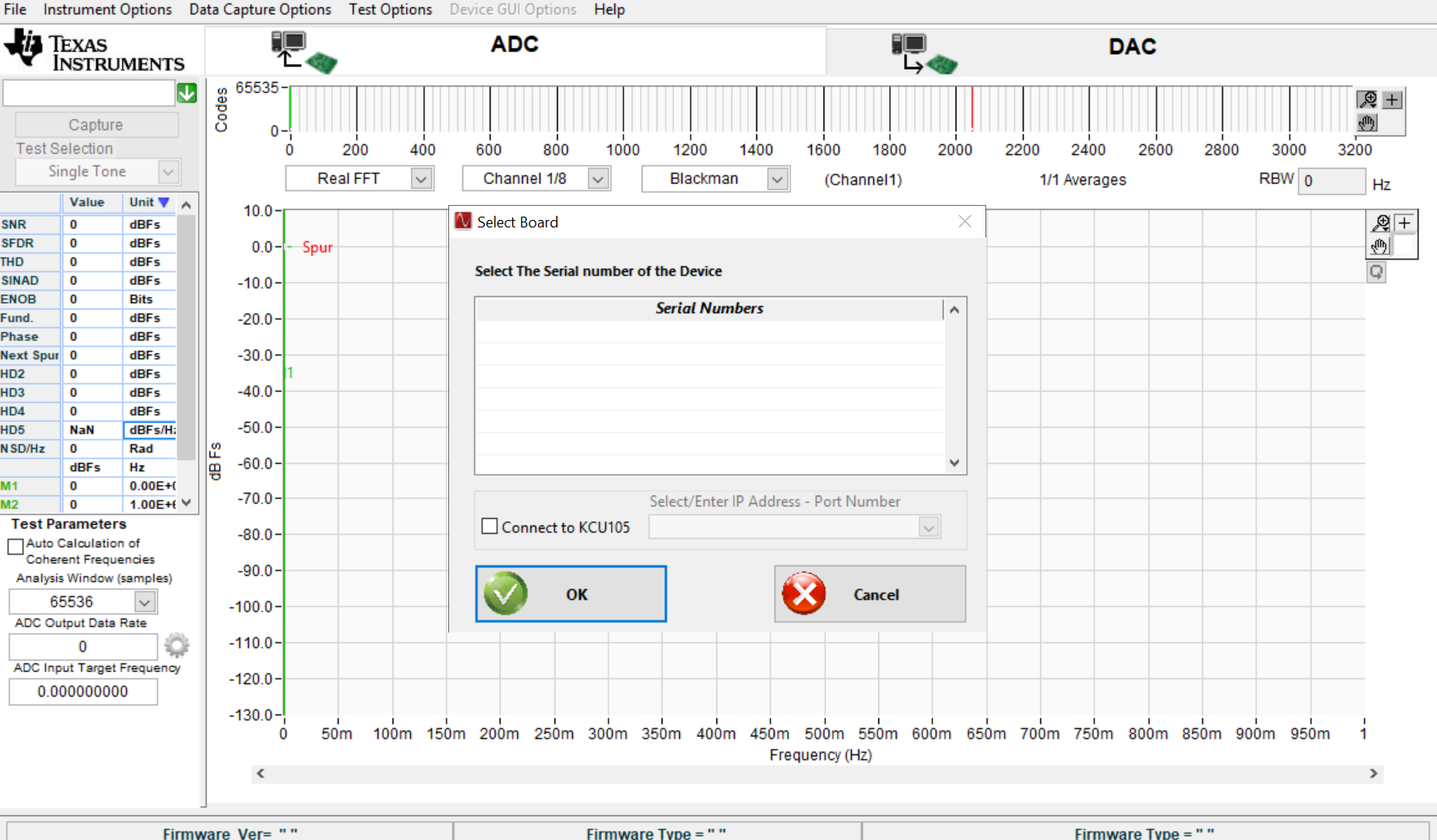
In the Vivado TCL console, execute the following:

cd <path to reference design folder> /Documentation

source capture.tcl

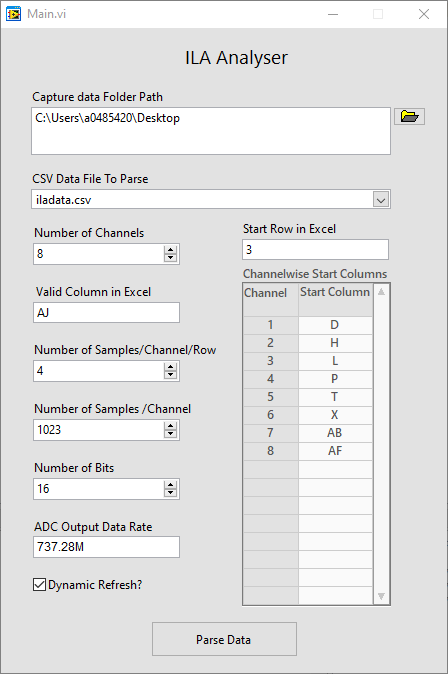
1. **Launch HSDC Pro and the Dynamic Refresh Control GUI for displaying and Rx analyzing data**

Open the HSDC Pro GUI and click ‘Okay’ on the box that pops up. We will be using HSDC Pro primarily as a display tool. It isn’t collecting data directly from the board, so it is fine if there is no serial number displayed.

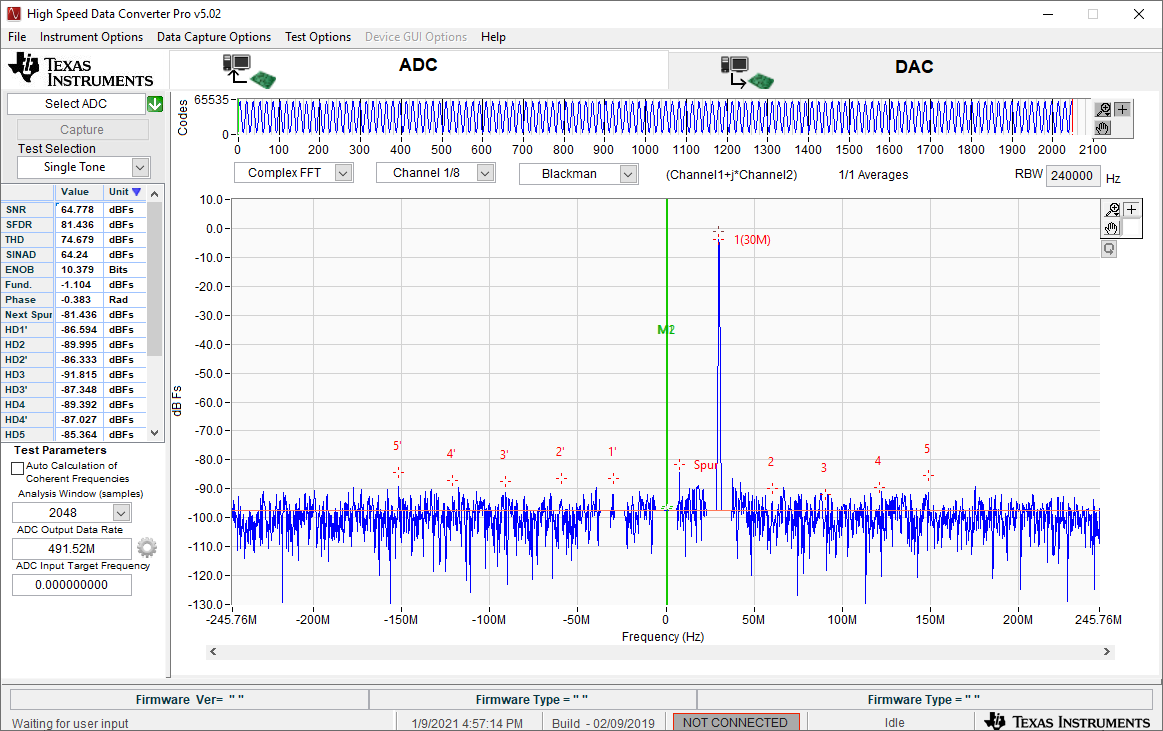


Open a Windows file browser and carry out the following

* Navigate to < path to TI204c\_capture\_setup folder> \ ILA Analyser Version 1.3
* Launch “ILA Analyser.exe”
* Set the Capture data Folder Path to the desktop directory as shown.



Click on “Parse Data” and you should now be viewing the data captured for Channel A. The utility is set up to update the waveform/FFT each time Vivado updates the CSV file.



Output FFT: NCO set to 1800MHz, input frequency: 1830MHz, Output tone at 30MHz in complex FFT