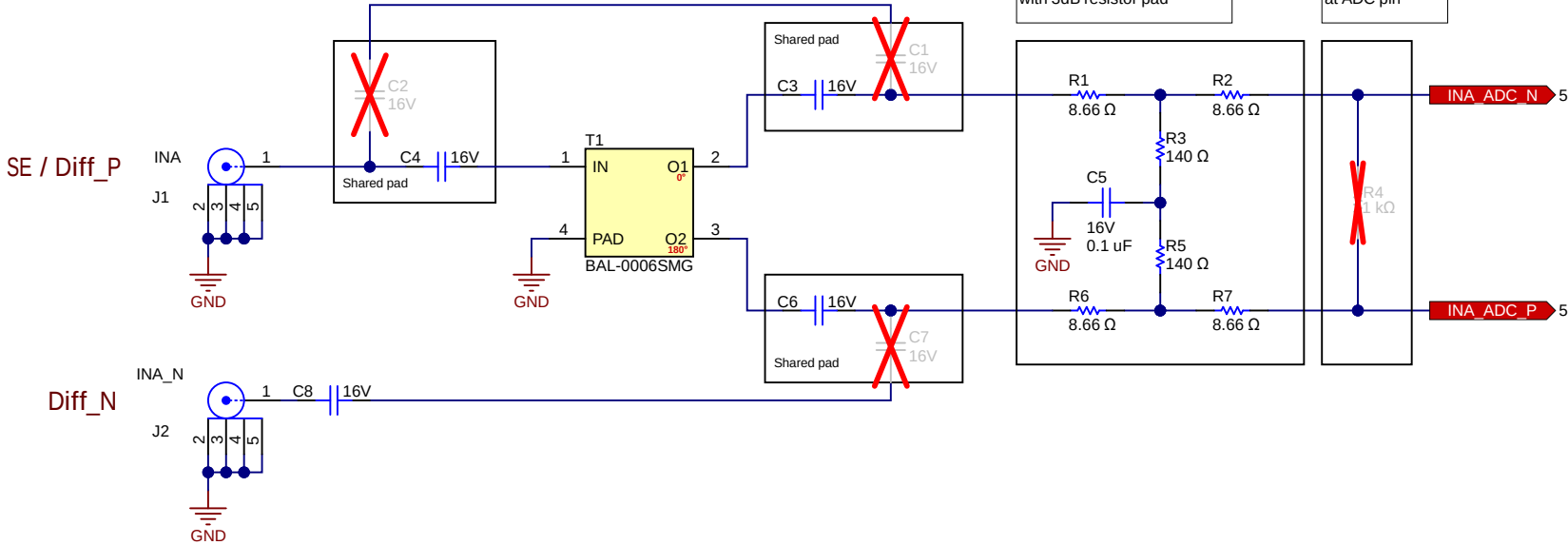


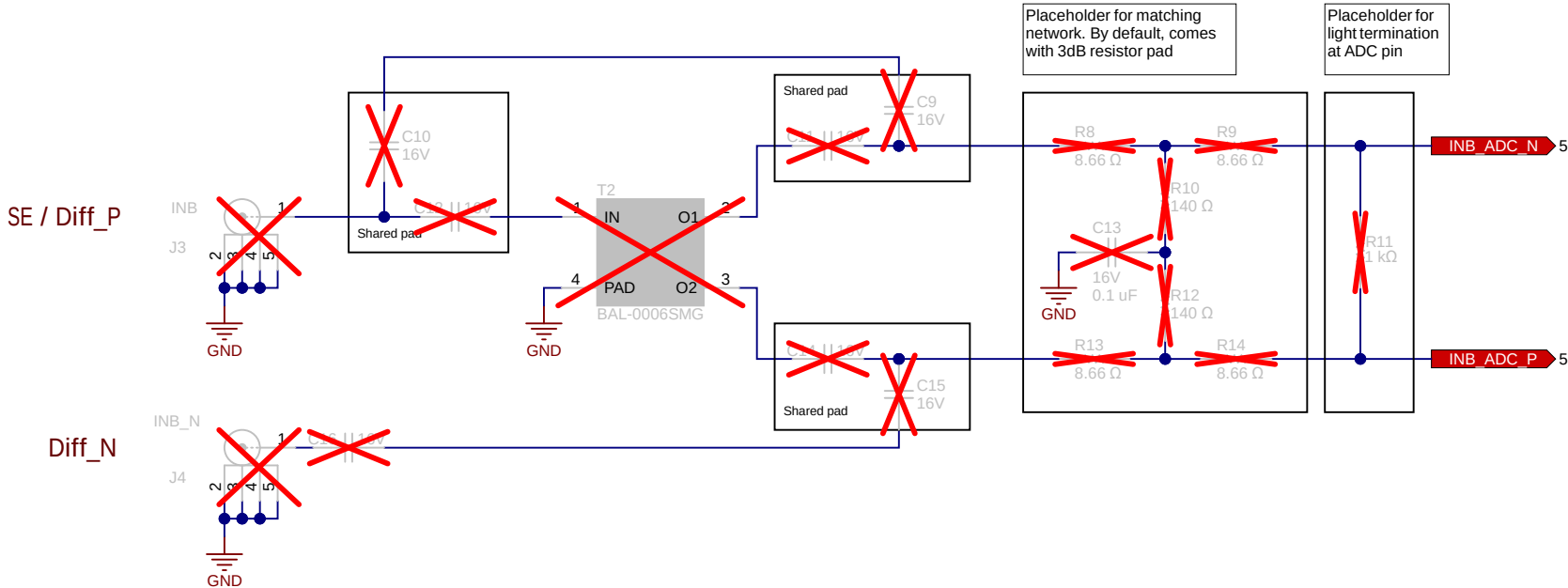


ADC EVM RF Input

Channel A

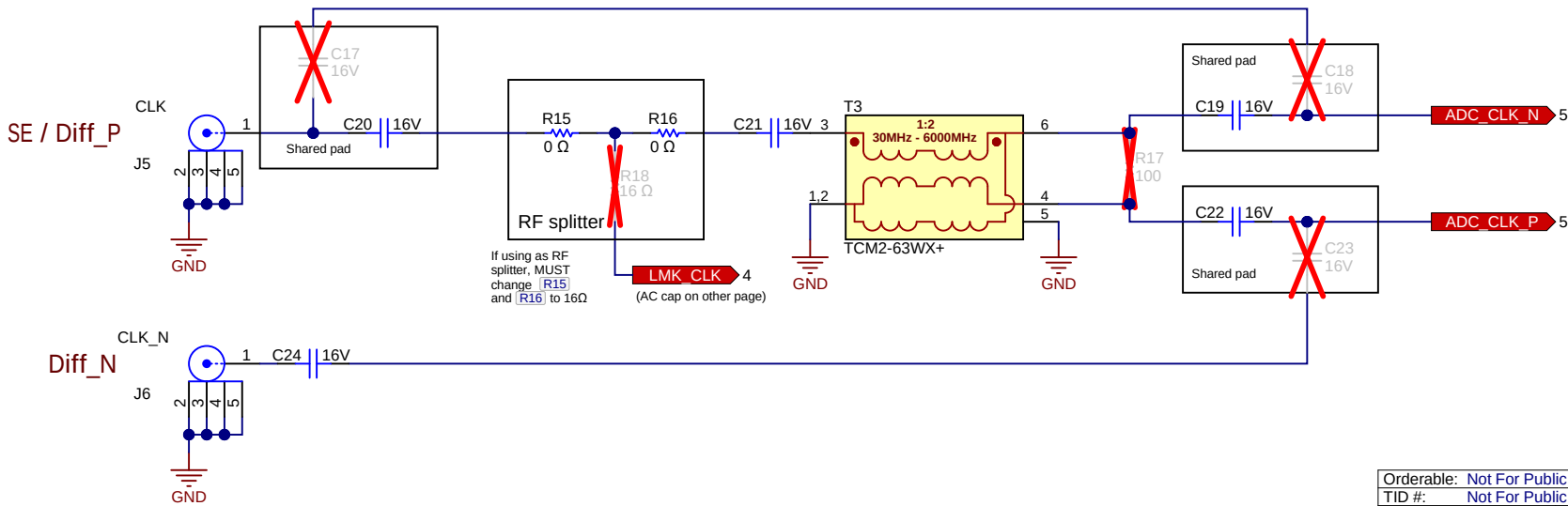


Channel B



Clock input

Differential by default
Note: LMK requires reference clock on input [J12](#)

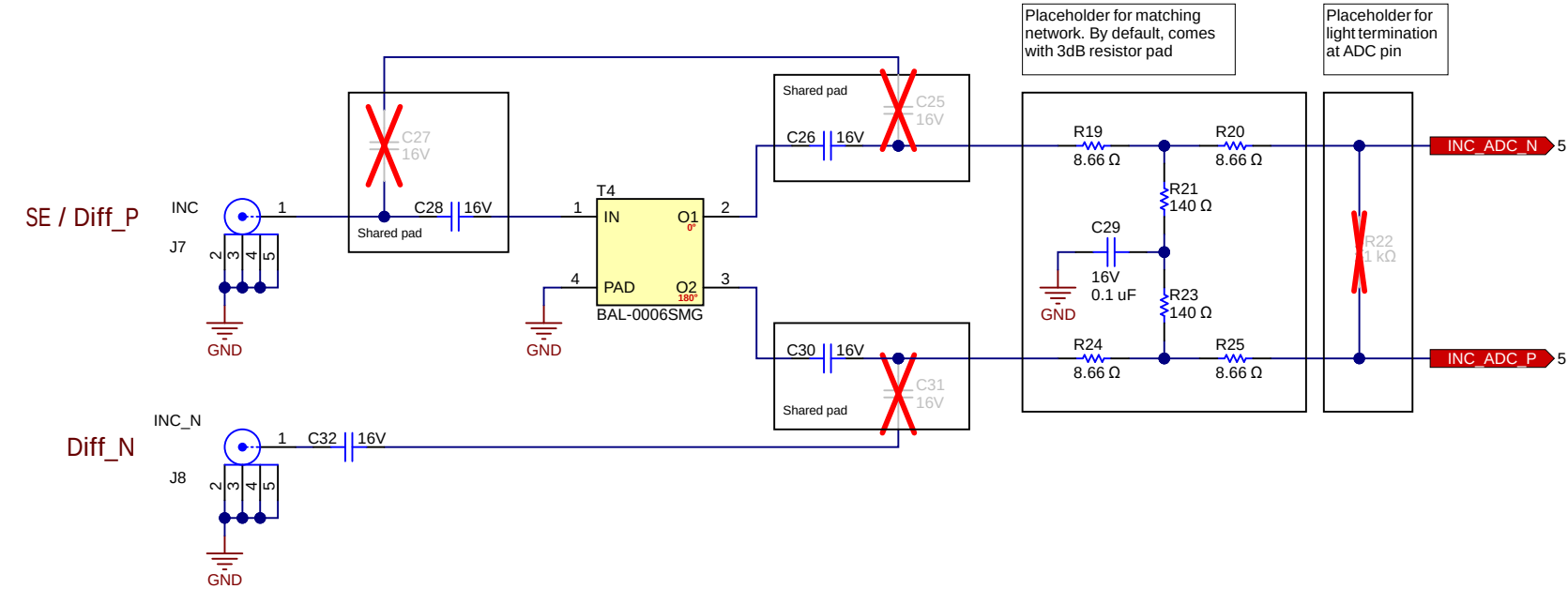


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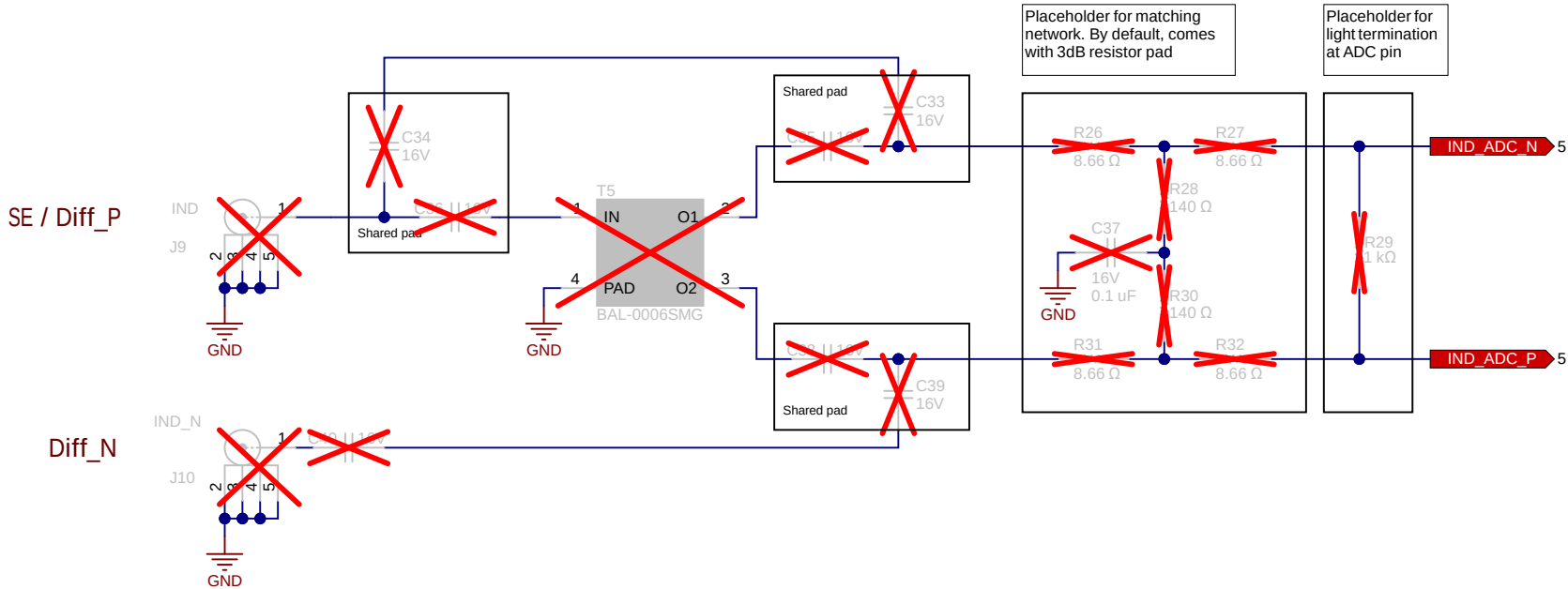
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SVN Rev:	cfec0883921a2ab84ee9a1a5050b24a5b45223	File:	ADC34RF7x_ADC_Input_AB_RevA.SchDoc	Sheet:	2 of 20
Drawn By:	CW	Size:	B		
Engineer:	CW	Contact:	http://www.ti.com/support		

ADC EVM RF Input

Channel C



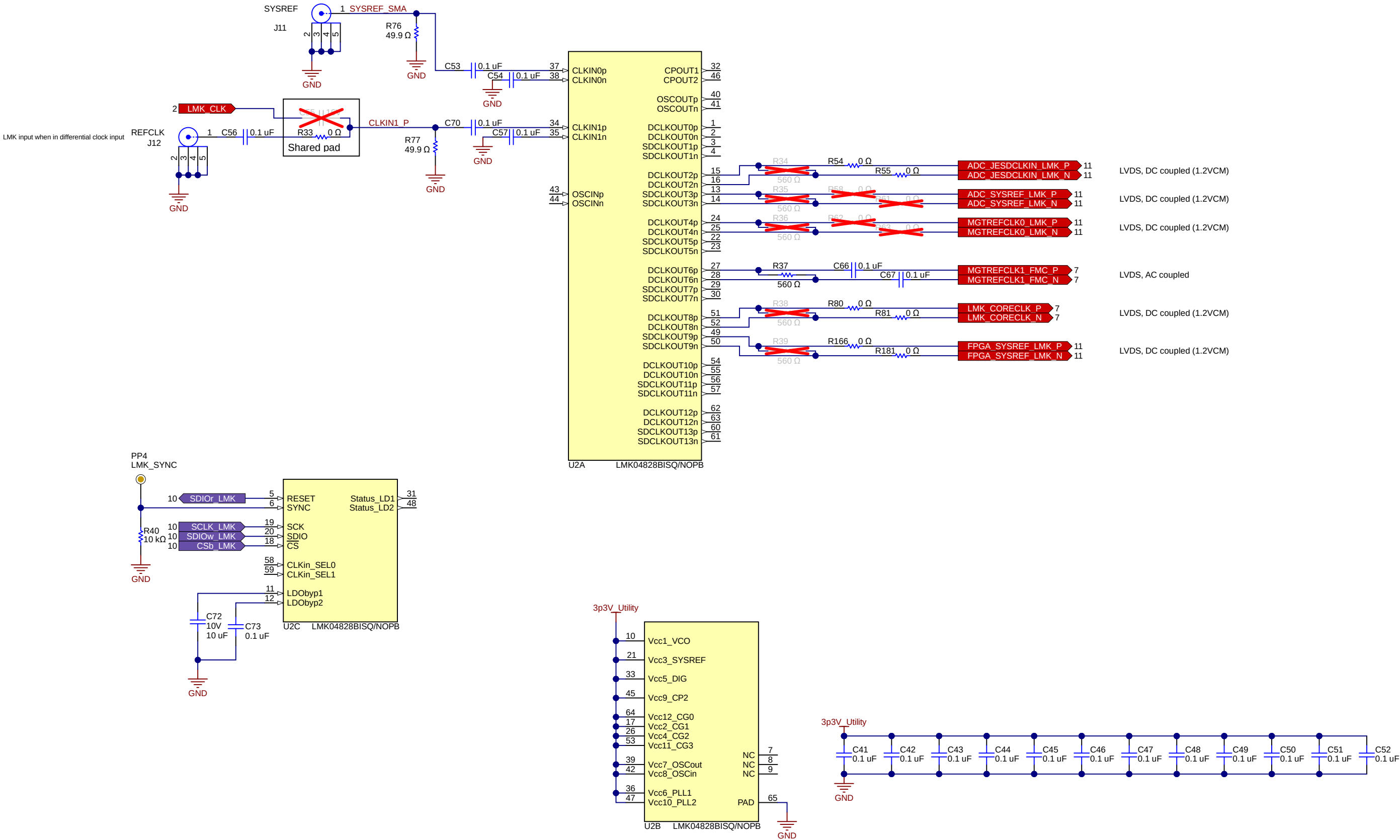
Channel D



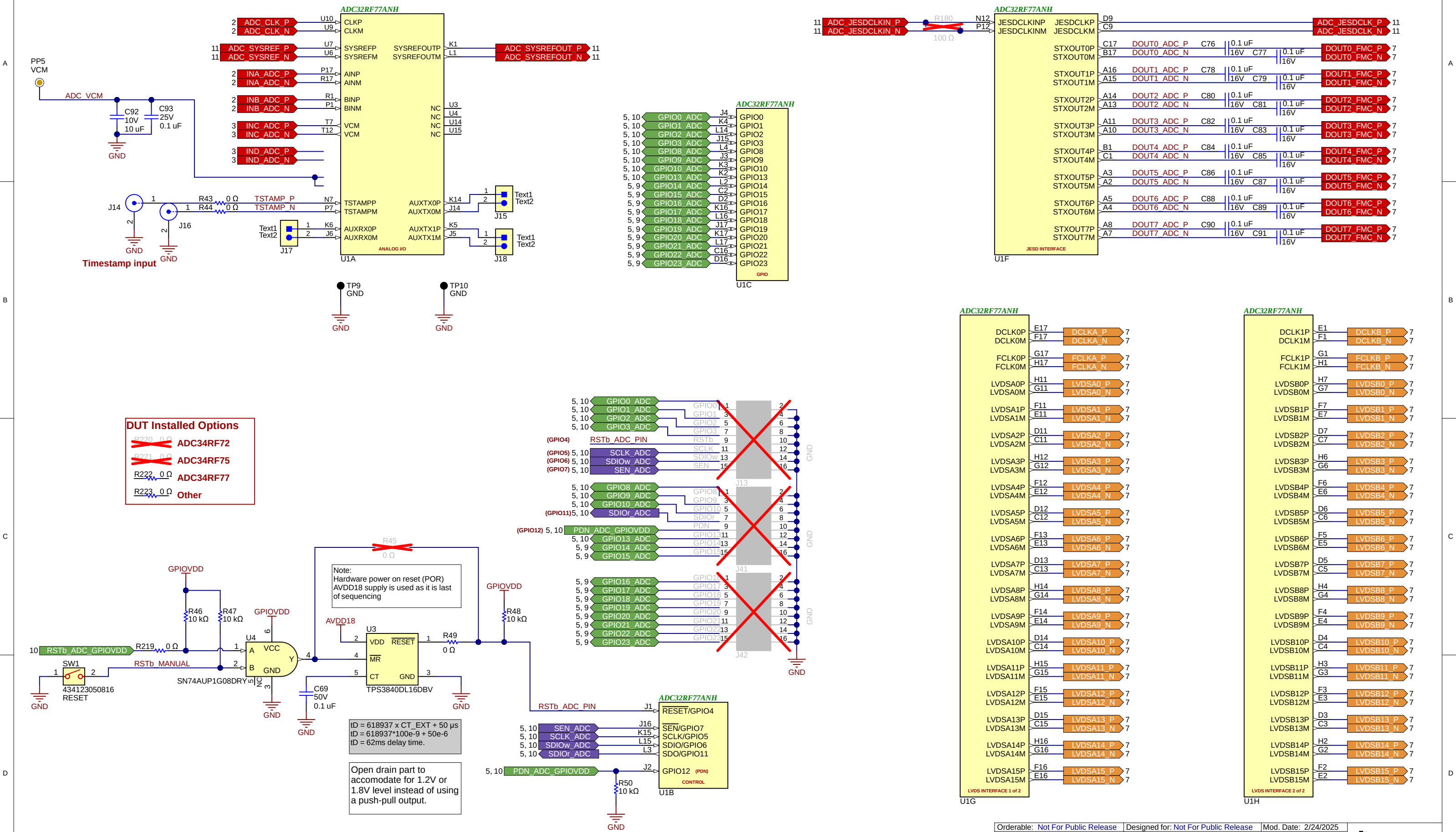
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Number:	-	Rev:	A	Sheet Title:	ADC EVM RF Input
SVN Rev:	3549342212367fc0980ad10327091e956605c003	ADC32RF77		Sheet:	3 of 20
Drawn By:		File:	ADC34RF7x_ADC Input_CD_RevA.SchDoc	Size:	B
Engineer:	CW	Contact:	http://www.ti.com/support		

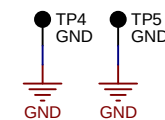
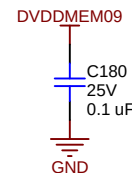
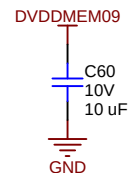
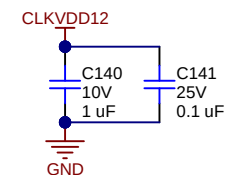
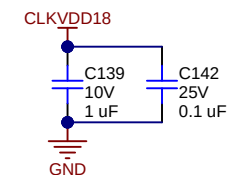
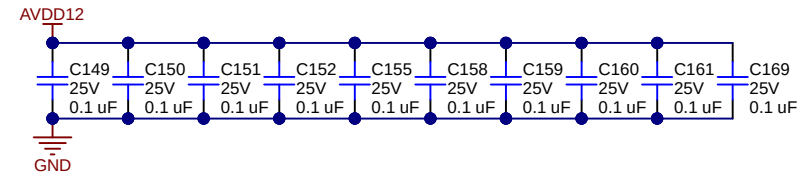
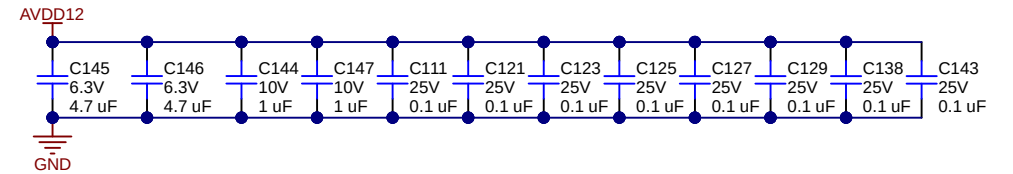
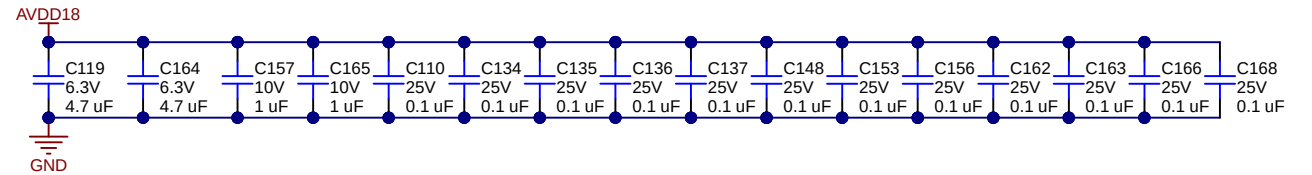
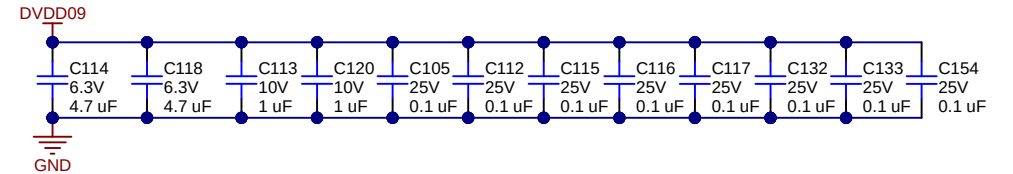
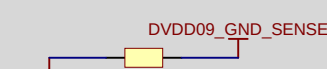
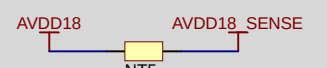
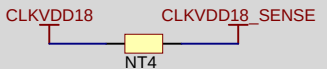
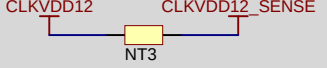
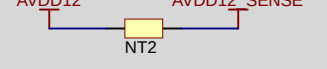
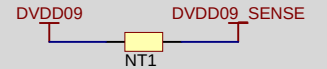
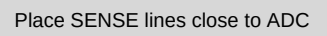
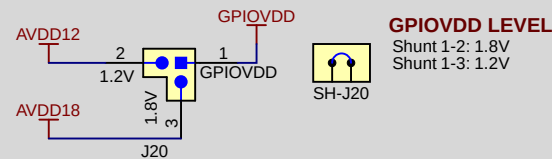
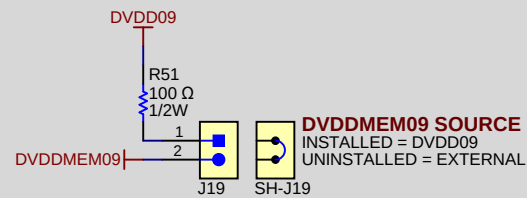
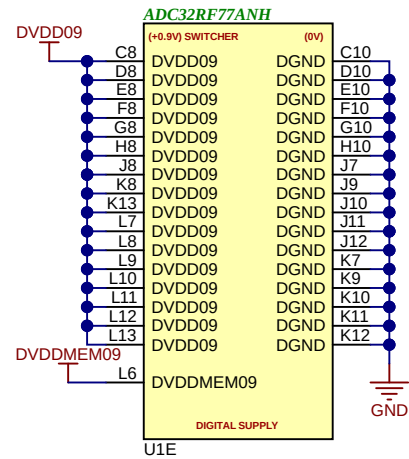
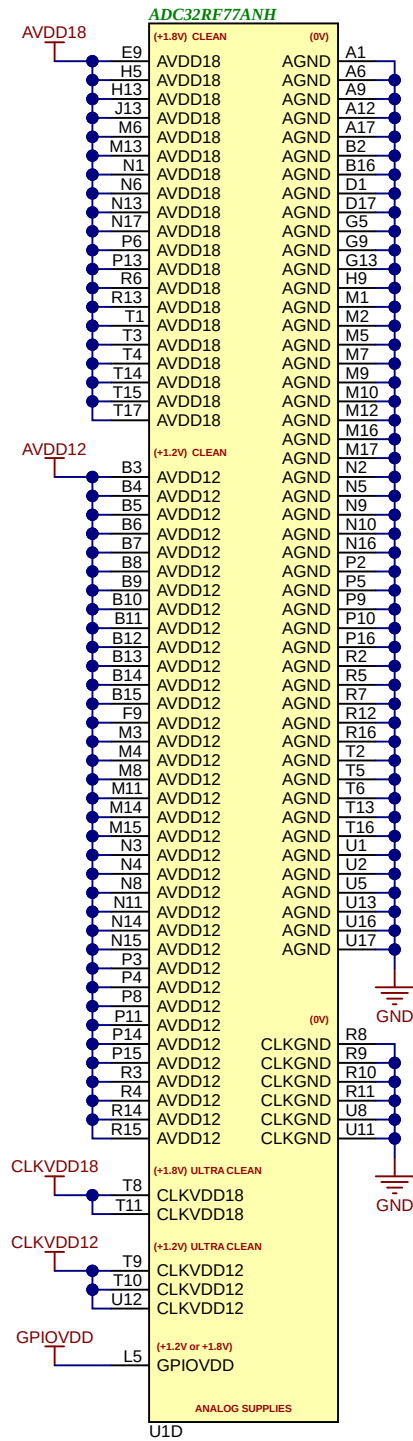
LMK04828 FPGA Clocks and SYSREF



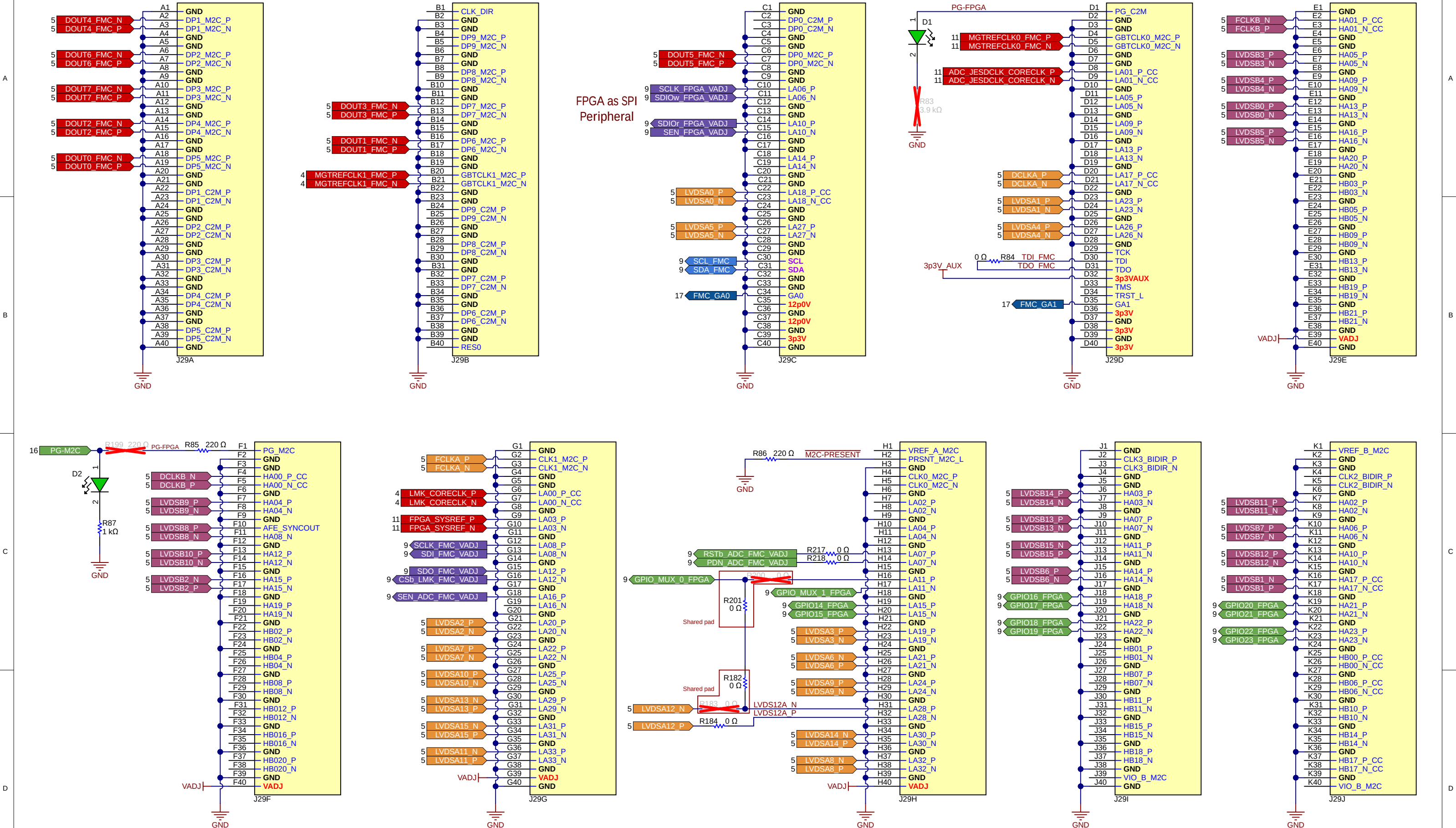
ADC Input, SERDES and Digital Pins



ADC EVM Power

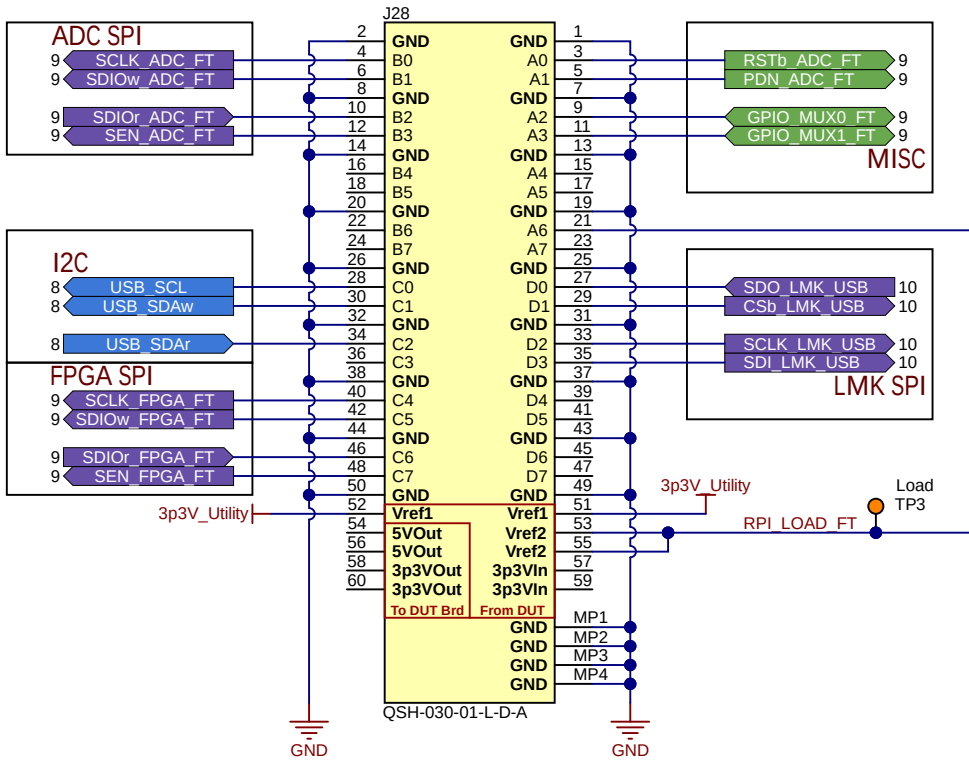


FMC Connector

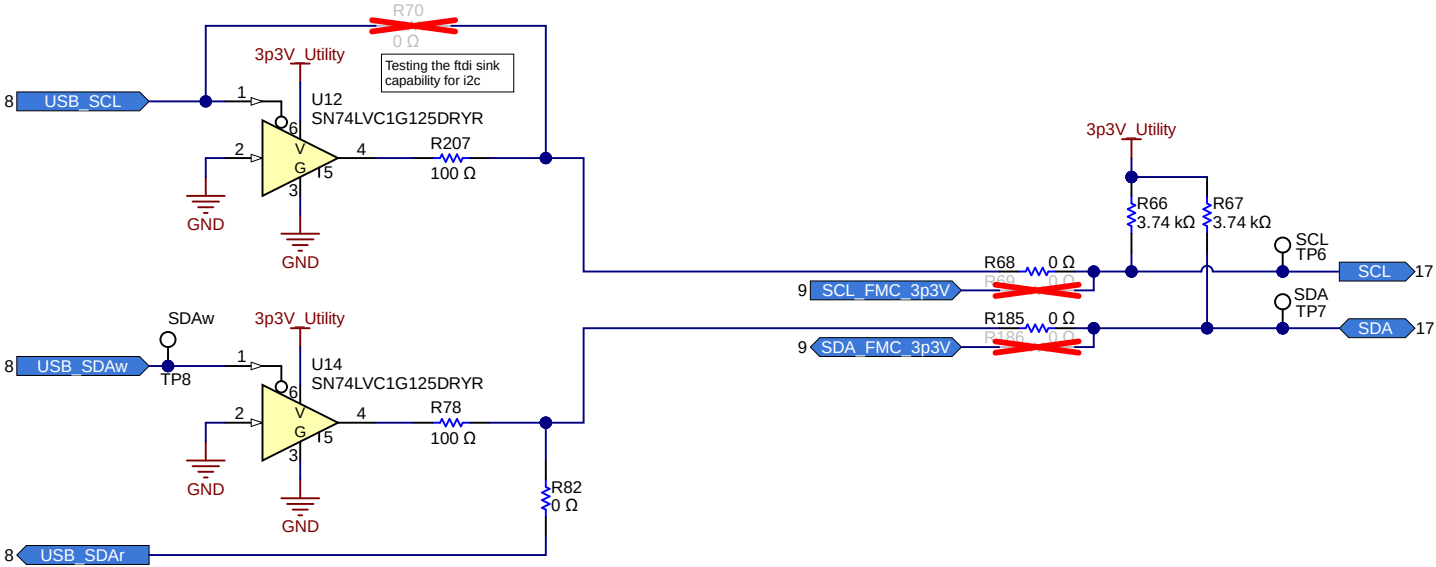


Note: FTDI pinout matches TII dualsite board for ADC(site1) & LMK

*Note: All SDIO naming convention is from the perspective of the FTDI host controller.
SDIOw = Serial Data In (FTDI → ADC/LMK)
SDIOr = Serial Data Out (ADC/LMK → FTDI)

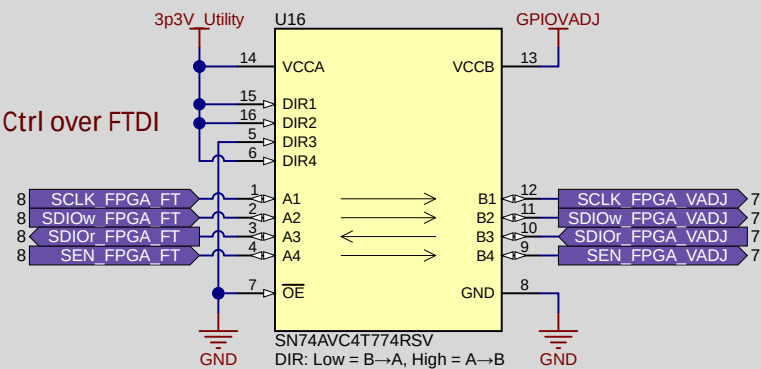


Vref1: Passes 3.3V to RPi autload board



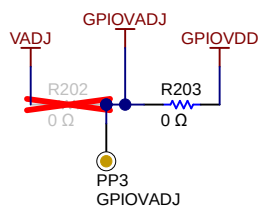
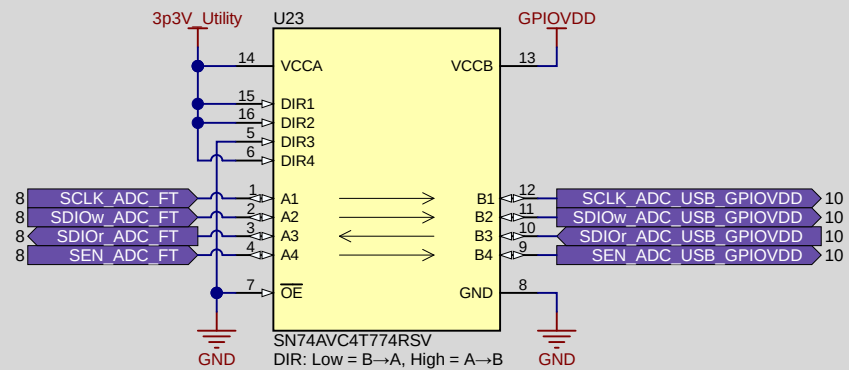
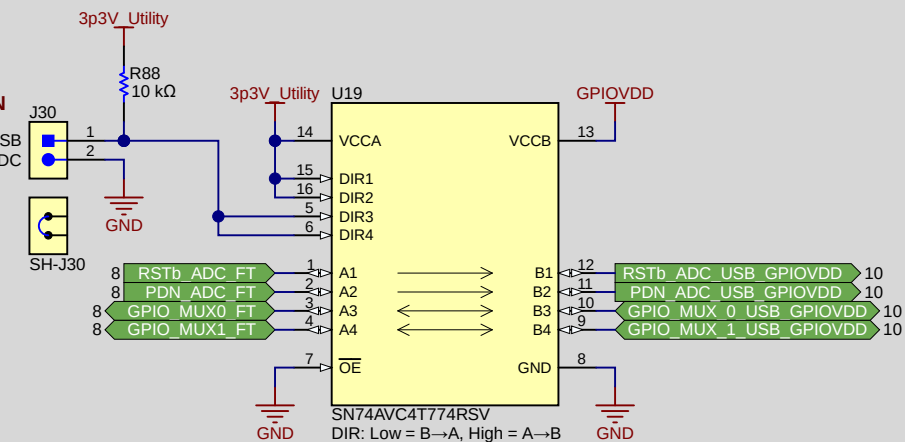
FTDI Level Shifting

FPGA Ctrl over FTDI

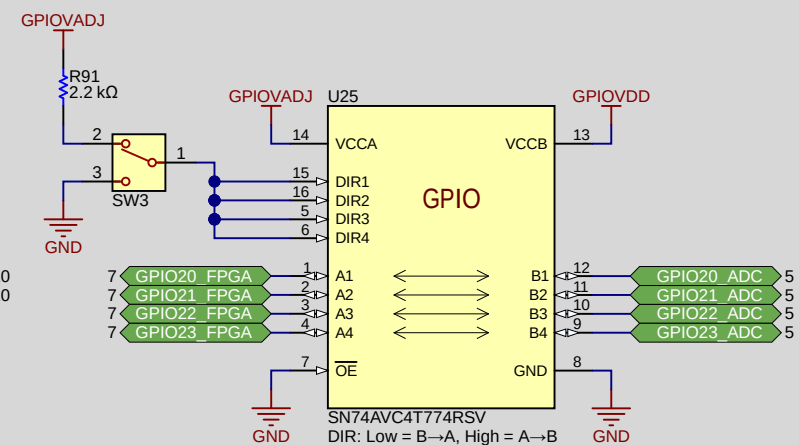
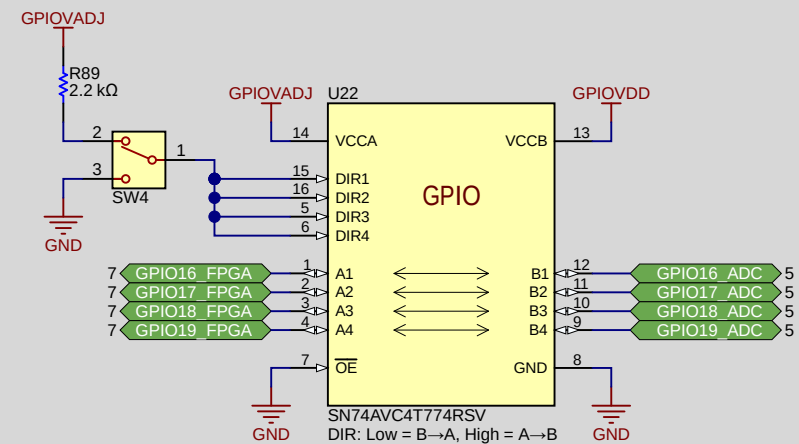
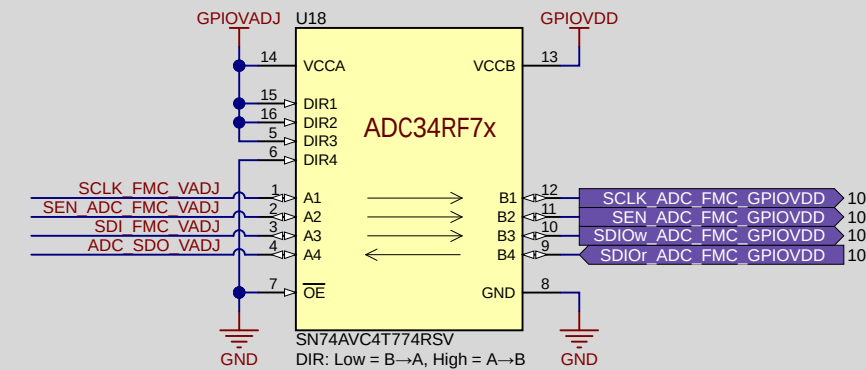
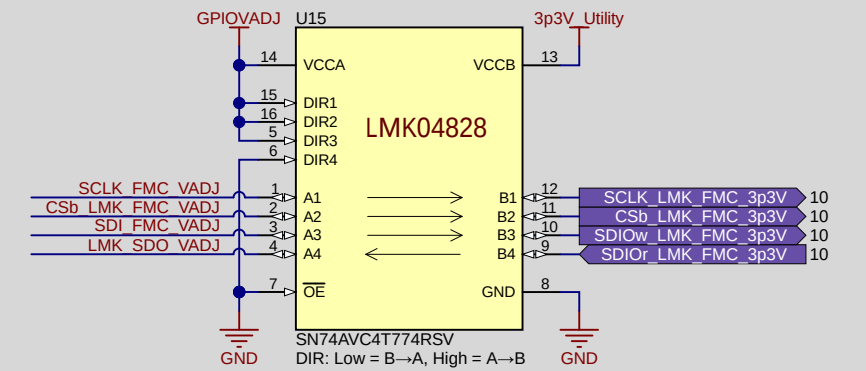
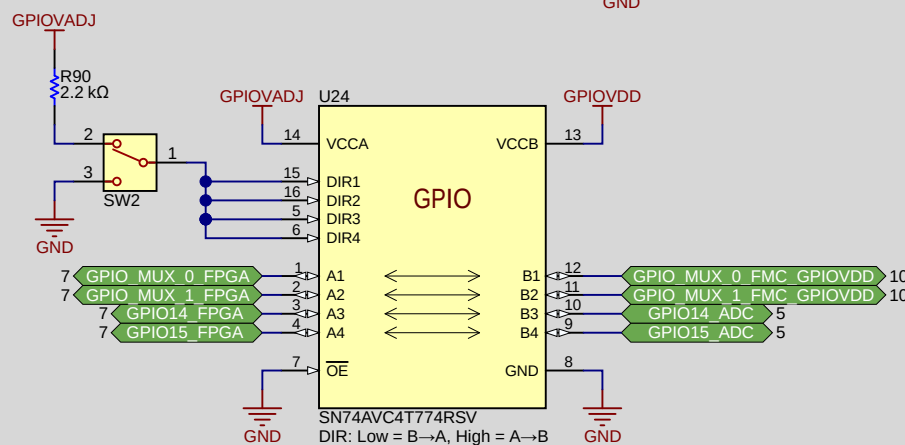
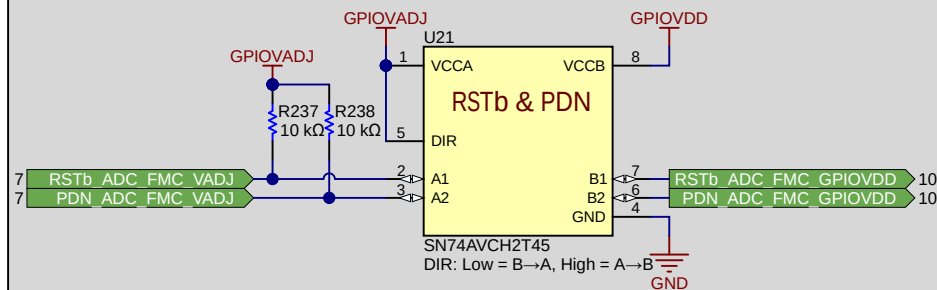
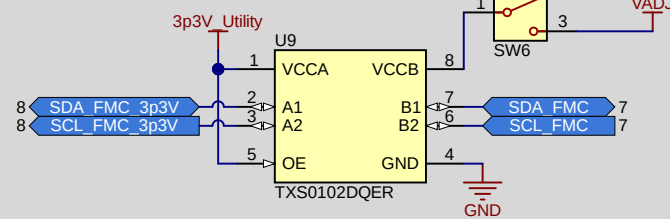
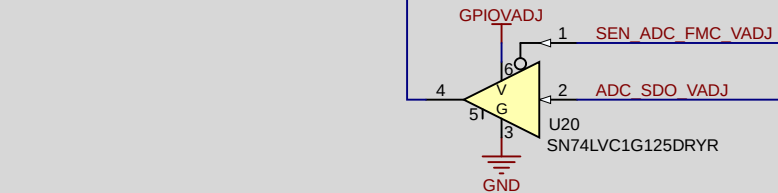
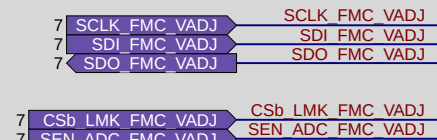


USB GPIO DIRECTION

INSTALLED = ADC to USB
UNINSTALLED = USB to ADC



FPGA Level Shifting



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Orderable: Not For Public Release	Designed for: Not For Public Release	Mod. Date: 3/13/2025
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Number: -	Rev: A	Sheet Title: Level Shifting
SVN Rev: cfc0883921a2ab84ee9a1a505022-ADC32RF77	Sheet: 9 of 20	
Drawn By: CW	File: ADC34RF7x_LVL_Shift_RevA.SchDoc	Size: B
Engineer: CW	Contact: http://www.ti.com/support	

MUXes

A

B

C

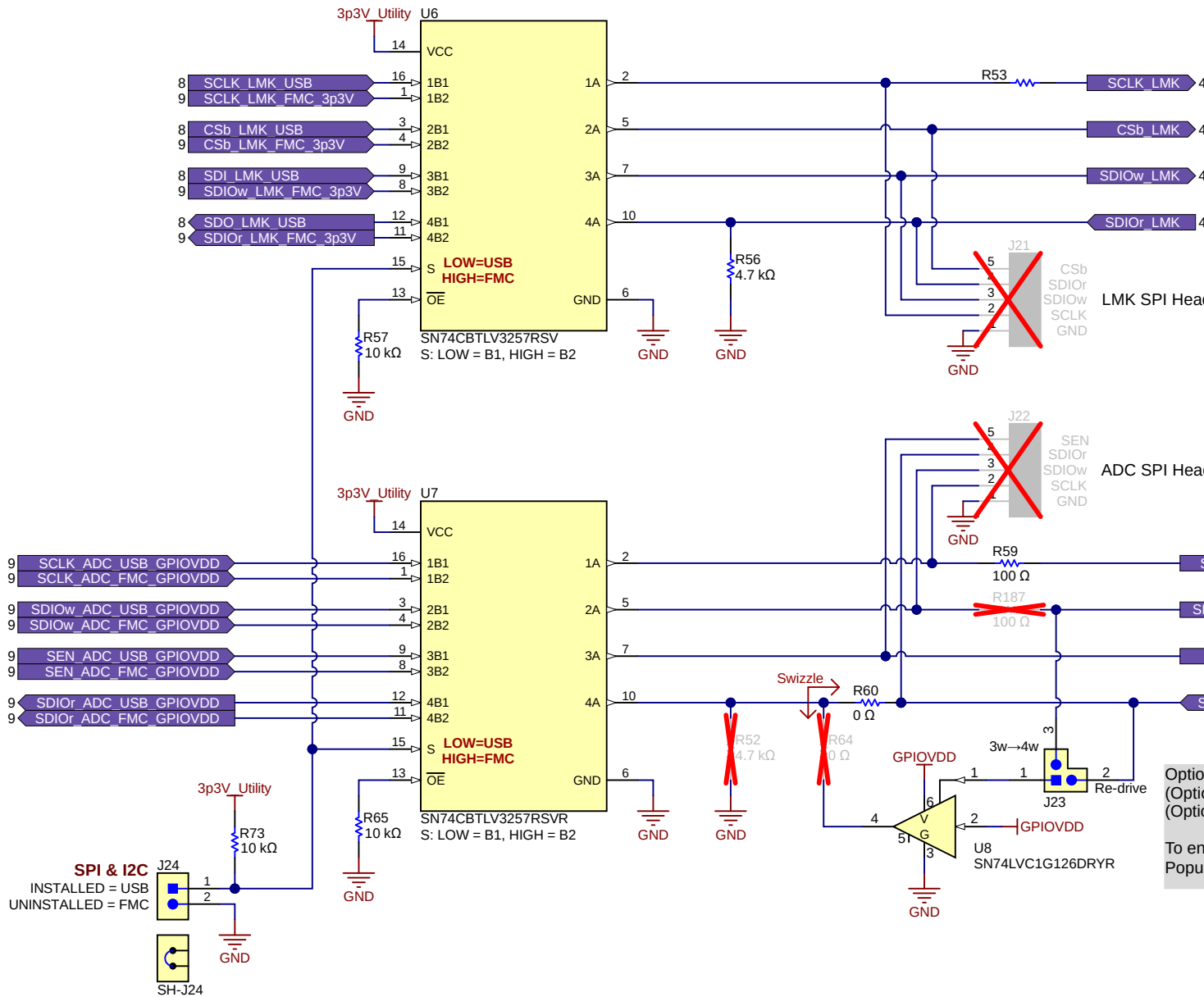
D

A

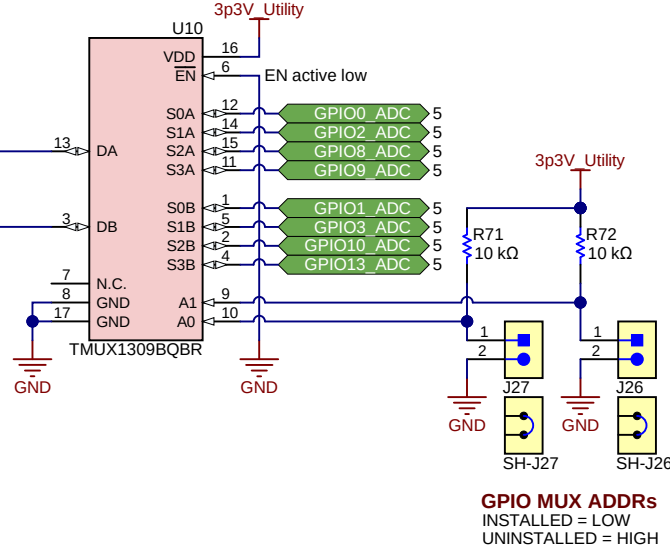
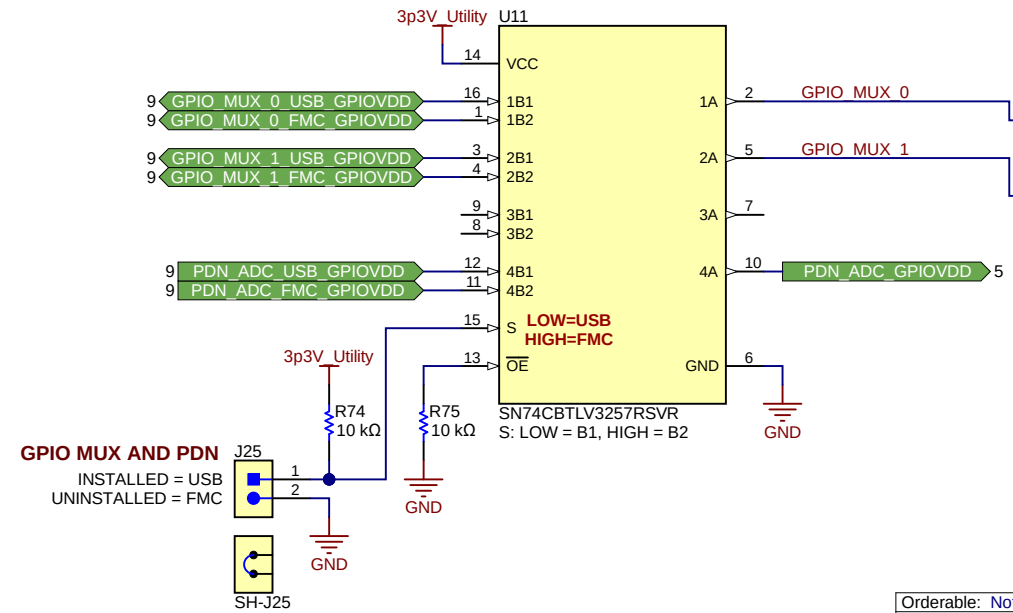
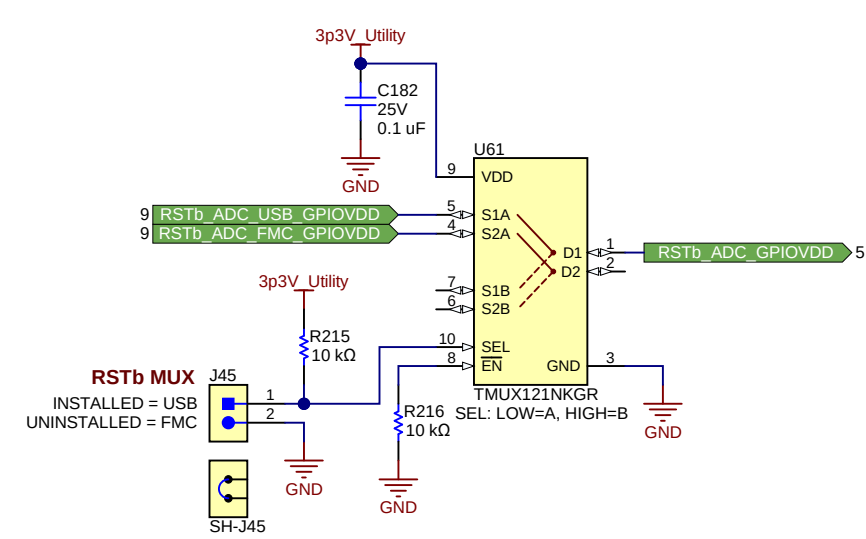
B

C

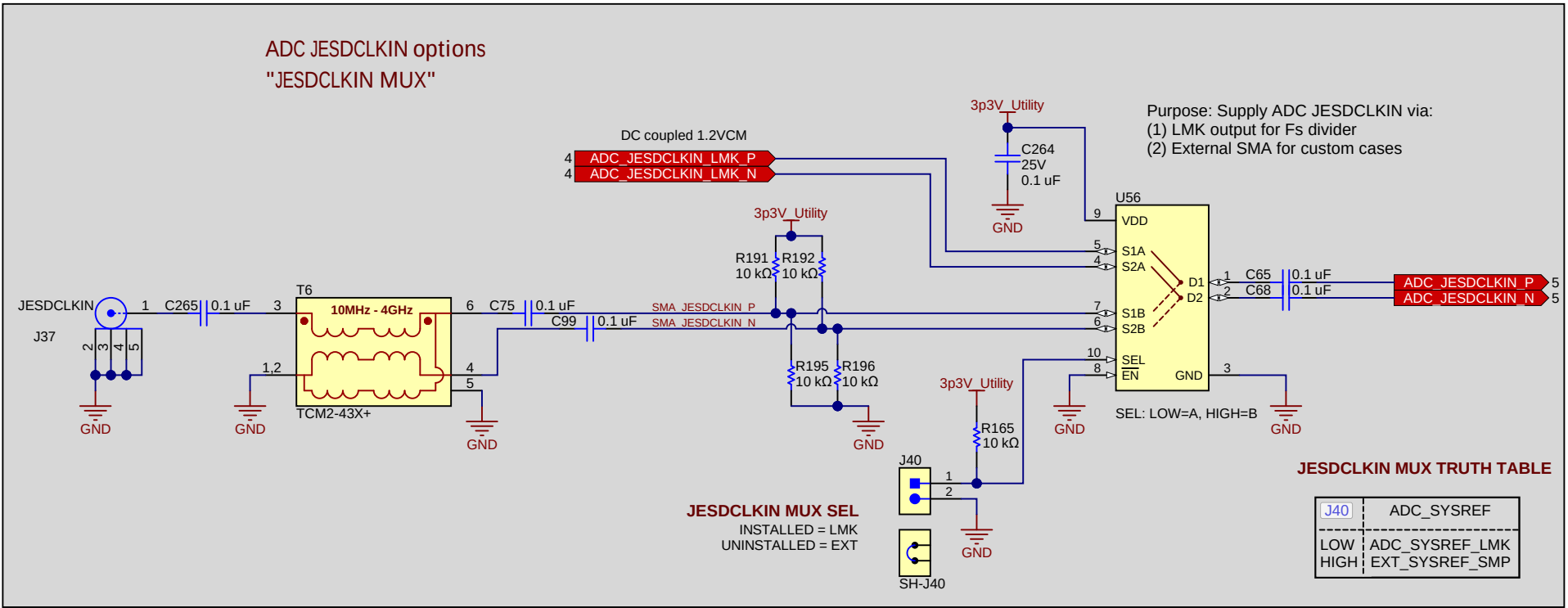
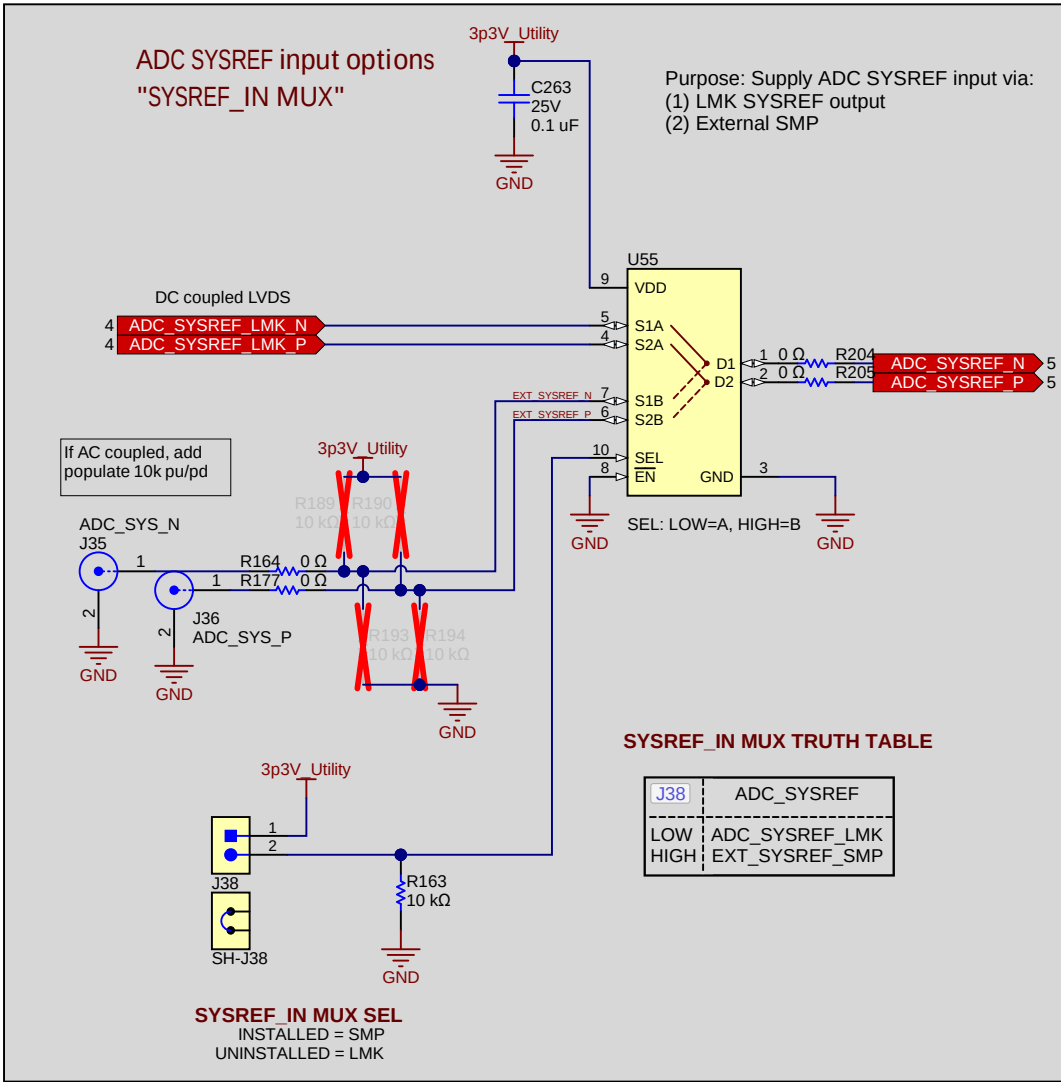
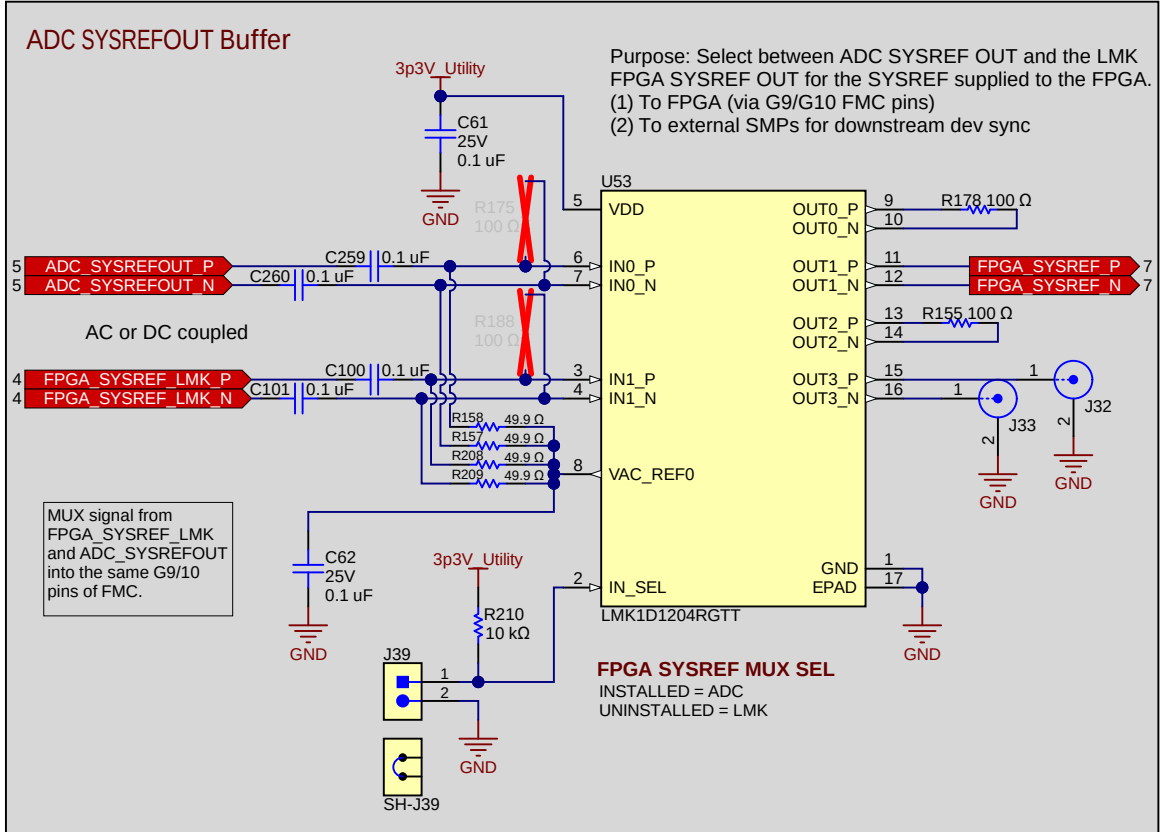
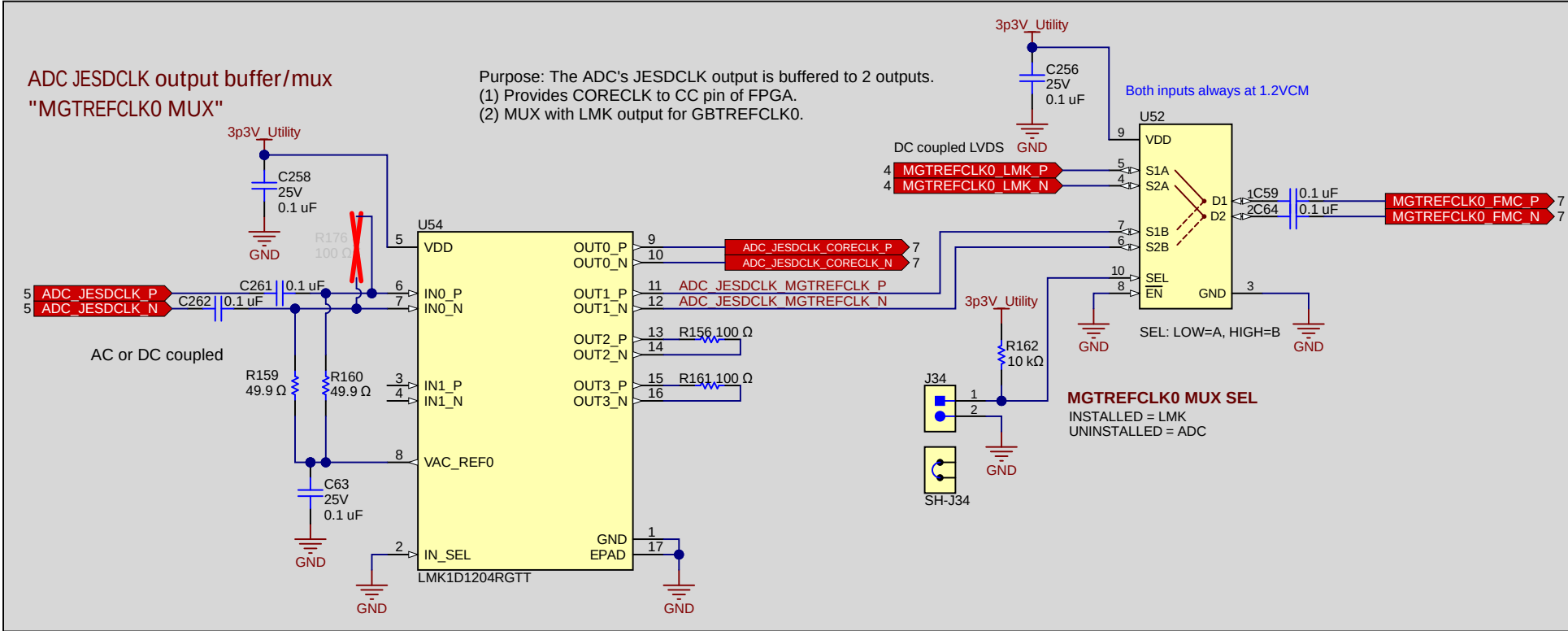
D



GPIO MUX TRUTH TABLE			
J27	J26	GPIO_MUX_0	GPIO_MUX_1
LOW	LOW	GPIO0_ADC	GPIO8_ADC
LOW	HIGH	GPIO1_ADC	GPIO9_ADC
HIGH	LOW	GPIO2_ADC	GPIO10_ADC
HIGH	HIGH	GPIO3_ADC	GPIO13_ADC



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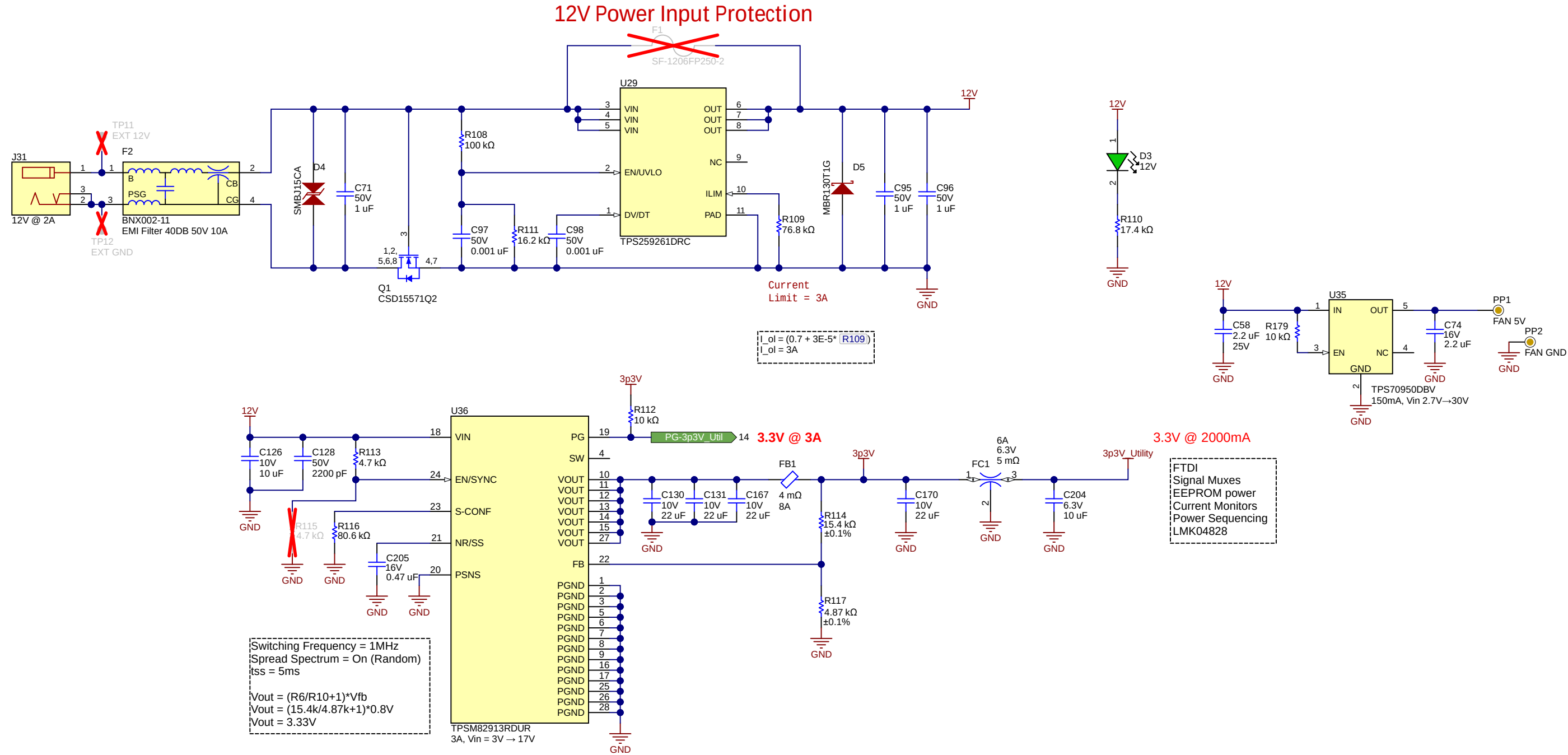


POWER UP SEQUENCE

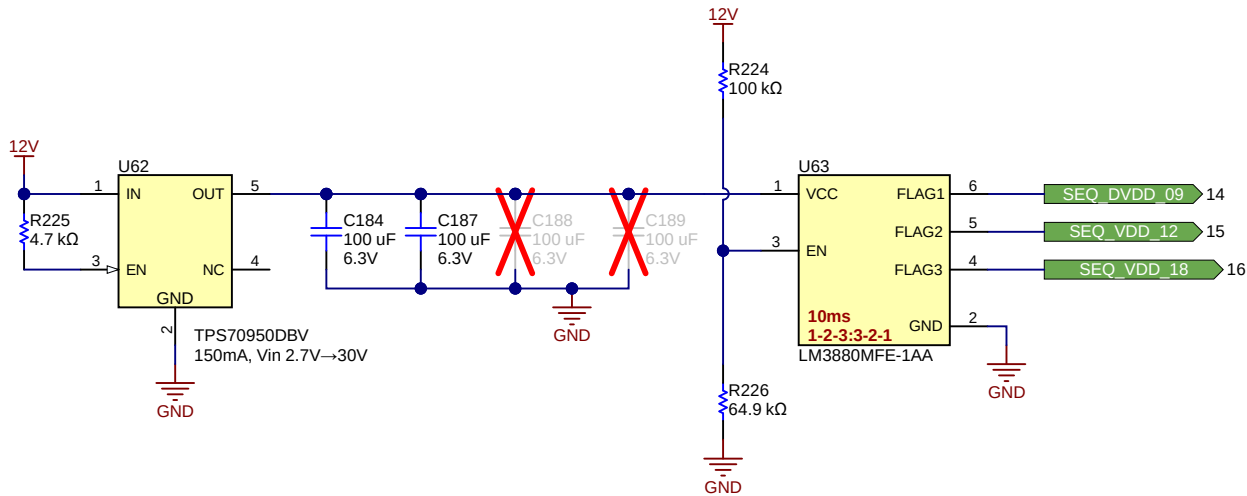
1. DVDD (0.9V)

2. AVDD12 (1.2V) → CLKVDD12 (1.2V)

3. AVDD18 (1.8V) → CLKVDD18 (1.8V)



Power Sequencer



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DVDD09, DC-DC before LDOs

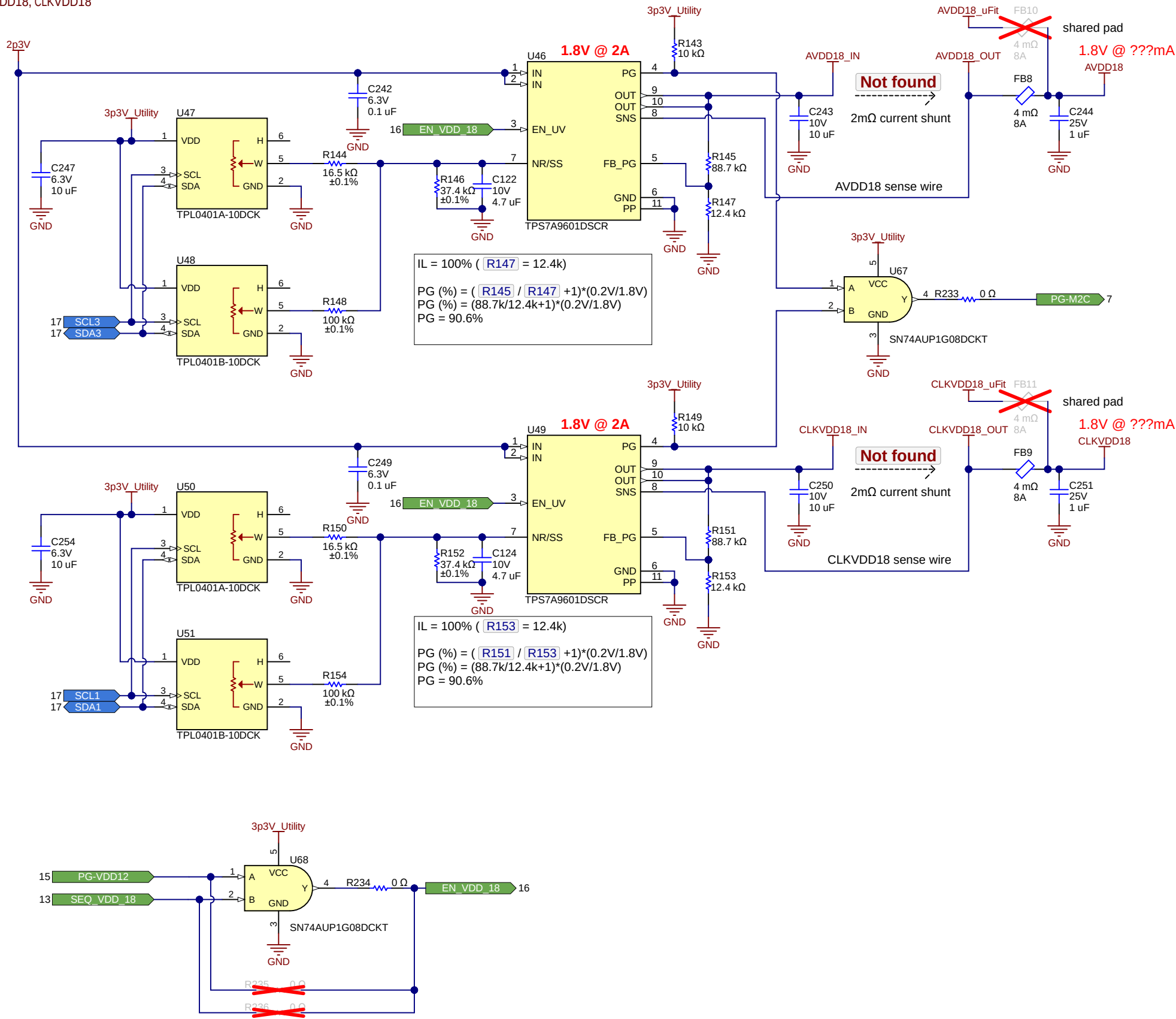


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EVM Power 4
AVDD18, CLKVDD18

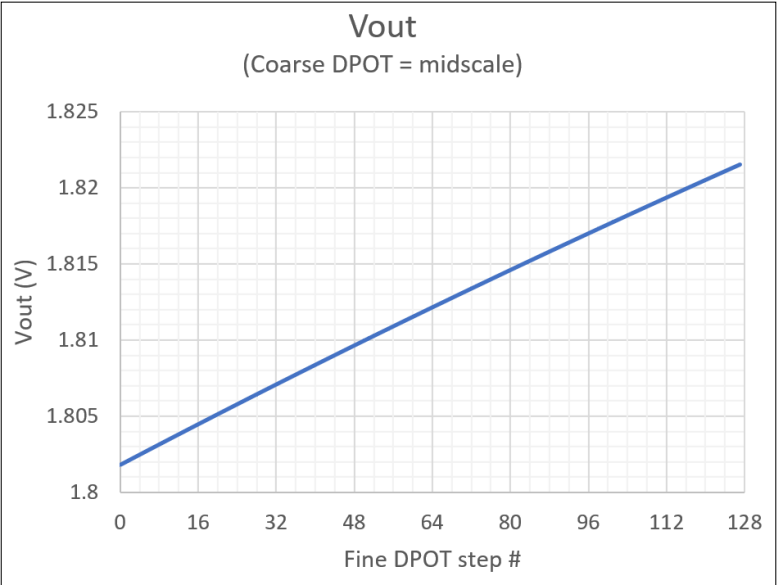
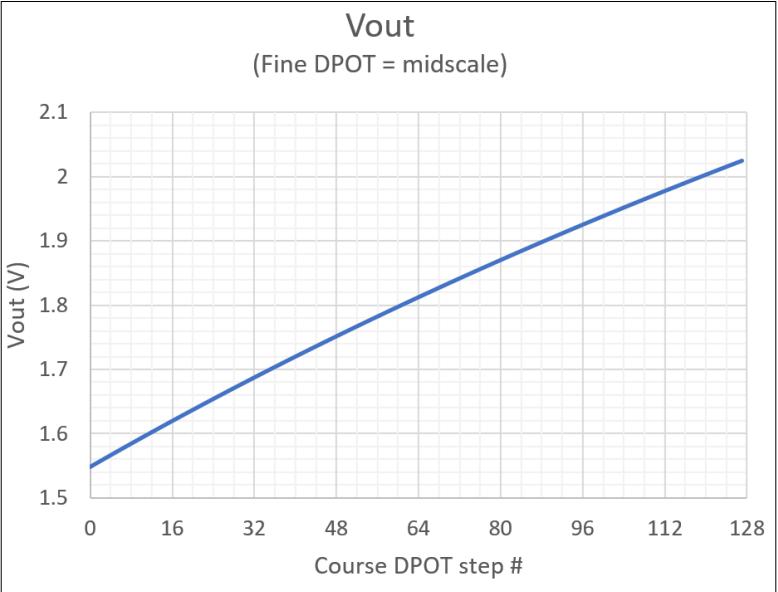


POWER UP SEQUENCE

1. DVDD (0.9V)
2. AVDD12 (1.2V) → CLKVDD12 (1.2V)
3. AVDD18 (1.8V) → CLKVDD18 (1.8V)

FOR ALL 1.8V MARGINING LDOs

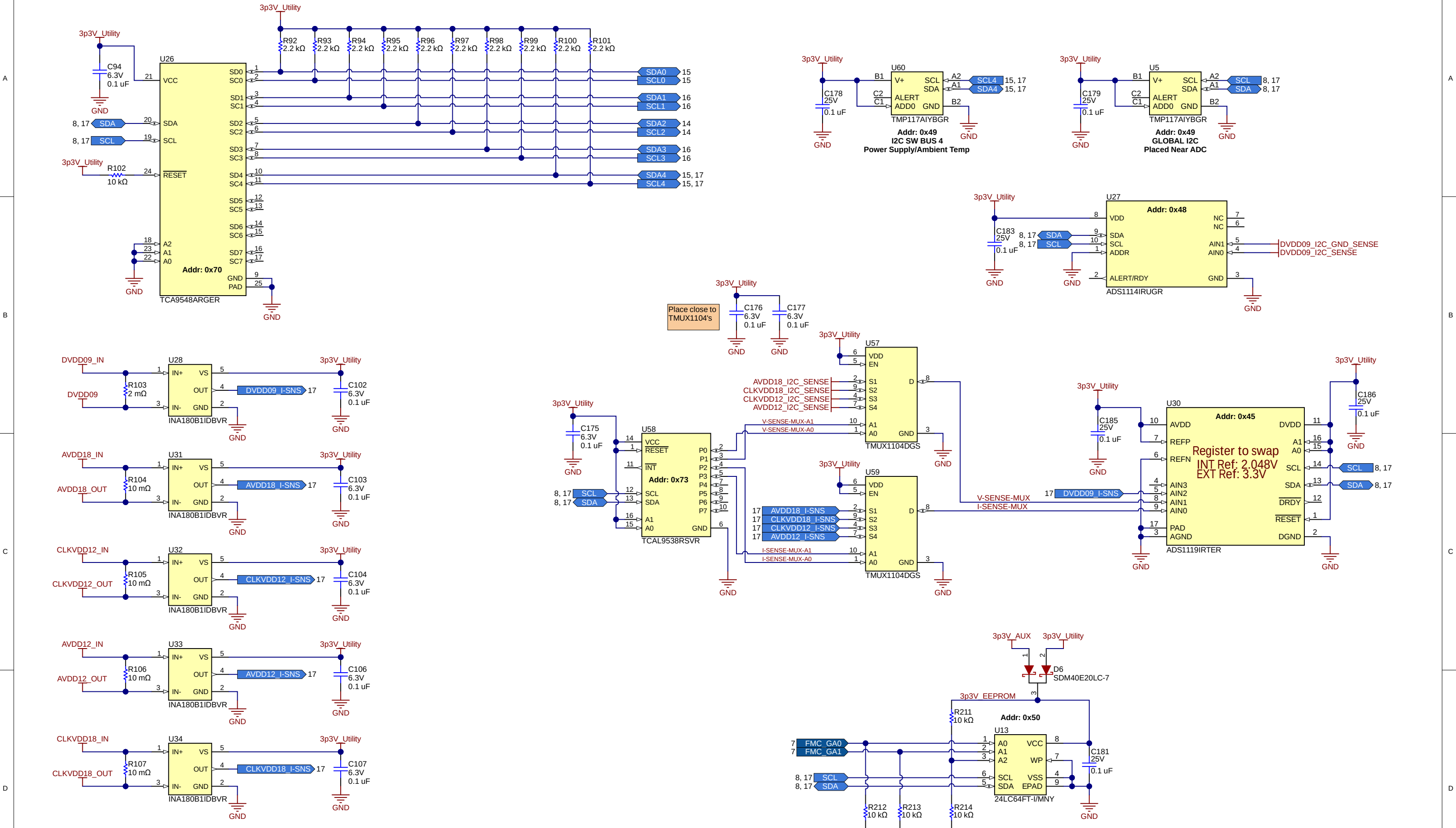
$$R_{NRSS} = 37.4k\Omega, R_{EQ_{COARSE}}(nom) = 21.5k\Omega, R_{EQ_{FINE}}(nom) = 105k\Omega$$
$$R_{EQ_{DPOTS}}(nom) = \frac{21.5k\Omega * 105k\Omega}{21.5k\Omega + 105k\Omega} = 17.8458498k\Omega$$
$$R_{EQ_{DPOTS_{NRSS}}}(nom) = \frac{17.8458498k\Omega * 37.4k\Omega}{17.8458498k\Omega + 37.4k\Omega} = 12.0811k\Omega \rightarrow V_{out} = 150\mu A * 12.0811k\Omega = 1.812V$$

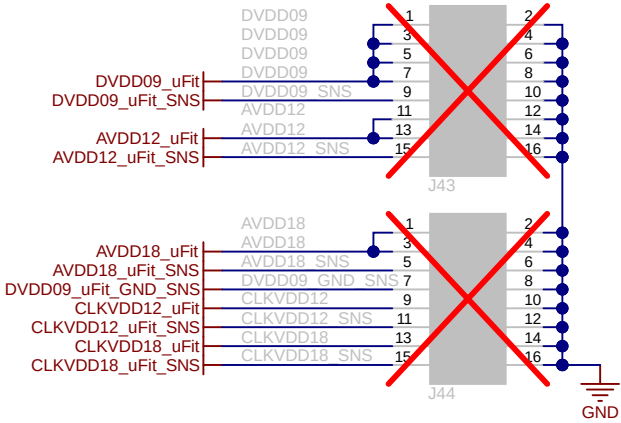


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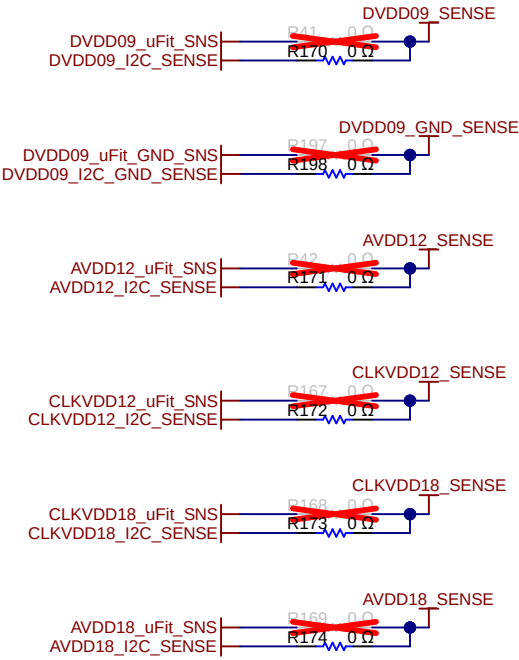
Orderable: Not For Public Release	Designed for: Not For Public Release	Mod. Date: 3/13/2025
TID #: Not For Public Release	Project Title: ADC34RF7xEVM	
Number: -	Rev: A	Sheet Title: EVM Power 4
SVN Rev: cfec0883921a2ab84ee9a1c5050b24b145022	ADC32RF77	Sheet: 16 of 20
Drawn By: CW	File: ADC34RF7x_Power4_RevA.SchDoc	Size: B
Engineer: CW	Contact: http://www.ti.com/support	

I2C Devices





Place 0 ohm resistor close to existing sense line to leave minimal stub



Misc Hardware/Logos

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

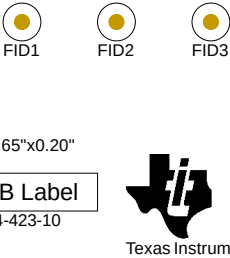
ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Variant/Label Table	
Variant	Label Text
001	ADC3xRF7x_RevE2

Size: 0.65"x0.20"
LBL1
PCB Label
THT-14-423-10



PCB
LOGO
FCC disclaimer



PCB Number: -
PCB Rev: A



PMSSS 440 0025 PH



2069-440-SS



PMSSS 440 0025 PH



2069-440-SS



Orderable: Not For Public Release		Designed for: Not For Public Release		Mod. Date: 2/24/2025	
TID #: Not For Public Release		Project Title: ADC34RF7xEVM			
Number: -		Rev: A		Sheet Title: Misc Hardware/Logos	
SVN Rev: 3549342212367fc0980ad0322001e956605c043		ADC32RF77		Sheet: 19 of 19	
Drawn By: CW		File: ADC34RF7x_Misc_RevA.SchDoc		Size: B	
Engineer: CW		Contact: http://www.ti.com/support			

Rev History & Variants

Revision History

Rev	Release Date	Notes
E1	Jun. 14, 2024	Initial Release
E2	Aug. 09, 2024	• Swap GPIO3 and GPIO11 (fixes default SDO mapping) • Simplify SPI pullup/pulldown • Changes defaults for onboard power • Differential clock input (RF72 only) and single ended analog inputs • Fix LED current limit resistors • Swap AIN0 and AIN1 inputs on ADS1114 • Combines I2C buses with optional break point • I2C bus pullup decreased to 3.74kΩ • Added second TMP117 on I2C bus 4 near power supply • Replaced all INA226 with INA180 shunts • Uses I2C IO expander for switching supply sense MUXes • EEPROM uses low Vf diode for powering through 3p3V_Utility and 3p3V_AUX (if connected to supporting FMC) • Updated DNI list to remove uncommonly used headers which are in high density areas • SYNCb routed to H31 through shared pad
E3	Jan. 28, 2025	• Separates RESETb onto unique MUX for individual control • Allows break from RESETb to only use manual switch into watchdog • Adds 0Ω series R onto PDN and RESETb paths from FMC

Variant(s)

Variant	Notes
001	• ADC34RF72
002	• ADC32RF77

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