Dual IF Receivers with SNRBoost^{3G+} Signal Processing

Check for Samples: ADS58C20 , ADS58C23

FEATURES

- **Maximum Input Sample Rate: 500 MSPS**
- **Maximum Output Sample Rate: 250 MSPS**
- **Resolution: 9-Bit/14-Bit Configurable**
- **Signal Processing with SNRBoost^{3G+} and Decimating Filter**
- **Wide Bandwidth Capture**
  - **75-MHz Signal Bandwidth per ADC Centered at Fs × 3/8**
  - **Using SNRBoost^{3G+} Signal Processing**
- **High Dynamic Performance (with SNRBoost^{3G+}enabled)**
  - **91dBc SFDR (HD2 to 5) in 75-MHz Band Centered at Fs × 3/8**
  - **94dBc SFDR (other than HD2 to 5) in 75-MHz Band Centered at Fs × 3/8**
  - **68dBFS MIN SNR in 75-MHz Band Centered at Fs × 3/8**
  - **75dBFS MIN SNR in 40-MHz Band Centered at Fs × 3/8**
  - **1W/Channel Power with SNRBoost^{3G+} Enabled**
- **High Dynamic Performance (14-bit mode, 125MHz band)**
  - **87dBc SFDR at 170MHz IF**
  - **70dBFS SNR at 170MHz IF**
  - **650mW/Channel Power**
- **High Impedance Input**
- **80-Pin TQFP Package with PowerPAD™**

APPLICATIONS

- **Multi-Carrier GSM Cellular Infrastructure Base Stations**
- **Multi-Carrier, Multi-Mode Cellular Infrastructure Base Stations**

DESCRIPTION

The ADS58C20 and ADS58C23 are dual IF receivers for wideband, multi-mode cellular infrastructure base stations. Each channel consists of two interleaved ADCs running at 250MSPS. The ADCs are followed by a 2x decimating filter centered at 1/8 × Fs or 3/8 × Fs providing high dynamic performance up to 110 MHz of bandwidth. This architecture eases front end filter design for wide bandwidth receivers. The devices have integrated buffers at the analog inputs with benefits of uniform performance and input impedance across a wide frequency range. The ADS58C2x use a novel implementation of the SNRBoost^{3G+} signal processing technology to provide high SNR in a band up to 75 MHz wide with only 9-bit output resolution. The ADS58C20 is a high performance part with superior specifications. The devices are available in a 80-pin TQFP package and is specified over the full industrial temperature range (–40°C to 85°C).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

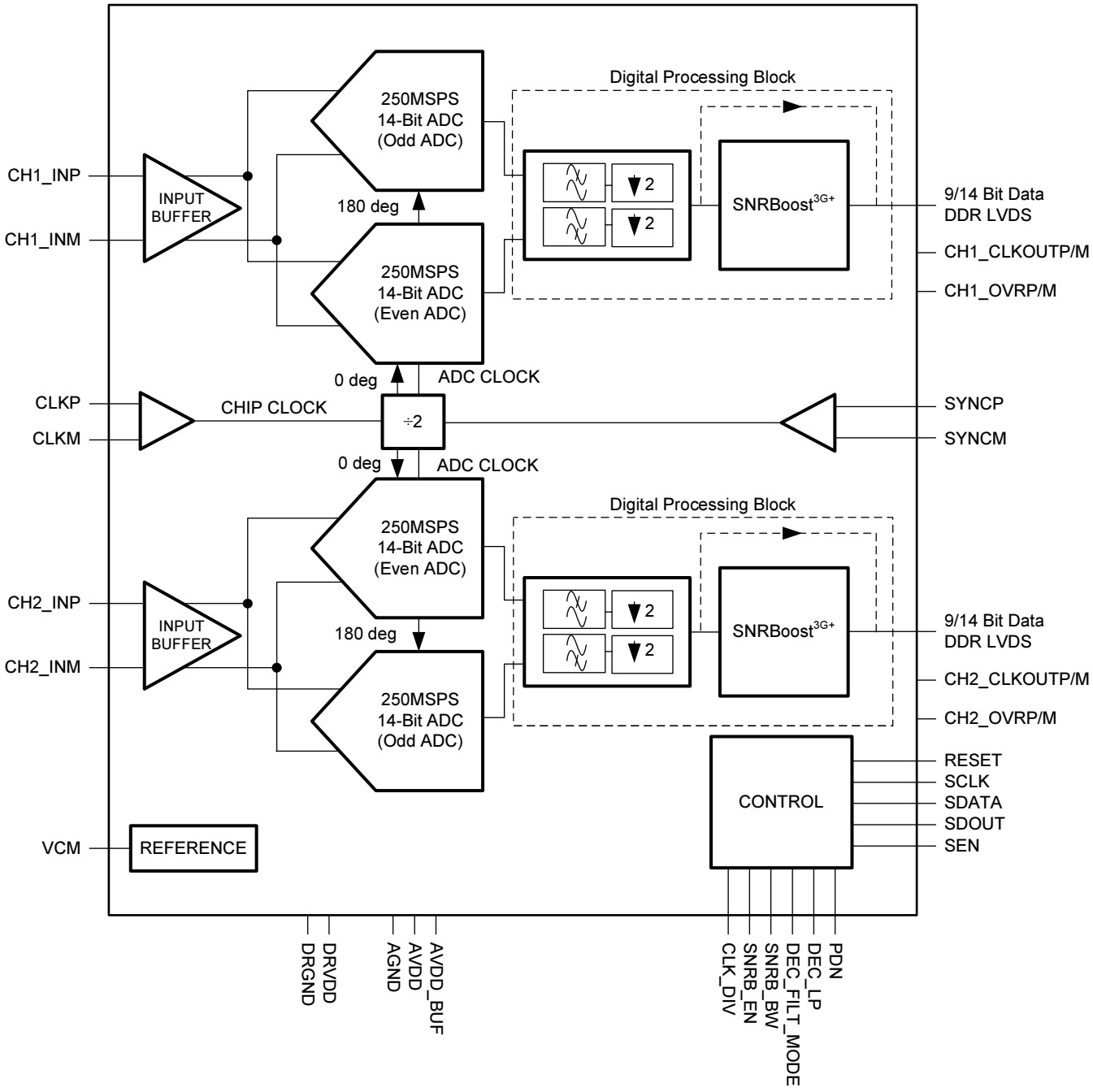
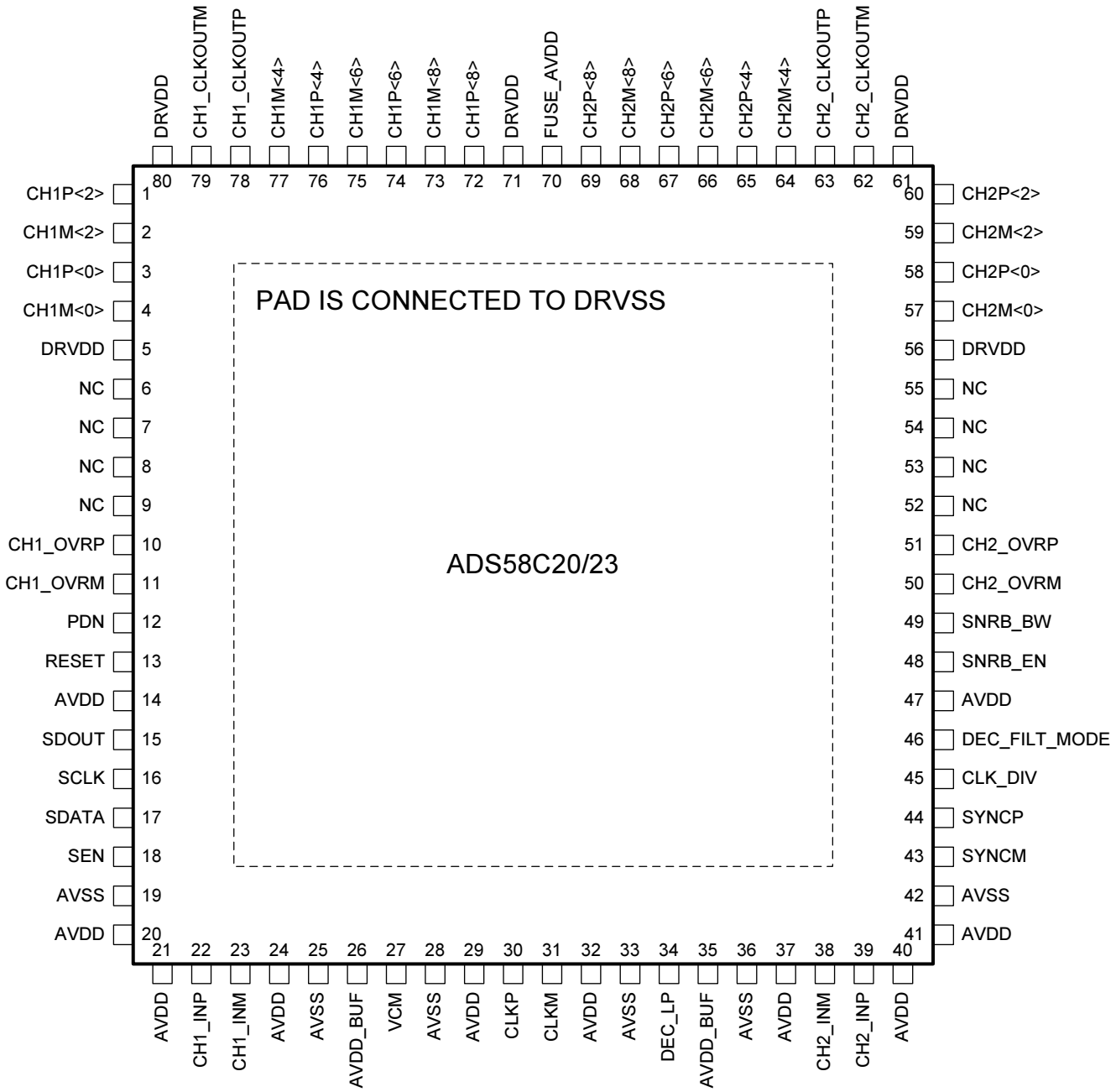


Figure 1. ADS58C20/23 Block Diagram

DEVICE INFORMATION

PFP PACKAGE (9 Bit)
(TOP VIEW)



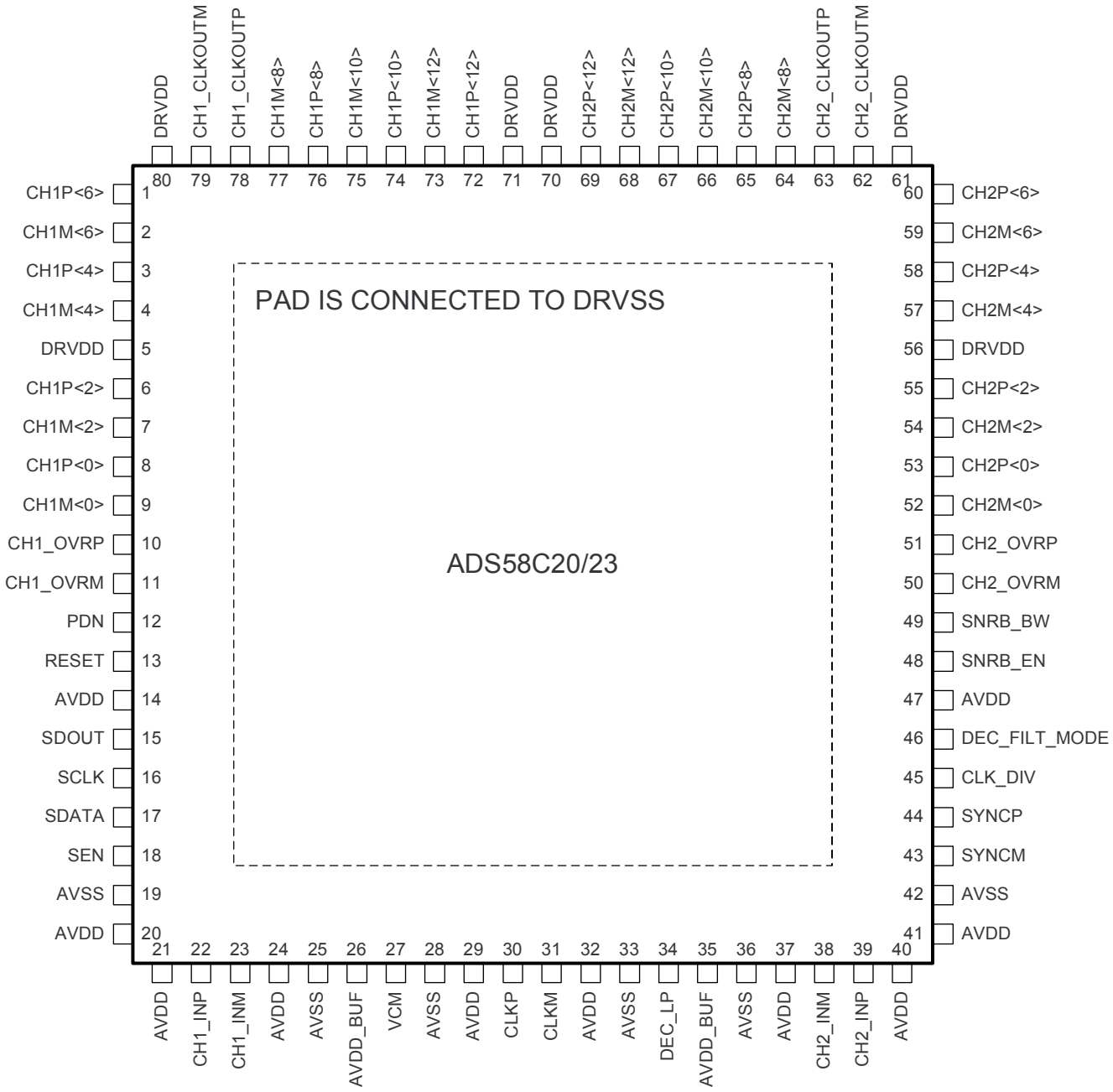
PIN FUNCTIONS (9-Bit Mode)

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL/SERIAL			
SCLK	16	I	Serial interface clock.This pin has an internal 170kΩ pull-down resistor.
SEN	18	I	Serial interface enable.This pin has an internal 170kΩ pull-up resistor.
SDATA	17	I	Serial interface data input.This pin has an internal 170kΩ pull-down resistor.
SDOUT	15	O	Serial interface data output, CMOS output (off DRVDD supply).

PIN FUNCTIONS (9-Bit Mode) (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RESET	13	I	Serial interface register reset. Active high.This pin has an internal 170kΩ pull-down resistor.
PDN	12	I	Chip power down. Active high.This pin has an internal 170kΩ pull-down resistor.
DEC_LP	34	I	0 - Enables high pass decimating filter 1 - Enables low pass decimating filter This pin has an internal 170kΩ pull-down resistor.
DEC_FILT_MODE	46	I	0 – Enables low latency decimating filter 1 – Enables high performance decimation filter with larger latency. This pin has an internal 170kΩ pull-down resistor.
SNRB_BW	49	I	0 – Enables 40MHz BW for SNRBoost^{3G+} 1 – Enables 75MHz BW for SNRBoost^{3G+} This pin has an internal 170kΩ pull-down resistor.
SNRB_EN	48	I	0-Disables SNRBoost^{3G+} 1-Enables SNRBoost^{3G+} This pin has an internal 170kΩ pull-down resistor
CLK_DIV	45	I	Control pin for selecting input clock divider ratio. 0 – Div by 2 1 – Div by 4 This pin has an internal 170kΩ pull-down resistor.
DATA INTERFACE			
CH1P/M<n>	1–4, 72–77	O	9-bit DDR LVDS output data for CH1. See Figure 2 on LVDS Data Format.
CH2P/M<n>	57–60, 64–69	O	9-bit DDR LVDS output data for CH2. See Figure 2 on LVDS Data Format.
NC	6–9,52–55	–	Do not connect
CH1_OVRP/M	10, 11	O	CH1 over-range indicator
CH2_OVRP/M	50, 51	O	CH2 over-range indicator
CH1_CLKOUTP/M	78, 79	O	Differential output clock for CH1 data
CH2_CLKOUTP/M	62, 63	O	Differential output clock for CH2 data
INPUT/REFERENCE			
CH1_INP/M	22, 23	I	Differential analog input for CH1
CH2_INP/M	38, 39	I	Differential analog input for CH2
VCM	27	O	Common-mode voltage for analog inputs, 1.9V
CLOCK/SYNC			
CLKP/M	30, 31	I	Refers to chip clock rate. Chip clock input is 2x or 4x of each interleaved ADC clock rate, referred to as 1x clock
SYNCP/M	43, 44	I	External sync input for clock divider (at 1x clock rate). If not used, do not float the pins-tie SYNCP to AVDD and SYNCM to ground.
POWER SUPPLY			
DRVDD	5, 56,61,70, 71,80	I	1.8V digital and output buffer supply
DRVSS	Thermal pad	I	Digital and output buffer ground
AVDD	14, 20, 21, 24, 29, 32, 37, 40, 41, 47,	I	1.9V analog supply
AVDD_BUF	26, 35	I	3.3V input buffer supply
AVSS	19, 25, 28, 33, 36, 42,	I	Analog ground

PFP PACKAGE (14 Bit)
(TOP VIEW)



PIN FUNCTIONS (14-Bit Mode)

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL/SERIAL			
SCLK	16	I	Serial interface clock.This pin has an internal 170kΩ pull-down resistor.
SEN	18	I	Serial interface enable.This pin has an internal 170kΩ pull-up resistor.
SDATA	17	I	Serial interface data input.This pin has an internal 170kΩ pull-down resistor.
SDOUT	15	O	Serial interface data output, CMOS output (off DRVDD supply).
RESET	13	I	Serial interface register reset. Active high.This pin has an internal 170kΩ pull-down resistor.
PDN	12	I	Chip power down. Active high.This pin has an internal 170kΩ pull-down resistor.

PIN FUNCTIONS (14-Bit Mode) (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DEC_LP	34	I	0 - Enables high pass decimating filter 1 - Enables low pass decimating filter This pin has an internal 170kΩ pull-down resistor.
DEC_FILT_MODE	46	I	0 – Enables low latency decimating filter 1 – Enables high performance decimation filter with larger latency. This pin has an internal 170kΩ pull-down resistor.
SNRB_BW	49	I	0 – Enables 40MHz BW for SNRBoost^{3G+} 1 – Enables 75MHz BW for SNRBoost^{3G+} This pin has an internal 170kΩ pull-down resistor.
SNRB_EN	48	I	0-Disables SNRBoost^{3G+} 1-Enables SNRBoost^{3G+} This pin has an internal 170kΩ pull-down resistor
CLK_DIV	45	I	Control pin for selecting input clock divider ratio. 0 – Div by 2 1 – Div by 4 This pin has an internal 170kΩ pull-down resistor.
DATA INTERFACE			
CH1P/M<n>	1–4, 6–9, 72–77	O	9-bit DDR LVDS output data for CH1. See Figure 3 on LVDS Data Format.
CH2P/M<n>	52–55, 57–60, 64–69,	O	9-bit DDR LVDS output data for CH2. See Figure 3 on LVDS Data Format.
CH1_OVRP/M	10, 11	O	CH1 over-range indicator
CH2_OVRP/M	50, 51	O	CH2 over-range indicator
CH1_CLKOUTP/M	78, 79	O	Differential output clock for CH1 data
CH2_CLKOUTP/M	62, 63	O	Differential output clock for CH2 data
INPUT/REFERENCE			
CH1_INP/M	22, 23	I	Differential analog input for CH1
CH2_INP/M	38, 39	I	Differential analog input for CH2
VCM	27	O	Common-mode voltage for analog inputs, 1.9V
CLOCK/SYNC			
CLKP/M	30, 31	I	Refers to chip clock rate. Chip clock input is 2x or 4x of each interleaved ADC clock rate, referred to as 1x clock
SYNCP/M	43, 44	I	External sync input for clock divider (at 1x clock rate). If not used, do not float the pins-tie SYNCP to AVDD and SYNCM to ground.
POWER SUPPLY			
DRVDD	5, 56,61,70, 71,80	I	1.8V digital and output buffer supply
DRVSS	Thermal pad	I	Digital and output buffer ground
AVDD	14, 20, 21, 24, 29, 32, 37, 40, 41, 47	I	1.9V analog supply
AVDD_BUF	26, 35	I	3.3V input buffer supply
AVSS	19, 25, 28, 33, 36, 42	I	Analog ground

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE- LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS58C20	TQFP-80	PFP	–40C to +85°C	ADS58C20I	ADS58C20IPFP	TRAY
					ADS58C20IPFPR	TAPE AND REEL
ADS58C23(2)				ADS58C23I	ADS58C23IPFP	TRAY
					ADS58C23IPFPR	TAPE AND REEL

(1) For the most current product and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) PRODUCT PREVIEW

EXPORT CLASSIFICATION

ADS58C20/23	Export Classification Number 5A991.b

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range, AVDD		–0.3	2.1	V
Supply voltage range, AVDD_BUF		–0.3	3.6	V
Supply voltage range, DRVDD		–0.3	2.1	V
Voltage between AGND and DRGND		–0.3	0.3	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		–2.4	2.4	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		–2.4	2.4	V
Voltage between AVDD_BUF to DRVDD/AVDD		–3.9	3.9	V
Voltage applied to input pins	INP, INM	–0.3V	minimum (1.9, AVDD + 0.3V)	V
	CLKP, CLKM(2)	–0.3	AVDD + 0.3V	V
	SYNCP, SYNCM	–0.3	AVDD + 0.3V	V
	SCLK, SEN, SDATA, SDOUT, RESET, PDN, DEC_LP, DEC_FILT_MODE, SNRB_BW, SNRB_EN, CLK_DIV	–0.3	3.9	V
Operating free-air temperature range, T_A		–40	85	°C
Operating junction temperature range, T_J			125	°C
Storage temperature range, T_{stg}		–65	150	°C
ESD, human body model			2	kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is < |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS58C20	UNITS
		TQFP (80) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	21.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	9.3	
θ_{JB}	Junction-to-board thermal resistance	8.2	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	4.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
SUPPLIES					
Analog supply voltage, AVDD		1.8	1.9	2.0	V
Analog buffer supply voltage, AVDD_BUF		3.15	3.3	3.45	V
Digital supply voltage, DRVDD		1.7	1.8	2.0	V
ANALOG INPUTS					
Differential input voltage range (1)	SNRBoost^{3G+}OFF, Filter bypassed, 0dB digital gain		1.9		V_{PP}
Maximum analog input frequency with 1.9V_{PP} input amplitude (1)			300		MHz
Maximum analog input frequency with 1.4V_{PP} input amplitude (1)			400		MHz
Input common-mode voltage			VCM ± 0.025		V
CLOCK INPUT					
Input clock frequency	Chip Clock Frequency	100		500	MHz
Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.2	1.5		V_{PP}
	LVPECL, ac-coupled		1.6		
	LVDS, ac-coupled		0.7		
Input clock duty cycle	Default after reset	35%	50%	65%	
DIGITAL OUTPUTS					
Maximum external load capacitance from each output pin to DRGND, C_{LOAD}			5		pF
Differential load resistance between the LVDS output pairs (LVDS mode), R_{LOAD}			100		Ω
Operating free-air temperature, T_A		–40		85	°C
HIGH PERFORMANCE MODES - It is recommended to enable the special modes listed below:					
Register address 0xF7, set <SPECIAL MODE1> to 1					
Register address 0xF7, set <SPECIAL MODE2> to 1					
Register address 0xBA, set <SPECIAL MODE3> to 1					
Register address 0xE0, set <SPECIAL MODE4> to 11					
Register address 0xEE, set <SPECIAL MODE5> to 1					
It is must to write the below mode after reset or wake up from power down in exact sequence given below: Register address 0x04, set <SPECIAL MODE6> to 1 Register address 0x04, reset <SPECIAL MODE6> to 0					

(1) See MAXIMUM APPLICABLE INPUT AND OUTPUT POWER section

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, chip clock frequency = 500 MHz, ADC clock frequency = 250 MHz, 50% clock duty cycle, AVDD_BUF = 3.3V, AVDD = 1.9V, DRVDD =1.8V, –1dBFS output signal, (unless otherwise noted) Min & max values are specified across the full temperature range T_{min}= -40°C to T_{max} = 85°C, AVDD=1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Differential input voltage range(1)			1.9		V_{PP}
	Differential input impedance R+jX (at 200 MHz)			50		Ω
	Differential input capacitance (at 200 MHz)			5.6		pF
	Analog input bandwidth	With 50Ω source impedance, and 50Ω termination		750		MHz
	Analog input common-mode current (each channel)			8		µA
	VCM common-mode voltage output			1.9		V
	VCM output current capability			1		mA
POWER SUPPLY						
IAVDD	Analog supply current	Default after Reset (9-bit mode, SNRBoost OFF, Filter ON)		365	410	mA
IAVDD_BUF	Analog buffer supply current			103	135	mA
IDRVDD	Output buffer supply current LVDS interface	Default after Reset (9-bit mode, SNRBoost OFF, Filter ON), 350mV LVDS swing, Input signal applied to one channel"		335	390	mA
		9-bit mode, SNRBoost ON, Filter ON		530	600	
	Analog power (AVDD+AVDD_BUF supply)			1.03		W
	Digital power LVDS interface (DRVDD supply)			0.6		W
	Power Consumption in Global Power Down Mode			5		mW
DC ACCURACY						
	Offset error	Specified across devices and channels within a device	–15		15	mV
There are two sources of gain error: internal reference inaccuracy and channel gain error						
	Gain error as a result of internal reference inaccuracy alone	Specified across devices and channels within a device	–5		5	%FS
	Gain error of channel alone	Specified across devices and channels within a device		±3		%FS
	Channel gain error temperature coefficient			0.001		Δ%/°C

(1) See MAXIMUM APPLICABLE INPUT AND OUTPUT POWER section

ELECTRICAL CHARACTERISTICS: 9-BIT MODE, FILTER ENABLED, SNRBoost^{3G+} ENABLED

TTypical values at T_A = 25°C, AVDD_BUF = 3.3V, AVDD = 1.9V, DRVDD = 1.8V, chip clock frequency = 500MHz, ADC clock frequency = 250 MHz, input signal frequency = 170MHz, 2x decimation, 50% clock duty cycle, –2dBFS output signal, (unless otherwise noted) Min & max values are specified over the full temperature range T_{min}= -40°C to T_{max} = 85°C, AVDD=1.9V, AVDD_BUF=3.3V, DRVDD=1.8V

PARAMETER	TEST CONDITIONS	ADS58C20			ADS58C23			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SNR Signal-to-noise ratio, LVDS	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	75	77.5			77.5		dBFS
	75 MHz bandwidth around 187.5MHz, 1.9dB Gain	68	70.5			70.5		
SINAD Signal-to-noise and distortion ratio	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	73.5	77			77		dBFS
	75 MHz bandwidth around 187.5MHz, 1.9dB Gain	67.5	70.3			70.3		
Harmonic distortion, HD2 to HD5	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	83	91			91		dBc
	75 MHz bandwidth around 187.5MHz, 1.9dB Gain	83	91			91		
Worst spur, other than HD2 to HD5	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	87	94			94		dBc
	75 MHz bandwidth around 187.5MHz, 1.9dB Gain	87	94			94		
SFDR Spurious free dynamic range	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	83	91			91		dBc
	75 MHz bandwidth around 187.5MHz, 1.9dB Gain	83	91			91		
THD Total harmonic distortion	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	80	87			87		dBc
	75 MHz bandwidth around 187.5MHz, 1.9dB Gain	80	87			87		
IMD Two-tone intermodulation distortion	F1 = 185 MHz, F2 = 190 MHz, each tone at –7dBFS		94.5			94.5		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6dB overload with sine wave input		1			1		Output Clock
Crosstalk	With a full-scale 170 MHz signal on aggressor and no signal on victim channel		>100			>100		dB
PSRR AC power-supply rejection ratio	For 50mV_{PP} signal on AVDD supply		<30			<30		dB

ELECTRICAL CHARACTERISTICS: 14-BIT MODE, DECIMATION FILTER ENABLED, SNRBoost^{3G+} DISABLED

Typical values at T_A = 25°C, AVDD_BUF = 3.3V, AVDD = 1.9V, DRVDD = 1.8V, chip clock frequency = 500 MHz, ADC Clock frequency = 250 MHz, Input signal frequency=170MHz, 2x decimation, 50% clock duty cycle, –1dBFS output signal, (unless otherwise noted) Min & max values are specified over the full temperature range T_{min} = -40°C to T_{max} = 85°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V

PARAMETER	TEST CONDITIONS	ADS58C20			ADS58C23			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SNR Signal-to-noise ratio, LVDS	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	75	77.5			77.5		dBFS
	75 MHz bandwidth around 187.5MHz, 0.5dB Gain	71.5	74			74		
SINAD Signal-to-noise and distortion ratio	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	73.5	77			77		dBFS
	75 MHz bandwidth around 187.5MHz, 0.5dB Gain	70.5	73.6			73.6		
Harmonic distortion, HD2 to HD5	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	83	91			91		dBc
	75 MHz bandwidth around 187.5MHz, 0.5dB Gain	83	91			91		
Worst spur, other than HD2 to HD5	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	87	94			94		dBc
	75 MHz bandwidth around 187.5MHz, 0.5dB Gain	87	94			94		
SFDR Spurious free dynamic range	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	83	91			91		dBc
	75 MHz bandwidth around 187.5MHz, 0.5dB Gain	83	91			91		
THD Total harmonic distortion	40 MHz bandwidth around 187.5MHz, 0.5dB Gain	80	87			87		dBc
	75 MHz bandwidth around 187.5MHz, 0.5dB Gain	80	87			87		
IMD Two-tone intermodulation distortion	F1 = 185 MHz, F2 = 190 MHz, Each tone at –7dBFS		94			94		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6dB overload with sine wave input		1			1		Output Clock
Crosstalk	With a full-scale 170 MHz signal on aggressor and no signal on victim channel		>100			>100		dB
PSRR AC power-supply rejection ratio	For 50mV$_{PP}$ signal on AVDD supply		<30			<30		dB

ELECTRICAL CHARACTERISTICS: 14-BIT MODE, DECIMATION FILTER DISABLED, SNRBoost^{3G+} DISABLED

Typical values at T_A = 25°C, AVDD_BUF = 3.3V, AVDD = 1.9V, DRVDD = 1.8V, chip clock frequency = 500MHz, ADC clock frequency = 250 MHz, 50% clock duty cycle, –1dBFS output signal, (unless otherwise noted) Min & max values are specified over the full temperature range T_{min}= -40°C to T_{max} = 85°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD=1.8V

PARAMETER	TEST CONDITIONS	ADS58C20			ADS58C23			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SNR Signal-to-noise ratio, LVDS	Fin = 170 MHz, Digital gain = 0.5dB	67	70			70		dBFS
SINAD Signal-to-noise and distortion ratio	Fin = 170 MHz, Digital gain = 0.5dB	66	69.5			69.5		dBFS
Harmonic Distortion, HD2 to HD3	Fin = 170 MHz, Digital gain = 0.5dB	74.5	87			87		dBc
Worst Spur, other than HD2 to HD3	Fin = 170 MHz, Digital gain = 0.5dB	84	96			96		dBc
SFDR, Spurious free dynamic range	Fin = 170 MHz, Digital gain = 0.5dB	74.5	87			87		dBc
THD Total harmonic distortion	Fin = 170 MHz, Digital gain = 0.5dB	71.5	82			82		dBc
IMD Two-tone intermodulation distortion	F1 = 185 MHz, F2 = 190 MHz, Each tone at –7dBFS		91			91		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6dB overload with sine wave input		1			1		Clock cycles
Crosstalk	With a full-scale 170 MHz signal on aggressor and no signal on victim channel		>100			>100		dB
PSRR AC power-supply rejection ratio	For 50mV$_{PP}$ signal on AVDD supply		<30			<30		dB

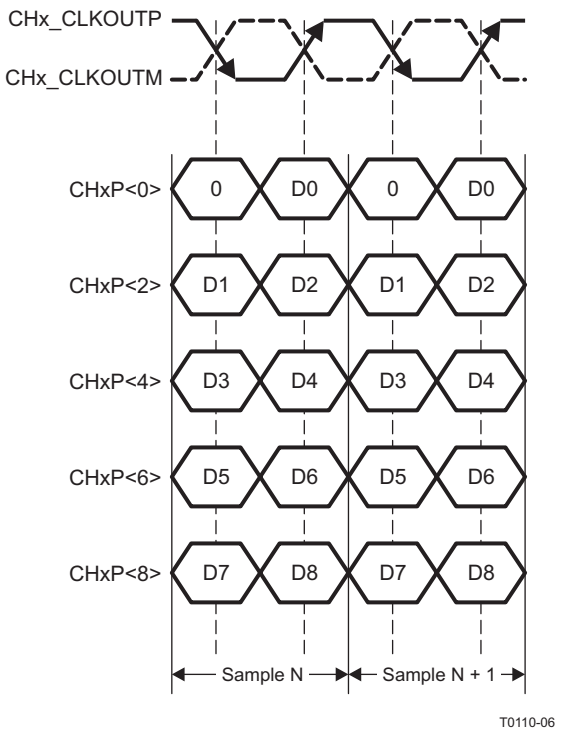


Figure 2. LVDS Output BIt Order in 9 Bit Mode

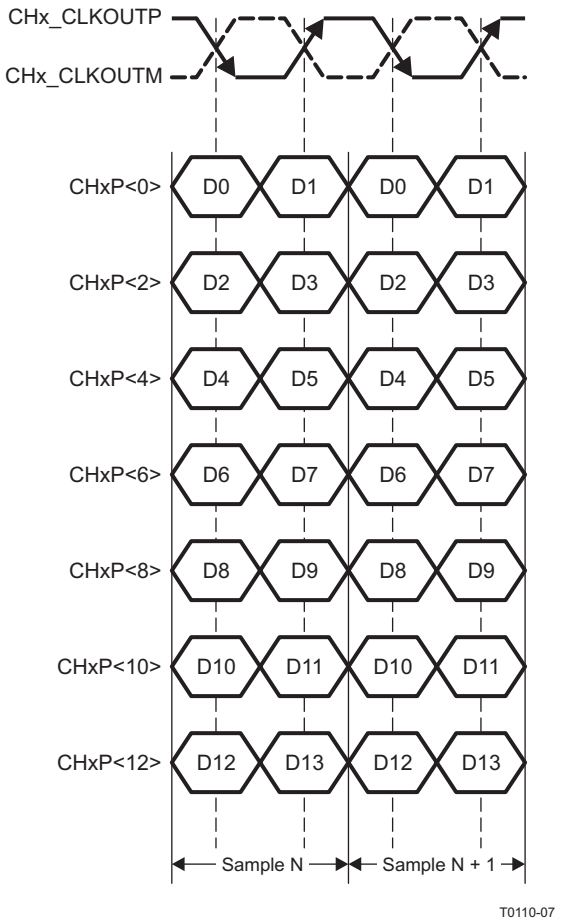
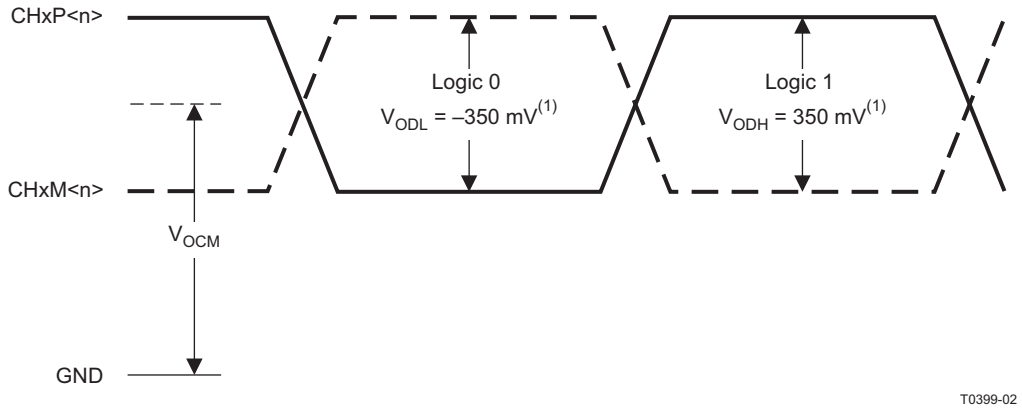


Figure 3. LVDS Output BIt Order in 14 Bit Mode

DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 1.9V, DRVDD = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital inputs - RESET, SCLK, SDATA, SEN, PDN, SNRB_EN, SNRB_BW, DEC_FILT_MODE, DEC_LP, CLK_DIV (1)						
High-level input voltage		**All pins support 1.8V and 3.3V cmos logic levels**	1.3			V
Low-level input voltage					0.4	V
High-level input current	RESET, SCLK, SDATA, PDN, SNRB_EN, SNRB_BW, DEC_FILT_MODE, DEC_LP, CLK_DIV	V_{HIGH} = 1.8V		10		µA
	SEN	V_{HIGH} = 1.8V		0		µA
Low-level input current	RESET, SCLK, SDATA, PDN, SNRB_EN, SNRB_BW, DEC_FILT_MODE, DEC_LP, CLK_DIV	V_{LOW} = 0V		0		µA
	SEN	V_{LOW} = 0V		–10		µA
DIGITAL OUTPUTS – SDOUT						
High-level output voltage			DRVDD – 0.1	DRVDD		V
Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS – LVDS INTERFACE (CHxP/M, CHx_OVRP/M, CHx_CLKOUTP/M)						
V_{ODH}, High-level output voltage		Standard swing LVDS	255	350	445	mV
V_{ODL}, Low-level output voltage		Standard swing LVDS	–445	–350	–255	mV
V_{ODH}, High-level output voltage		Low swing LVDS		120		mV
V_{ODL}, Low-level output voltage		Low swing LVDS		–120		mV
V_{OCM}, Output common-mode voltage			0.85	1.05	1.35	V
DIGITAL FILTER						
Low latency decimation filter		1dB bandwidth, Chip clock frequency = 500 MSPS		110		MHz
		Pass-band ripple		±0.3		dB
		Stop-band attenuation	17			dB



(1) With external 100 Ω termination

Figure 4. LVDS Voltage Levels

TIMING CHARACTERISTICS(1)

Typical values are at +25°C, AVDD = 1.9V, AVDD_BUF=3.3V, DRVDD = 1.8V, chip clock frequency = 500 MSPS, sine wave input clock, C_{LOAD} = 5pF(2), and R_{LOAD} = 100Ω(3), unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, AVDD_BUF = 3.3V and DRVDD = 1.7V to 2.0V.

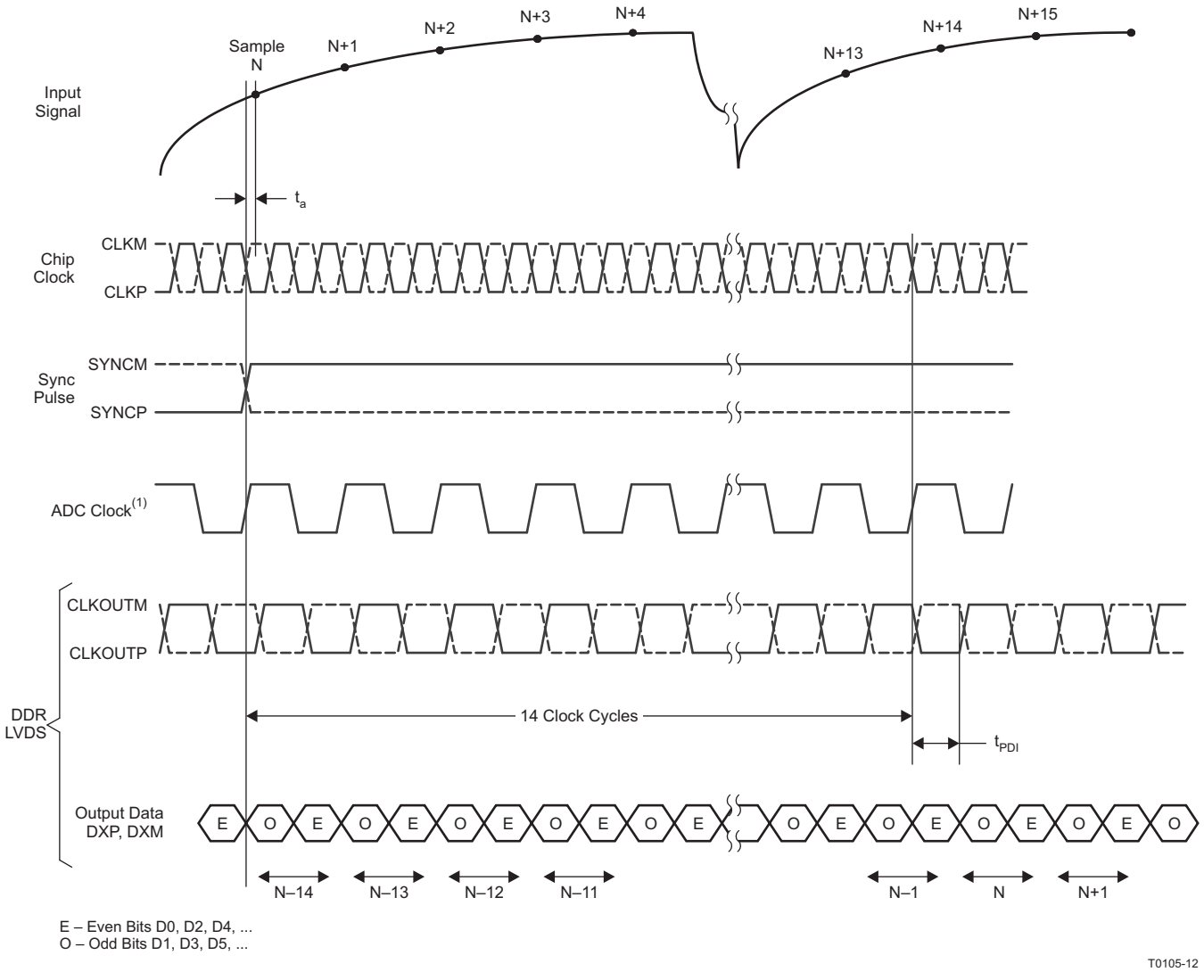
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay		0.7	1.2	1.6	ns
	Aperture delay matching	Between the two channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±150		ps
t_J	Aperture jitter	With divide by 2 option for input clock		130		f_S rms
	Wakeup time	Time to valid data after coming out of Channel power-down mode		10	100	µs
	ADC latency(4)	Default latency with SNRBoost3G+ :OFF; Filter: ON; Digital gain: OFF		14+Filter's delay		Output clock cycles
		Latency with SNRBoost3G+ :ON; Filter: ON; Digital gain: OFF		16+Filter's delay		
		Latency with SNRBoost3G+ :ON; Filter: ON; Digital gain: ON		19+Filter's delay		
DDR LVDS MODE(5)						
Data setup time(6)(7)		Data valid to zero-crossing of CHx_CLKOUTP(8)				
t_{SU0}	For output bits D0-D1 of 14-bit mode	CHxP/M<0> of 14-bit mode	0.68	1.0		ns
t_{SU2}	For output bits D2-D3 of 14-bit mode	CHxP/M<2> of 14-bit mode	0.68	1.0		ns
t_{SU4}	For output bits D4-D5 of 14-bit mode (For output bit D0 of 9bit mode)	CHxP/M<4> of 14-bit mode, CHxP/M<0> of 9-bit mode	0.67	1.0		ns
t_{SU6}	For output bits D6-D7 of 14-bit mode (For output bit D1-D2 of 9bit mode)	CHxP/M<6> of 14-bit mode, CHxP/M<2> of 9-bit mode	0.65	1.0		ns
t_{SU8}	For output bits D8-D9 of 14-bit mode (For output bits D3-D4 of 9bit mode)	CHxP/M<8> of 14-bit mode, CHxP/M<4> of 9-bit mode	0.61	1.0		ns
t_{SU10}	For output bits D10-D11 of 14-bit mode (For output bits D5-D6 of 9bit mode)	CHxP/M<10> of 14-bit mode, CHxP/M<6> of 9-bit mode	0.67	1.1		ns
t_{SU12}	For output bits D12-D13 of 14-bit mode (For output bits D7-D8 of 9bit mode)	CHxP/M<12> of 14-bit mode, CHxP/M<8> of 9-bit mode	0.57	1.0		ns
t_{SU_OVR}	For OVR output bits	CHx_OVRP/M	0.78	1.2		ns
Data hold time(6)(7)		Zero-crossing of CHx_CLKOUTP to data becoming invalid				
t_{H0}	For output bits D0-D1 of 14-bit mode	CHxP/M<0> of 14-bit mode	0.59	0.8		ns
t_{H2}	For output bits D2-D3 of 14-bit mode	CHxP/M<2> of 14-bit mode	0.59	0.77		ns
t_{H4}	For output bits D4-D5 of 14-bit mode (For output bit D0 of 9bit mode)	CHxP/M<4> of 14-bit mode, CHxP/M<0> of 9-bit mode	0.5	0.77		ns
t_{H6}	For output bits D6-D7 of 14-bit mode (For output bit D1-D2 of 9bit mode)	CHxP/M<6> of 14-bit mode, CHxP/M<2> of 9-bit mode	0.55	0.77		ns
t_{H8}	For output bits D8-D9 of 14-bit mode (For output bits D3-D4 of 9bit mode)	CHxP/M<8> of 14-bit mode, CHxP/M<4> of 9-bit mode	0.63	0.83		ns
t_{H10}	For output bits D10-D11 of 14-bit mode (For output bits D5-D6 of 9bit mode)	CHxP/M<10> of 14-bit mode, CHxP/M<6> of 9-bit mode	0.52	0.73		ns
t_{H12}	For output bits D12-D13 of 14-bit mode (For output bits D7-D8 of 9bit mode)	CHxP/M<12> of 14-bit mode, CHxP/M<8> of 9-bit mode	0.52	0.79		ns
t_{H_OVR}	For OVR output bits	CHx_OVRP/M	0.2	0.5		ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CHx_CLKOUTP-CHx_CLKOUTM)		52%		
t_{PDI}	Clock propagation delay	Chip clock falling edge cross-over to rising edge of output clock	6.5	8	9.5	ns

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, tPDI is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) See Timing Diagram
(7) Setup and hold time of a channel are measured with respect same channel's output clock
(8) Data valid refers to a logic high of +100mV and a logic low of –100mV.

TIMING CHARACTERISTICS(1) (continued)

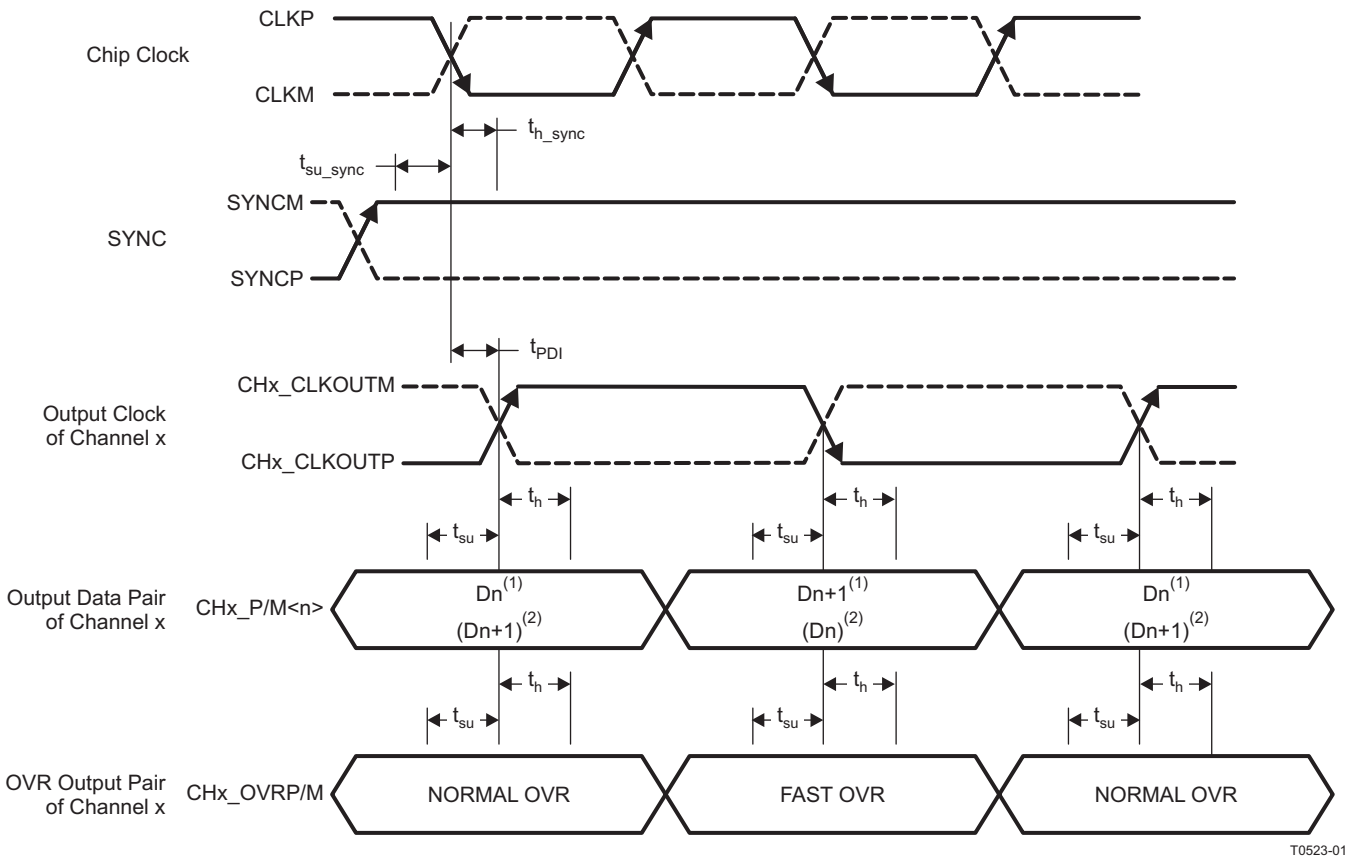
Typical values are at +25°C, AVDD = 1.9V, AVDD_BUF=3.3V, DRVDD = 1.8V, chip clock frequency = 500 MSPS, sine wave input clock, C_{LOAD} = 5pF(2), and R_{LOAD} = 100Ω(3), unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, AVDD_BUF = 3.3V and DRVDD = 1.7V to 2.0V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100mV to +100mV, Fall time measured from +100mV to –100mV		0.13		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100mV to +100mV, Fall time measured from +100mV to –100mV		0.14		ns



(1) When a pulse is applied on SYNCP/M, the rising edge of even ADC Clock gets aligned to falling edge of Chip Clock.

Figure 5. Latency



(1) Represents multiplexed bits of a DDR LVDS output pair in 9-bit mode. Dn represents Bits D0,D2,D4…, whereas Dn+1 represents bits D1,D3,D5…

(2) Represents multiplexed bits of a DDR LVDS output pair in 14-bit mode. Dn represents Bits D0,D2,D4…, whereas Dn+1 represents bits D1,D3,D5...

Figure 6. Setup and Hold Timing

DEVICE CONFIGURATION

The ADS58C20/23 has several modes that can be configured using a serial programming interface, as described below. In addition, the device has six dedicated parallel pins for controlling common functions such as power down, decimation filter and SNRBoost^{3G+} control.

The functions controlled by each parallel pin are described in Table pin functions.

DETAILS OF SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 20MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on the RESET pin (of width greater than 10ns), as shown in Figure 7; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D1 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

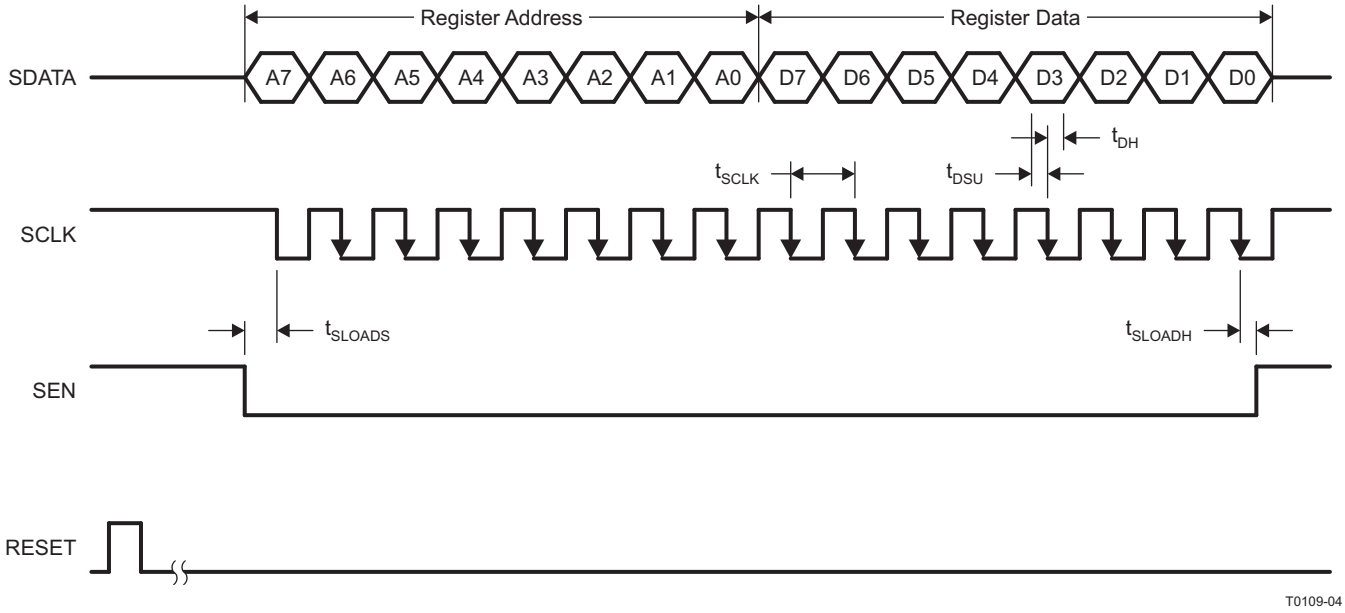


Figure 7. Serial Interface Timing

Table 1. Serial Interface Timing Characteristics(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1/tSCLK)	>DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.9V, AVDD_BUF = 3.3V, and DRVDD = 1.8V, unless otherwise noted.

Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 15).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to '0'.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float.

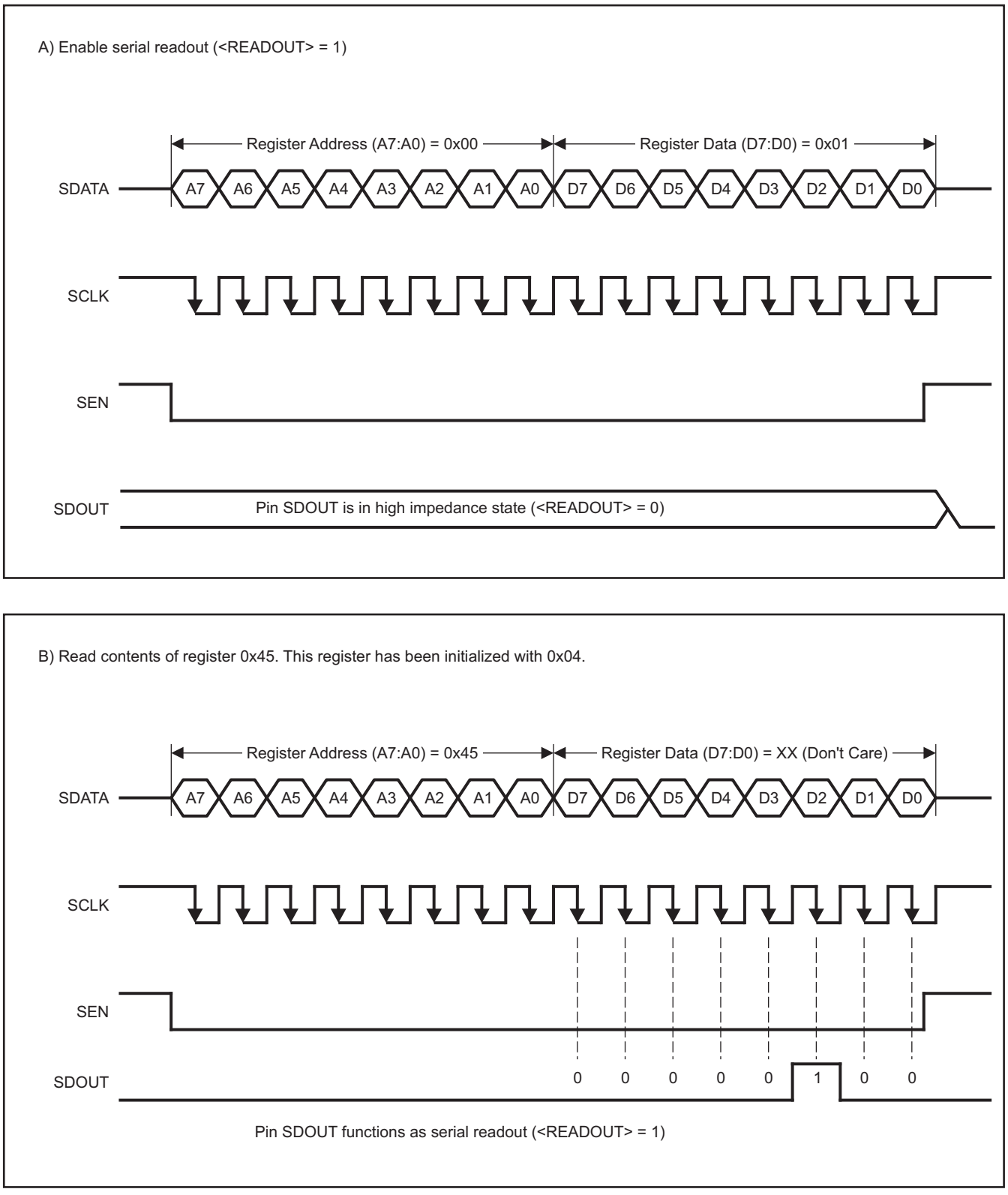
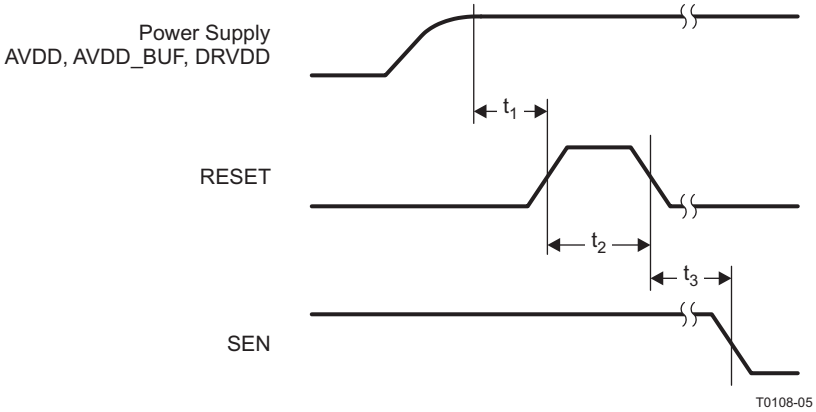


Figure 8. Serial Readout Timing Diagram

Table 2. Reset Timing (only when Serial Interface is Used)(1)

PARAMETER			MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1		20	ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.



Note: A high pulse on the RESET pin is required in the serial interface mode when initialized through a hardware reset.

Figure 9. Reset Timing

SUMMARY OF SERIAL INTERFACE REGISTERS

REGISTER ADDRESS	REGISTER DATA							
A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	<RESET>	<READOUT>
01	<LVDS SWING>						0	0
04	<SPECIAL MODE6>	0	0	0	0	0		
25	<DIG GAIN CH 1, ODD>				<DIS DIG GAIN CH 1, ODD>	<TEST PATTERN CH 1, ODD>		
2B	<DIG GAIN CH 1, EVEN>				<DIS DIG GAIN CH 1, EVEN>	<TEST PATTERN CH 1, EVEN>		
2C	0	<FILT GAIN CH 1 >				<FILT GAIN OVERRIDE CH1>	<SNRB BW PIN OVERRIDE CH1>	<SNRB BW OPTION CH 1>
2D	0	<FILT OPTION CH 1>	<FILT PIN OVERRIDE CH 1>	0	<SEL OVR ORDER CH1>		<DEC FILT ORDER CTRL CH1>	
31	<DIG GAIN CH 2, EVEN>				<DIS DIG GAIN CH 2, EVEN>	<TEST PATTERN CH 2, EVEN>		
32	0	<FILT GAIN CH 2>				<FILT GAIN OVERRIDE CH2>	<SNRB BW PIN OVERRIDE CH2>	<SNRB BW OPTION CH 2>
33	0	<FILT OPTION CH 2>	<FILT PIN OVERRIDE CH 2>	0	<SEL OVR ORDER CH2>		<DEC FILT ORDER CTRL CH2>	
37	<DIG GAIN CH 2, ODD>				<DIS DIG GAIN CH 2, ODD>	<TEST PATTERN CH 2, ODD>		
3D	0	0	<EN OFFSET CORR>	0	0	0	0	0
3F	0	0	<CUSTOM PATTERN D13-D8 >					
40	<CUSTOM PATTERN D7-D0>							
42	0	0	0	0	<DIG GAIN EN COMMON>	0	0	0
44	0	0	0	0	0	<ADC OUT SEL>	<LOW LAT 1>	<LOW LAT 0>
45	<STBY>	0	0	0	0	<PDN GLOBAL>	0	<CONFIG PDN PIN>
BA	0	0	0	0	<SPECIAL MODE3>	0	0	0
BD	<FAST OVR THRESH PROG>							
BE	<EN FAST OVR THRESH>	0	0	0	0	0	0	0
E0	0	<SPECIAL MODE4>		0	0	0	0	0
EA	<SNRB PIN OVERRIDE>	0	0	0	0	0	0	0
EE	<SPECIAL MODE5>	0	0	0	0	0	0	0
F1	0	0	0	0	0	0	<EN LVDS SWING>	

SUMMARY OF SERIAL INTERFACE REGISTERS (continued)

REGISTER ADDRESS	REGISTER DATA							
F3	0	0	0	0	< 14bit MODE>	0	0	0
F7	<SPECIAL MODE1>	<CLKOUT PRG CH1 <8:5> >				0	0	<SPECIAL MODE2>
F8	<CLKOUT PRG CH1 <4:0> >					0	0	0
FA	0	0	0	0	0	0	<DIS SYNC PIN>	0
FD	<CLKOUT PRG CH2 D7-D0>							
FE	0	0	0	0	<PDN CH2>		<PDN CH1>	

DESCRIPTION OF SERIAL INTERFACE REGISTERS

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
00	00	0	0	0	0	0	0	<RESET>	<READOUT>

D1 **<RESET>**

1 Software reset applied – resets all internal registers to their default values and self-clears to 0.

D0 **<READOUT>**

0 Serial readout of registers is disabled. Pin SDOUT is put in high-impedance state.

1 Serial readout is enabled. Pin SDOUT functions as serial data readout with CMOS logic levels, running off DRVDD

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
01	00	<LVDS SWING>						0	0

D7–D2 **<LVDS SWING>** LVDS swing programmability (after setting bit <EN LVDS SWING>)

000000 Default LVDS swing; ±350mV with external 100-Ω termination

011011 ±410mV LVDS swing with external 100-Ω termination

110010 ±480mV LVDS swing with external 100-Ω termination

010100 ±600mV LVDS swing with external 100-Ω termination

001111 ±120mV LVDS swing with external 100-Ω termination

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
04	00	<HIGH SFDR MODE>	0	0	0	0	0	0	0

D7 **<HIGH SFDR MODE>** Helps improve SFDR. After Reset or wake up from powoer down, first set this bit to 1, then clear it to 0.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
25	00	<DIG GAIN CH 1, ODD>				<DIS DIG GAIN CH 1, ODD>	<TEST PATTERN CH 1, ODD>		

D2–D0 **< TEST PATTERN CH 1, ODD >** Test Patterns of ODD ADC of channel 1 come out (**only after** filter is *bypassed* by setting bit **<LOW LAT 1>** to high)

000 Default

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern

In 9-bit mode, outputs data <D8:D0> is an alternating sequence of 101010101 and 010101010
In 14-bit mode, outputs data <D13:D0> is an alternating sequence of 01010101010101 and 10101010101010

100 Outputs digital ramp

In 9-bit mode, output data increments by one 9-bit LSB every 32th clock cycle from code 0 to code 511.
In 14-bit mode, output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383.

101 Outputs custom pattern

Program a pattern in 9-bit mode using <CUSTOM PATTERN D13-D5 > bits of register 0x3F and register 0x40
Program a pattern in 14-bit mode using <CUSTOM PATTERN D13-D0 > bits of register 0x3F and register 0x40

D3 **<DIS DIG GAIN CH 1, ODD>** Digital Gain disabled for ODD ADC of channel 1

0 Digital gain is enabled

1 Digital gain gets disabled

D7-D4 **<DIG GAIN CH 1, ODD>** Digital gain control bits for ODD ADC of channel 1 (only after <DIG GAIN EN COMMON> bit is set)

0000 0 dB

0001 0.5 dB

0010 1.0 dB

0011 1.5 dB

0100 2.0 dB

0101 2.5 dB

0110 3.0 dB

0100 3.5 dB

1000 4.0 dB

1001 4.5 dB

1010 5.0 dB

1011 5.5 dB

1100 6.0 dB

Other combinations - do not use

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
2B	00	<DIG GAIN CH 1, EVEN>				<DIS DIG GAIN CH 1, EVEN>	<TEST PATTERN CH 1, EVEN>		

D2–D0 **< TEST PATTERN CH 1, EVEN >** Test Patterns of EVEN ADC of channel 1 come out (**only after** filter is *bypassed* by setting bit **<LOW LAT 1>** and EVEN ADC is selected by setting bit **<ADC OUT SEL>**)

000 Default

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern

In 9-bit mode, outputs data <D8:D0> is an alternating sequence of 101010101 and 010101010
In 14-bit mode, outputs data <D13:D0> is an alternating sequence of 01010101010101 and 10101010101010

100 Outputs digital ramp

In 9-bit mode, output data increments by one 9-bit LSB every 32th clock cycle from code 0 to code 511.
In 14-bit mode, output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383.

101 Outputs custom pattern

Program a pattern in 9-bit mode using <CUSTOM PATTERN D13-D5 > bits of register 0x3F and register 0x40
Program a pattern in 14-bit mode using <CUSTOM PATTERN D13-D0 > bits of register 0x3F and register 0x40

D3 **<DIS DIG GAIN CH 1, EVEN>** Digital Gain disabled for EVEN ADC of channel 1

0 Digital gain is enabled

1 Digital gain gets disabled

D7-D4 **<DIG GAIN CH 1, EVEN>** Digital gain control bits for EVEN ADC of channel 1 (only after <DIG GAIN EN COMMON> bit is set)

0000 0 dB

0001 0.5 dB

0010 1.0 dB

0011 1.5 dB

0100 2.0 dB

0101 2.5 dB

0110 3.0 dB

0100 3.5 dB

1000 4.0 dB

1001 4.5 dB

1010 5.0 dB

1011 5.5 dB

1100 6.0 dB

Other combinations - do not use

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
2C	00	0	<FILT GAIN CH 1 >				<FILT GAIN OVERRIDE CH 1>	<SNRB BW PIN OVERRIDE CH 1>	<SNRB BW OPTION CH 1>

D0 **<SNRB BW OPTION CH 1>**

0 Default, 40 MHz bandwidth selected for SNRBoost^{3G+} on channel 1

1 75 MHz bandwidth selected for SNRBoost^{3G+} on channel 1

D1 **<SNRB BW PIN OVERRIDE CH 1>**

0 Default, SNR_BW pin controls SNRBoost^{3G+} bandwidth for channel 1

1 SNRBoost^{3G+} bandwidth is controlled by bit **<SNRB BW OPTION CH 1>** for channel 1

D2 **<FILT GAIN OVERRIDE CH 1>**

0 Default

1 Override default filter gain setting for channel 1

D6-D3 **<FILT GAIN CH 1>** Filter gain control bits for channel 1 (only after bit <FILT GAIN OVERRIDE CH 1> is set)

0000 -3.1dB Gain

0001 -2.1dB Gain

0010 -1.5dB Gain

0011 -1.0dB Gain

0100 -0.5dB Gain

0101 0dB Gain

0110 0.5dB Gain

0111 1.0dB Gain

1000 1.5dB Gain

1001 2.0dB Gain

1010 3.0dB Gain

other combinations - do not use

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
2D	00	0	<FILT OPTION CH 1>	<FILT PIN OVERRIDE CH 1>	0	<SEL OVR ORDER CH1>		<DEC FILT ORDER CTRL CH1>	

D1-D0 **<DEC FILT ORDER CTRL CH1>**Decimation Filter Order Control for CH 1

00,01 Pin DEC_FILT_MODE controls order of decimation filter

10 Low-latency decimation filter (12th order) is selected

11 High-latency decimation filter (20th order) is selected

D3-D2 **<SEL OVR ORDER CH1>**The device outputs OVR signal for channel 1 on the CH1_OVRP/M pins. Using these register bits, the user can select the order & type of OVR on the CH1_OVR pins

	Output clock falling edge (CH1_CLKOUT)	Output clock rising edge (CH1_CLKOUT)
00	CH1 FAST OVR	CH1 Normal OVR
01	CH1 FAST OVR	CH1 FAST OVR
10	CH1 Normal OVR	CH1 Normal OVR

11 CH1 Normal OVR CH1 FAST OVR

D5 **<FILT PIN OVERRIDE CH 1>**

0 Default, Pin DEC_LP controls Low-Pass or High-Pass filter option

1 Override pin control to choose Low-Pass or High-Pass filter option for channel 1

D6 **FILT OPTION CH 1>** select Low-Pass or High-Pass option for decimation filter of channel 1 (only after bit <FILT PIN OVERRIDE CH 1> is set)

0 Default HIGH PASS FILTER selected for channel 1

1 LOW PASS FILTER selected for channel 1

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
31	00	<DIG GAIN CH 2, EVEN>				<DIS DIG GAIN CH 2, EVEN>	<TEST PATTERN CH 2, EVEN>		

D2–D0 < **TEST PATTERN CH 2, EVEN** > Test Patterns of EVEN ADC of channel 2 come out (**only after** filter is *bypassed* by setting bit **<LOW LAT 1>** and EVEN ADC is selected by setting bit **<ADC OUT SEL>**)

000 Default

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern

In 9-bit mode, outputs data <D8:D0> is an alternating sequence of 101010101 and 010101010
In 14-bit mode, outputs data <D13:D0> is an alternating sequence of 01010101010101 and 10101010101010

100 Outputs digital ramp

In 9-bit mode, output data increments by one 9-bit LSB every 32th clock cycle from code 0 to code 511. In 14-bit mode, output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383.

101 Outputs custom pattern

Program a pattern in 9-bit mode using <CUSTOM PATTERN D13-D5 > bits of register 0x3F and register 0x40
Program a pattern in 14-bit mode using <CUSTOM PATTERN D13-D0 > bits of register 0x3F and register 0x40

D3 **<DIS DIG GAIN CH 2, EVEN>** Digital Gain disabled for EVEN ADC of channel 2

0 Digital gain is disabled

1 Digital gain gets enabled

D7-D4 **<DIG GAIN CH 2, EVEN>** Digital gain control bits for EVEN ADC of channel 2 (only after <DIG GAIN EN COMMON> bit is set)

0000 0 dB

0001 0.5 dB

0010 1.0 dB

0011 1.5 dB

0100 2.0 dB

0101 2.5 dB
0110 3.0 dB
0100 3.5 dB
1000 4.0 dB
1001 4.5 dB
1010 5.0 dB
1011 5.5 dB
1100 6.0 dB
other combinations - do not use

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
32	00	0	<FILT GAIN CH 2 >				<FILT GAIN OVERRIDE CH2>	<SNRB BW PIN OVERRIDE CH 2>	<SNRB BW OPTION CH 2>

D0 <SNRB BW OPTION CH 2>
0 Default, 40 MHz bandwidth selected for SNRBoost^{3G+} on channel 2
1 75 MHz bandwidth selected for SNRBoost^{3G+} on channel 2

D1 <SNRB BW PIN OVERRIDE CH 2>
0 Default, SNR_BW pin controls SNRBoost^{3G+} bandwidth for channel 2
1 SNRBoost^{3G+} bandwidth is controlled by bit **<SNRB BW OPTION CH 2>** for channel 2

D2 <FILT GAIN OVERRIDE CH 2>
0 Default
1 Override default filter gain setting for channel 2

D6-D3 **<FILT GAIN CH2>** Filter gain control bits for channel 2 (only after bit <FILT GAIN OVERRIDE CH 2> is set)
0000 -3.1dB Gain
0001 -2.1dB Gain
0010 -1.5dB Gain
0011 -1.0dB Gain
0100 -0.5dB Gain
0101 0 dB Gain
0110 0.5dB Gain
0111 1.0dB Gain
1000 1.5dB Gain
1001 2.0dB Gain
1010 3.0dB Gain
other combinations - do not use

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
33	00	0	<FILT OPTION CH 2>	<FILT PIN OVERRIDE CH 2>	0	<SEL OVR ORDER CH2>		<DEC FILT ORDER CTRL CH2>	

D1-D0 **<DEC FILT ORDER CTRL CH2>** Decimation Filter Order Control for CH 2

00,01 Pin DEC_FILT_MODE controls order of decimation filter

10 Low-latency decimation filter (12th order) is selected

11 High-latency decimation filter (20th order) is selected

D3-D2 **<SEL OVR ORDER CH2>** The device outputs OVR signal for channel 2 on the CH2_OVRP/M pins. Using these register bits, the user can select the order & type of OVR on the CH2_OVR pins

	Output clock falling edge (CH2_CLKOUT)	Output clock rising edge (CH2_CLKOUT)
00	CH2 FAST OVR	CH2 Normal OVR
01	CH2 FAST OVR	CH2 FAST OVR
10	CH2 Normal OVR	CH2 Normal OVR
11	CH2 Normal OVR	CH2 FAST OVR

D5 **<FILT PIN OVERRIDE CH 2>**

0 Default, Pin DEC_LP controls Low-Pass or High-Pass filter option

1 Override pin control to choose Low-Pass or High-Pass filter option for channel 2

D6 **<FILT OPTION CH 2>** select Low-Pass or High-Pass option for decimation filter of channel 2 (only after bit <FILT PIN OVERRIDE CH 2> is set)

0 Default HIGH PASS FILTER selected for channel 2

1 LOW PASS FILTER selected for channel 2

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
37	00	<DIG GAIN CH 2, ODD>				<DIS DIG GAIN CH 2, ODD>	<TEST PATTERN CH 2, ODD>		

D2–D0 < **TEST PATTERN CH 2, ODD** > Test patterns of ODD ADC of channel 2 come out (**only after** filter is *bypassed* by setting bit **<LOW LAT 1>** to high)

000 Default

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern

In 9-bit mode, outputs data <D8:D0> is an alternating sequence of 101010101 and 010101010
In 14-bit mode, outputs data <D13:D0> is an alternating sequence of 01010101010101 and 10101010101010

100 Outputs digital ramp

In 9-bit mode, output data increments by one 9-bit LSB every 32th clock cycle from code 0 to code 511. In 14-bit mode, output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383.

101	Outputs custom pattern Program a pattern in 9-bit mode using <CUSTOM PATTERN D13-D5 > bits of register 0x3F and register 0x40 Program a pattern in 14-bit mode using <CUSTOM PATTERN D13-D0 > bits of register 0x3F and register 0x40

D3 **<DIS DIG GAIN CH 2, ODD>** Digital gain disabled for ODD ADC of channel 2

0	Digital gain is enabled
1	Digital gain gets disabled

D7-D4 **<DIG GAIN CH 2, ODD>** Digital gain control bits for ODD ADC of channel 2 (only after <DIG GAIN EN COMMON> bit is set)

0000	0 dB
0001	0.5 dB
0010	1.0 dB
0011	1.5 dB
0100	2.0 dB
0101	2.5 dB
0110	3.0 dB
0100	3.5 dB
1000	4.0 dB
1001	4.5 dB
1010	5.0 dB
1011	5.5 dB
1100	6.0 dB
	other combinations - do not use

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
3D	00	0	0	<EN OFFSET CORR>	0	0	0	0	0

D5 **<EN OFFSET CORR>** enable offset correction for both channels (only after bit <DIG GAIN EN COMMON> is set)

0	Offset correction is disabled
1	Offset correction is enabled for both channels.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
3F	00	0	0	<CUSTOM PATTERN D13-D8 >					

D5–D0 **<CUSTOM PATTERN D13-D8>**

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
40	00	<CUSTOM PATTERN D7-D0 >							

D7–D0 <CUSTOM PATTERN D7-D0>

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
42	00	0	0	0	0	<DIG GAIN EN COMMON>	0	0	0

D3 **<DIG GAIN EN COMMON>** Enables digital gain control for all ADCs. After this bit is enabled, digital gain can be disabled for individual ADC by bits <DIS DIG GAIN CH1, EVEN>, <DIS DIG GAIN CH1, ODD>, <DIS DIG GAIN CH2, EVEN>, <DIS DIG GAIN CH2, ODD>.

0 Digital gain is disabled for all ADCs

1 Digital gain gets enabled for all ADCs.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
44	00	0	0	0	0	0	<ADC OUT SEL >	<LOW LAT 1>	<LOW LAT 0>

D0 <LOW LAT 0>

0 Default

1 Bypass SNRBoost^{3G+} block after <SNRB PIN OVERRIDE> is set to '1'

D1 <LOW LAT 1>

0 Default

1 By-pass Decimation Filter

D2 < **ADC OUT SEL** > select ADC output for digital test patterns

0 Output of ODD ADC comes out on output data lines.

1 Output of EVEN ADC comes out on output data lines.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
45	00	<STBY>	0	0	0	0	<PDN GLOBAL>	0	<CONFIG PDN PIN>

D0 <CONFIG PDN PIN>

0 PDN pin functions as STBY control pin.

1 PDN pin functions as global power down control pin.

D2 <PDN GLOBAL>

0 Normal operation

1 Total power down – All channel ADCs, internal references and output buffers are powered down. Wake-up time from this mode is slow.

D7 <STBY>

0 Normal operation

1 Both channels are put in standby. Wake-up time from this mode is fast.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
BA	00	0	0	0	0	<SPECIAL MODE3>>	0	0	0

D3 <SPECIAL MODE3>>

0 Do Not Use

1 This bit must be set to 1 always (recommended for best performance)

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
BD	00	<FAST OVR THRESH PROG>							

D7-D0 **<FAST OVR THRESH PROG>**The device has a Fast OVR mode that indicates overload condition at the ADC input. The input voltage level at which the overload is detected is called the threshold & is programmable using these bits. The FAST OVR is triggered 7 output clock cycles after the overload condition occurs. To enable the FAST OVR programmability, enable the register bit<EN FAST OVR THRESH>. Threshold at which FAST OVR is triggered = 1.9V x [decimal value of FAST OVR THRESH PROG>]/255. After reset, the default value of <FAST OVR THRESH PROG> is 180 (decimal).

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
BE	00	<EN FAST OVR THRESH>	0	0	0	0	0	0	0

D7 <EN FAST OVR THRESH>

0 FAST OVR threshold programmability disabled

1 FAST OVR threshold programmability enabled

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
E0	00	0	<SPECIAL MODE4>		0	0	0	0	0

D6-D5 <SPECIAL MODE4>

00,01,10 Do Not Use

11 These bits must be set to 11 always (recommended for best performance)

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
EA	00	<SNRB PIN OVERRIDE>	0	0	0	0	0	0	0

D7 <SNRB PIN OVERRIDE>

0 SNRBoost^{3G+} is controlled by pins. Pin SNRB_EN enables it and pin SNRB_BW controls its bandwidth.

1 SNRBoost^{3G+} is controlled by serial interface registers

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
EE	00	<SPECIAL MODE5>	0	0	0	0	0	0	0

D7 <SPECIAL MODE5>

0 Do Not Use

1 This bit must be set to 1 always (recommended for best performance)

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
F1	00	0	0	0	0	0	0	<EN LVDS SWING>	

D1-D0 <EN LVDS SWING> Enables LVDS swing control by <LVDS SWING> bits

00 LVDS swing control is disabled.

01, 10 Do not use

11 LVDS swing control is enabled.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
F3	00	0	0	0	0	<14bit MODE>	0	0	0

D3 <14 bit MODE>

0 14-bit mode is disabled. Device is in 9-bit mode.

1 14-bit mode is enabled.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
F7	00	<SPECIAL MODE1>	<CLKOUT PRG CH1 <8:5> >				0	0	<SPECIAL MODE1>
F8	00	<CLKOUT PRG CH1 <4:0> >					0	0	0

<CLKOUT PRG CH1> Bits CLKOUT PRG CH1 control output clock position for channel 1 as described below

Clock position control	CLKOUT PRG CH1<8:5>	CLKOUT PRG CH1<4:0>
default position	0000	00000
Output clock advances by 250ps	0001	10001
Output clock advances by 100ps	0010	10010
Output clock advances by 850ps	0011	10011
Output clock advances by 1.1ns	0111	10111
Output clock advances by 1.4ns	1011	11011
Output clock advances by 1.8ns	1111	11111

D7 <SPECIAL MODE1>

0 Do Not Use

1 This bit must be set to 1 always (recommended for best performance)

D0 <SPECIAL MODE2>

0 Do Not Use

1 This bit must be set to 1 always (recommended for best performance)

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
FA	00	0	0	0	0	0	<DIS SYNC PIN>	0	0

D3 <DIS SYNC PIN>

0 SYNCP/M pin is enabled and can be used for synchronizing multiple chips.

1 SYNCP/M pin is disabled.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
FD	00	CLKOUT PRG CH 2							

D7-D0 <CLKOUT PRG CH 2> Control output clock shift for channel 2. Amount of shift in output clock of channel 2 is given below.

00000000 default position

00010001 output clock advances by 250ps

00100010 output clock advances by 100ps

00110011 output clock advances by 850ps

01110111 output clock advances by 1.1ns

10111011 output clock advances by 1.4ns

11111111 output clock advances by 1.8ns

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
FE	00	0	0	0	0	<PDN CH 2>		<PDN CH 1>	

D1-D0 <PDN CH 1>

00 Default after reset, normal operation

01 CH 1 ODD ADC is powered down, must be used when decimation filter is bypassed in 14-bit mode

10 CH 1 EVEN ADC is powered down

11 Power down EVEN & ODD ADC of CH1

D3-D2 <PDN CH 2>

00 Default after reset, normal operation

10 CH 2 ODD ADC is powered down, must be used when decimation filter is bypassed in 14-bit mode

10 CH 2 EVEN ADC is powered down

11 Power down EVEN & ODD ADC of CH2

TYPICAL CHARACTERISTICS

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT IN 9-BIT MODE, INPUT FREQUENCY = 185MHZ, HIGH-PASS DECIMATION FILTER ON

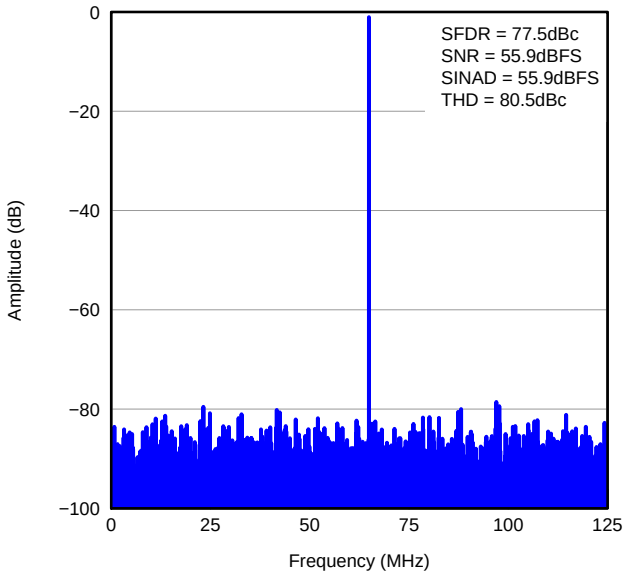


Figure 10.

FFT IN 9-BIT MODE, INPUT FREQUENCY = 185MHZ, WITH SNRBoost^{3G+} SELECTED FOR 75MHZ BW AND HIGH-PASS DECIMATION FILTER ON

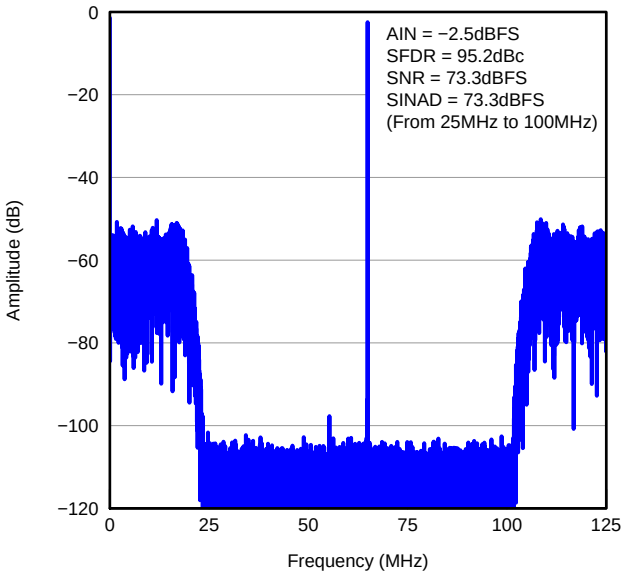


Figure 11.

FFT IN 9-BIT MODE, INPUT FREQUENCY = 185MHZ, WITH SNRBoost^{3G+} SELECTED FOR 40MHZ BW AND HIGH-PASS DECIMATION FILTER ON

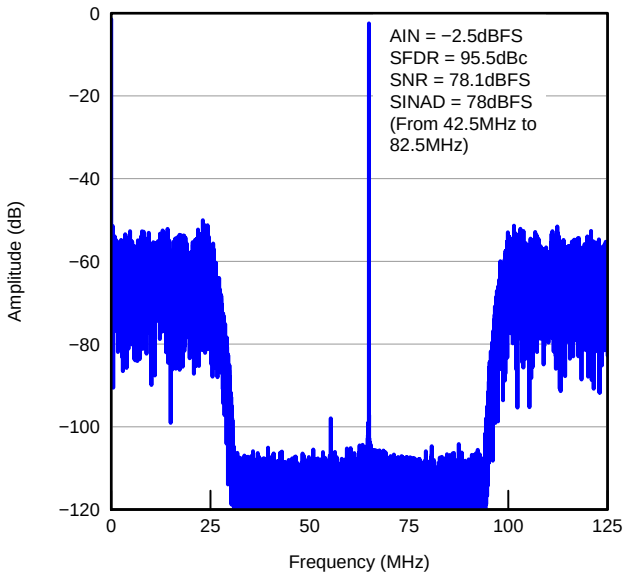


Figure 12.

FFT IN 9-BIT MODE, INPUT FREQUENCY = 60MHZ, LOW-PASS DECIMATION FILTER ON

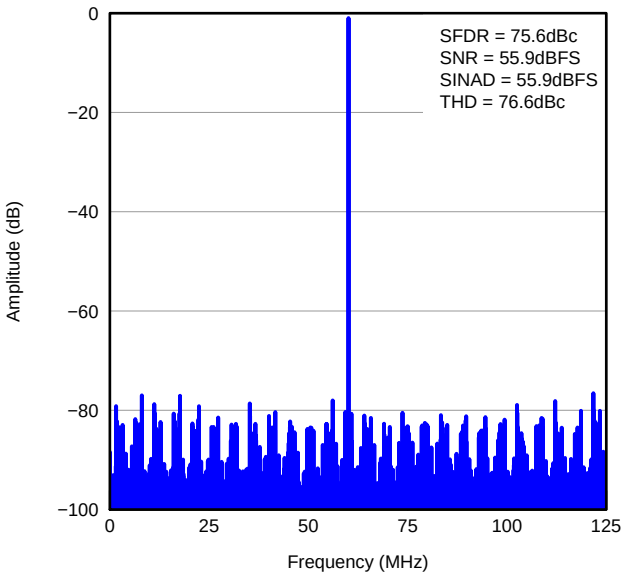


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT IN 9-BIT MODE, INPUT FREQUENCY = 60MHZ, WITH SNRBoost^{3G+} SELECTED FOR 75MHZ BW AND LOW-PASS DECIMATION FILTER ON

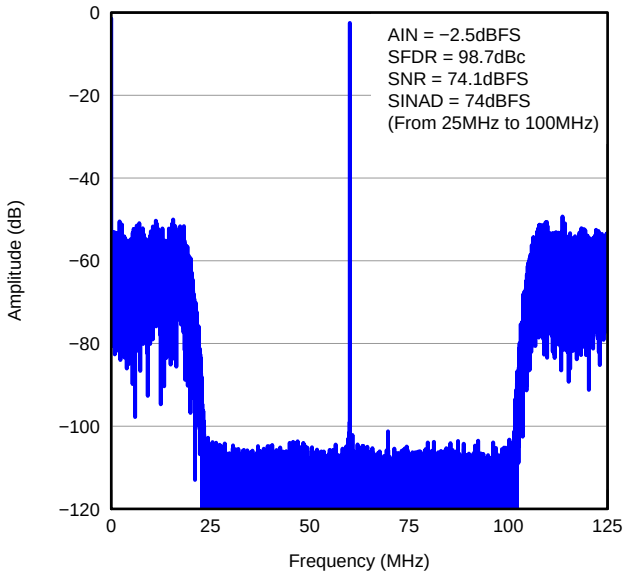


Figure 14.

FFT IN 9-BIT MODE, INPUT FREQUENCY = 60MHZ, WITH SNRBoost^{3G+} SELECTED FOR 40MHZ BW AND LOW-PASS DECIMATION FILTER ON

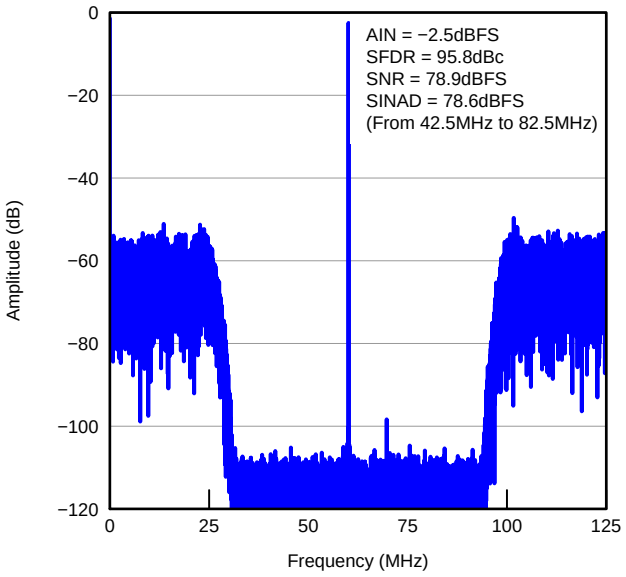


Figure 15.

FFT IN 14-BIT MODE, INPUT FREQUENCY = 185MHZ, HIGH-PASS DECIMATION FILTER ON

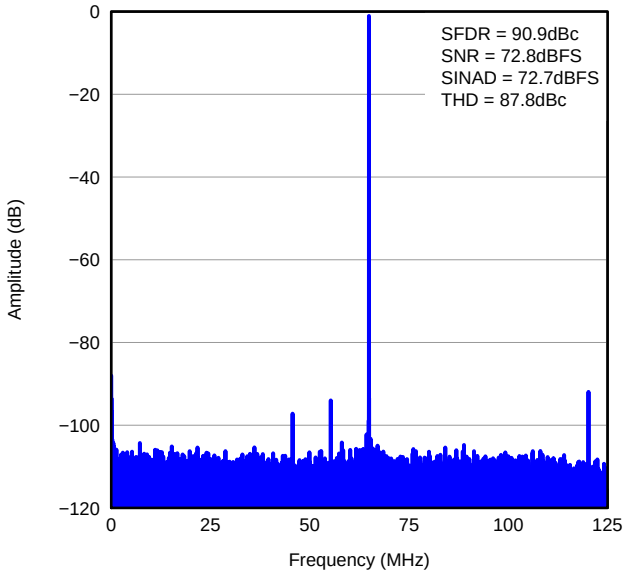


Figure 16.

FFT IN 14-BIT MODE, INPUT FREQUENCY = 60MHZ, LOW-PASS DECIMATION FILTER ON

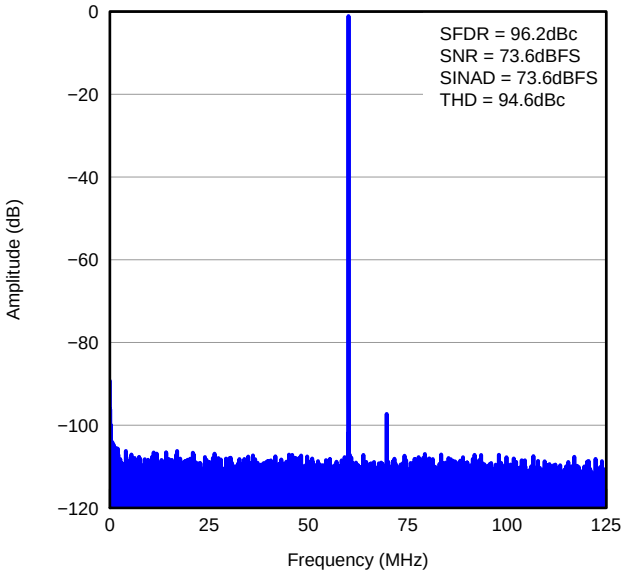


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT IN 14-BIT MODE, INPUT FREQUENCY = 185MHZ, DECIMATION FILTER OFF

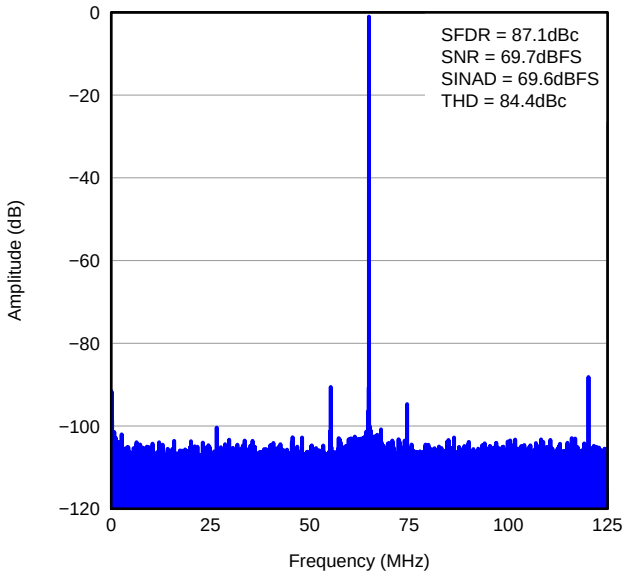


Figure 18.

FFT FOR 2-TONE INPUT SIGNAL IN 14-BIT MODE, DECIMATION FILTER ON

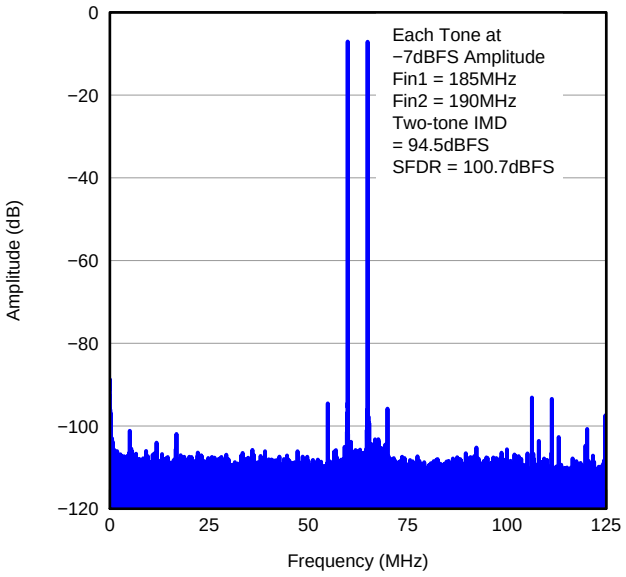


Figure 19.

FFT FOR 2-TONE INPUT SIGNAL IN 14-BIT MODE, DECIMATION FILTER OFF

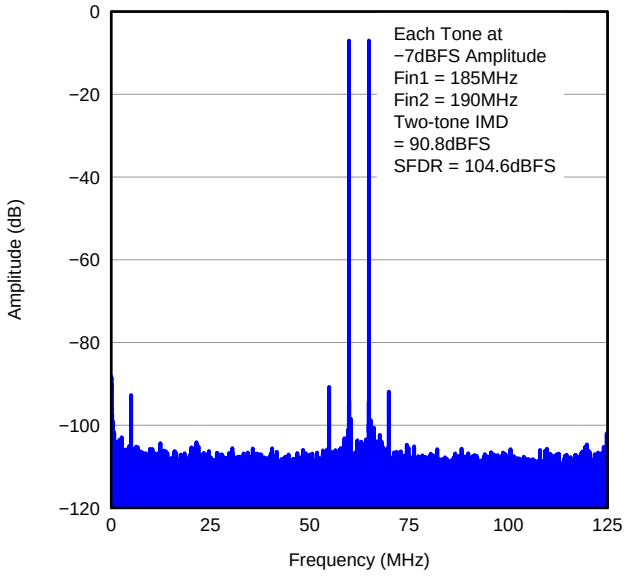


Figure 20.

SFDR vs INPUT FREQUENCY, DECIMATION FILTER ON

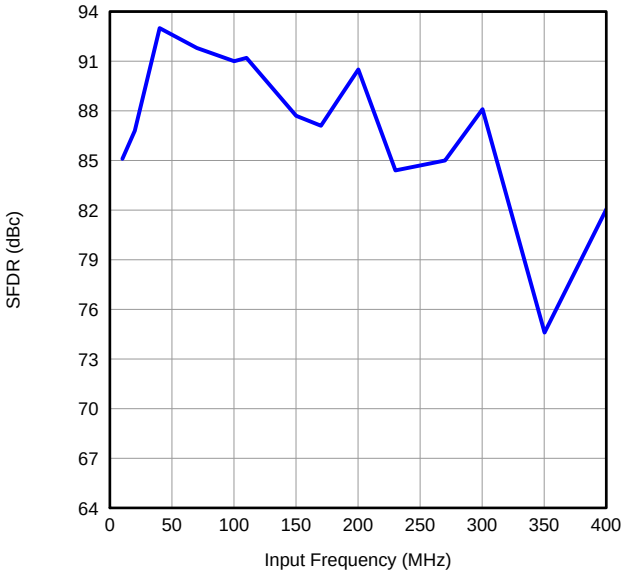


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SFDR vs INPUT FREQUENCY, DECIMATION FILTER OFF

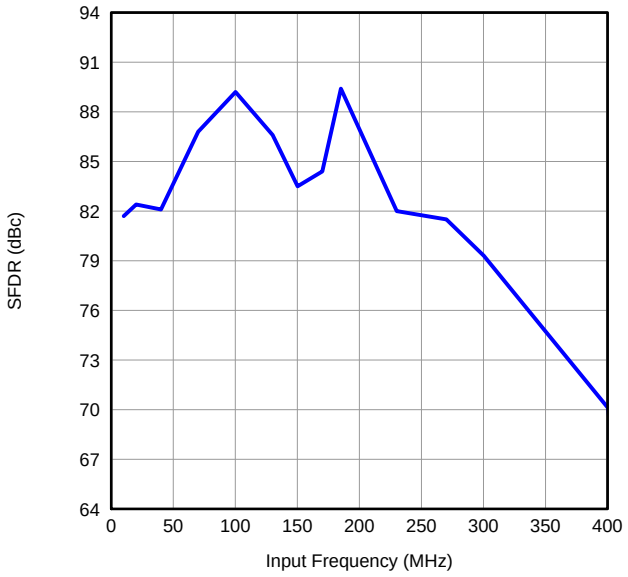


Figure 22.

SNR vs INPUT FREQUENCY, DECIMATION FILTER ON

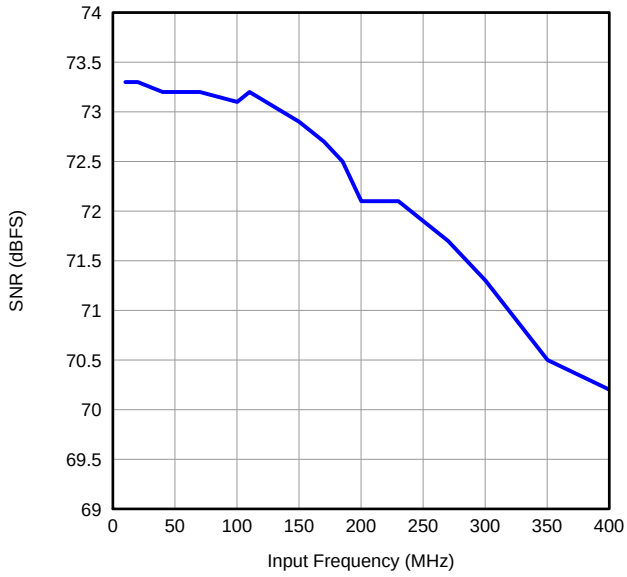


Figure 23.

SNR vs INPUT FREQUENCY, DECIMATION FILTER OFF

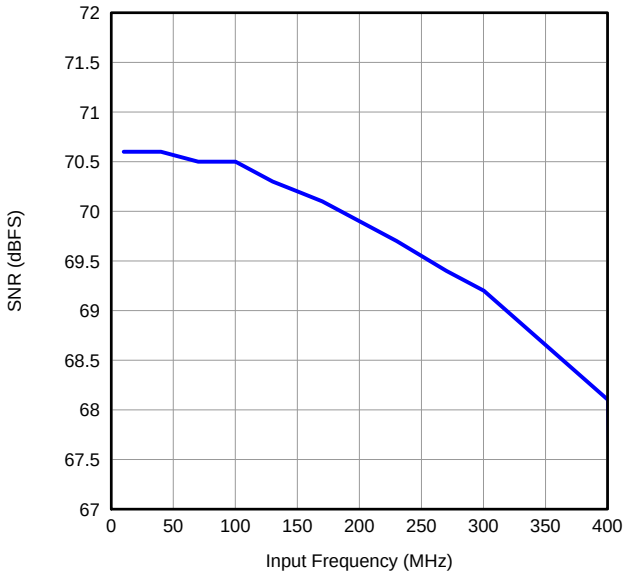


Figure 24.

VARIATION OF IN-BAND SNR WITH SNRBoost^{3G+} AND DECIMATION FILTER ON

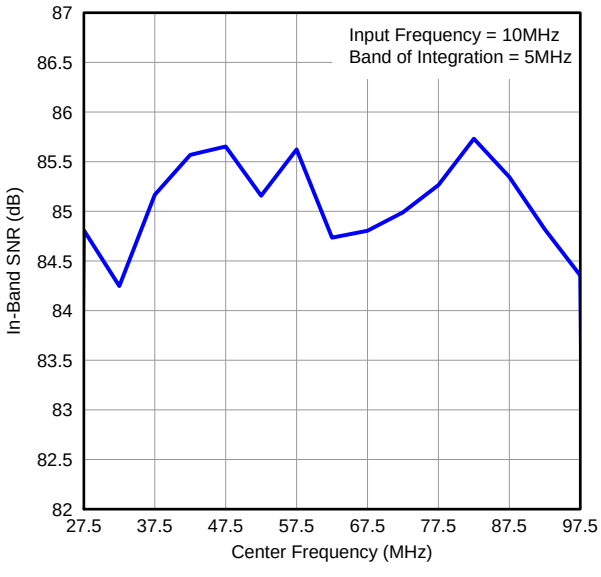


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SFDR vs GAIN ACROSS INPUT FREQUENCY, DECIMATION FILTER ON

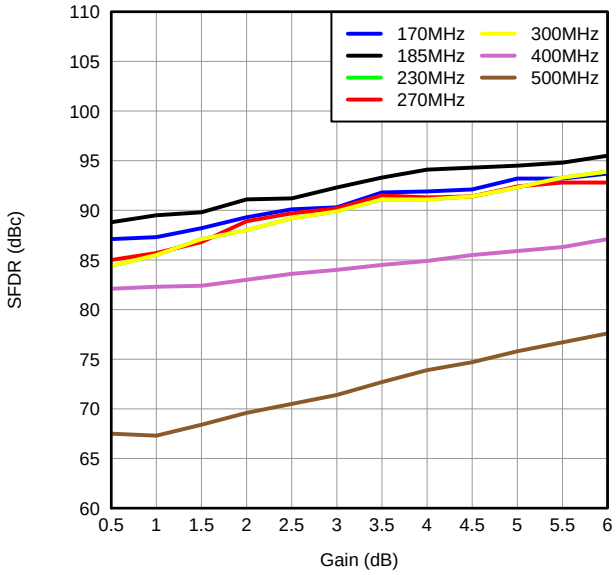


Figure 26.

SFDR vs GAIN ACROSS INPUT FREQUENCY, DECIMATION FILTER OFF

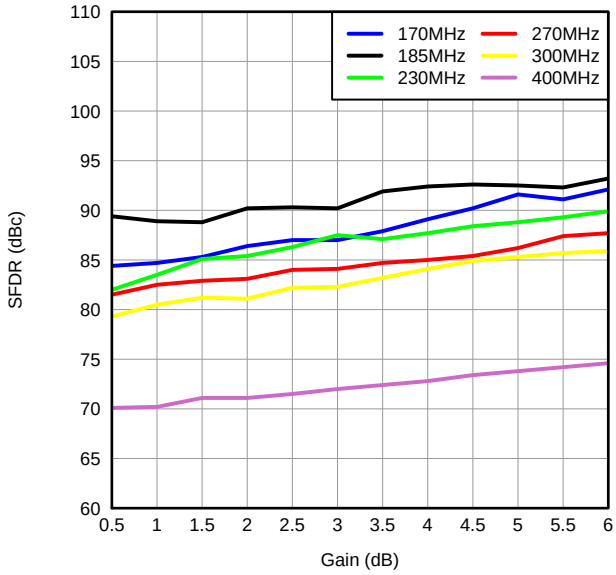


Figure 27.

SINAD vs GAIN ACROSS INPUT FREQUENCY, DECIMATION FILTER ON

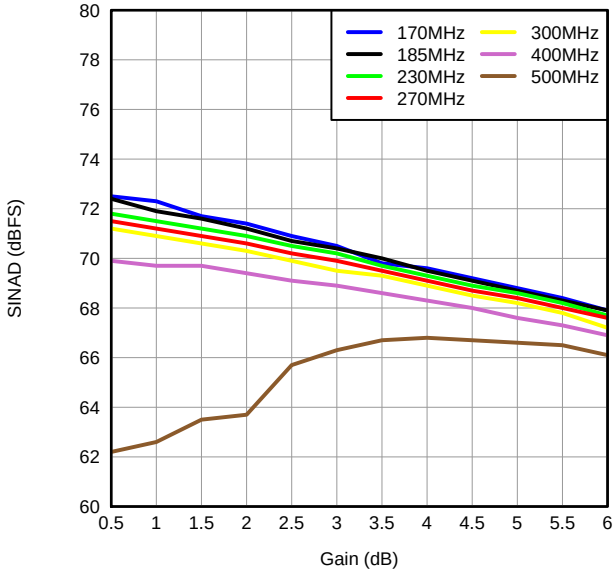


Figure 28.

SINAD vs GAIN ACROSS INPUT FREQUENCY, DECIMATION FILTER OFF

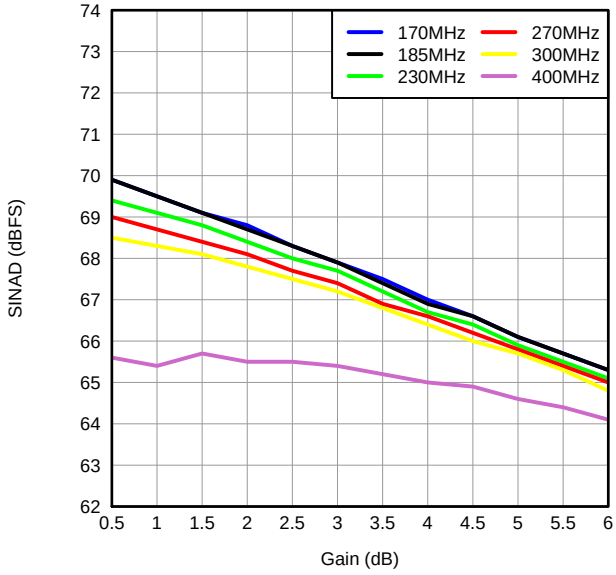


Figure 29.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

PERFORMANCE vs INPUT AMPLITUDE, DECIMATION FILTER ON

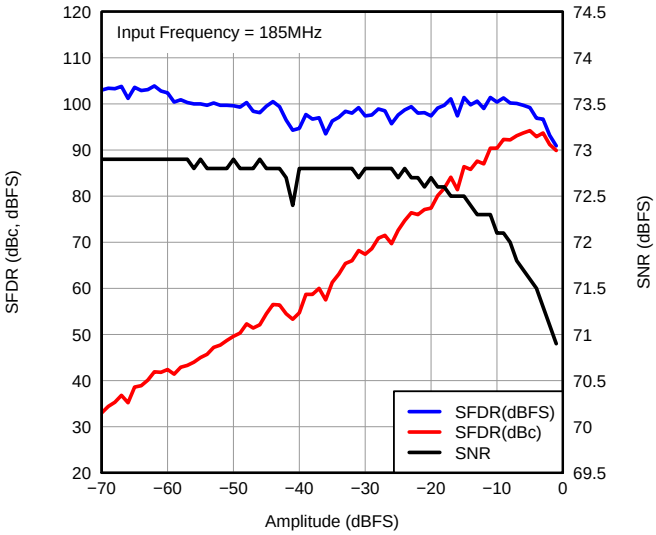


Figure 30.

PERFORMANCE vs INPUT AMPLITUDE, DECIMATION FILTER OFF

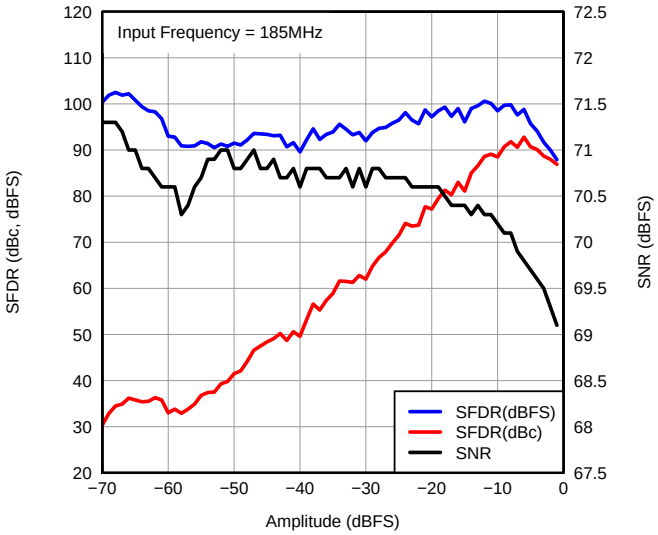


Figure 31.

PERFORMANCE vs INPUT AMPLITUDE WITH SNRBoost^{3G+} ON, DECIMATION FILTER ON

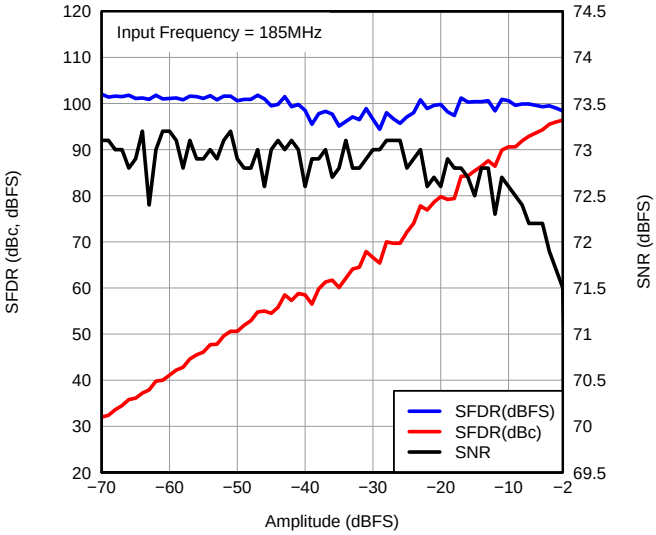


Figure 32.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE, DECIMATION FILTER OFF

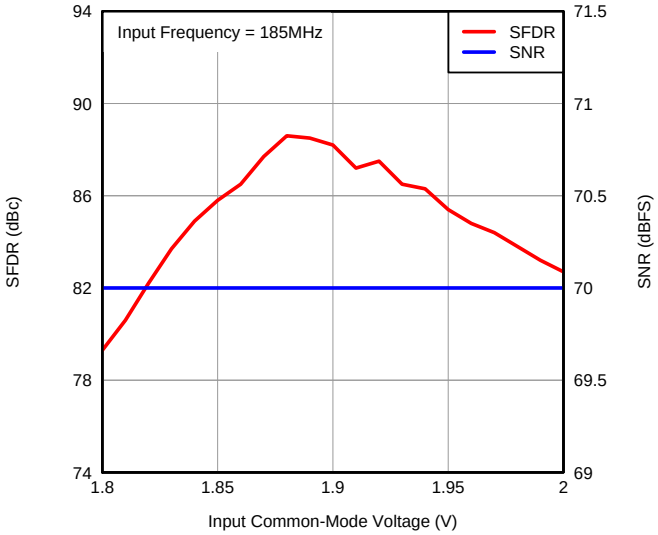


Figure 33.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SFDR vs TEMPERATURE ACROSS AVDD SUPPLY, DECIMATION FILTER ON

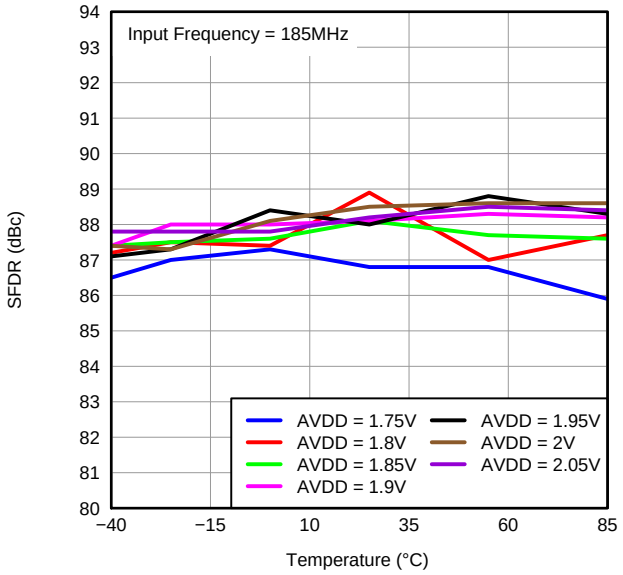


Figure 34.

SNR vs TEMPERATURE ACROSS AVDD SUPPLY, DECIMATION FILTER ON

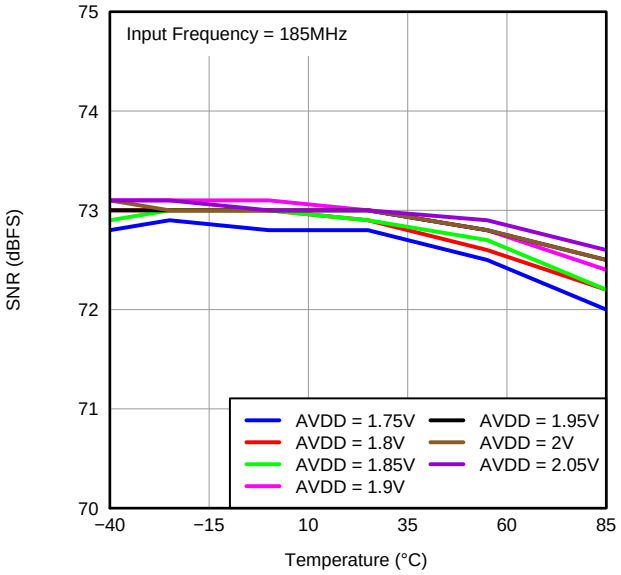


Figure 35.

SFDR vs TEMPERATURE ACROSS AVDD SUPPLY, DECIMATION FILTER OFF

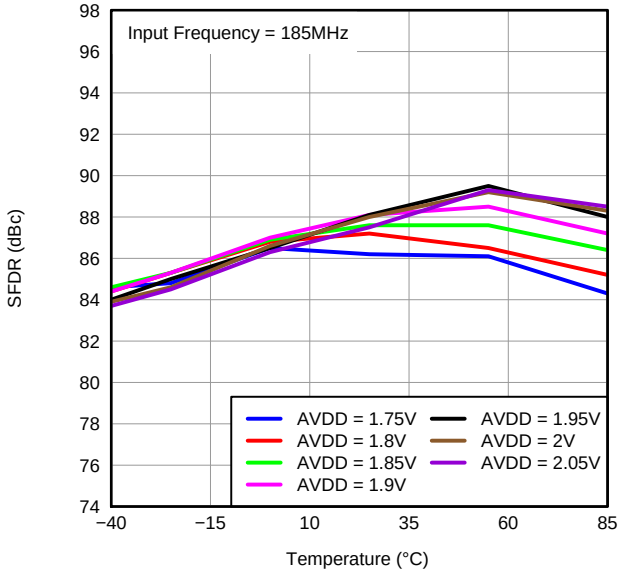


Figure 36.

SNR vs TEMPERATURE ACROSS AVDD SUPPLY, DECIMATION FILTER OFF

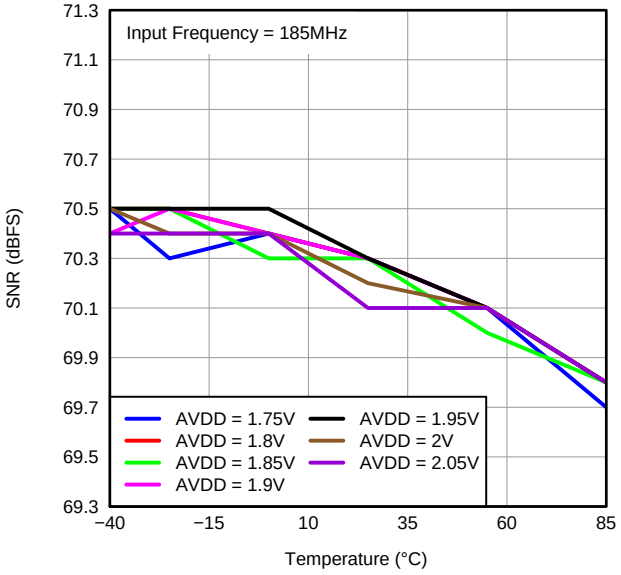


Figure 37.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

PERFORMANCE vs DRVDD SUPPLY VOLTAGE, DECIMATION FILTER ON

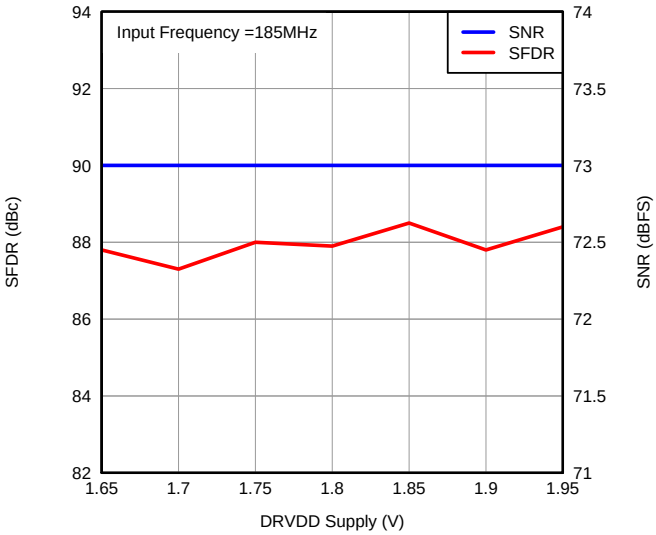


Figure 38.

PERFORMANCE vs DRVDD SUPPLY VOLTAGE, DECIMATION FILTER OFF

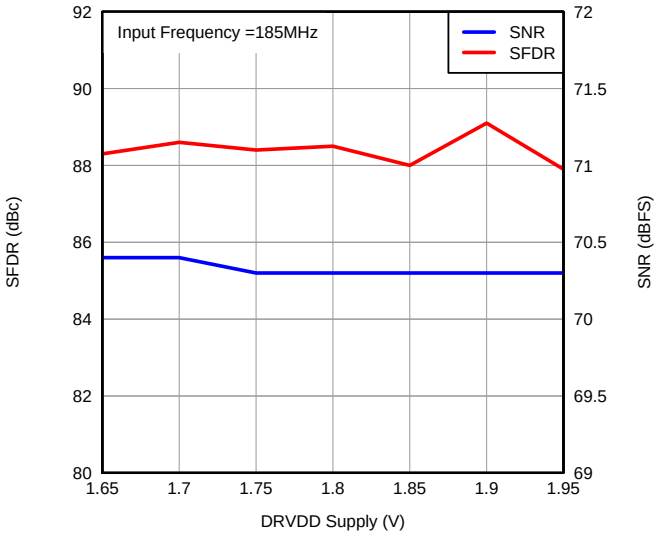


Figure 39.

PERFORMANCE vs BUFFER SUPPLY VOLTAGE, DECIMATION FILTER ON

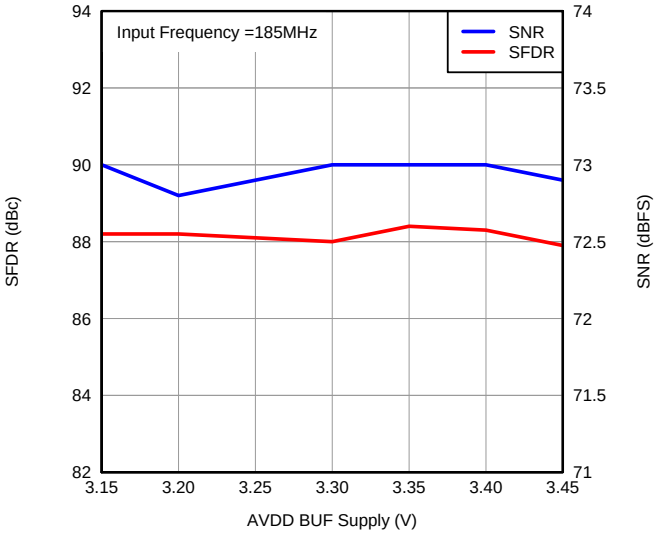


Figure 40.

PERFORMANCE vs BUFFER SUPPLY VOLTAGE, DECIMATION FILTER OFF

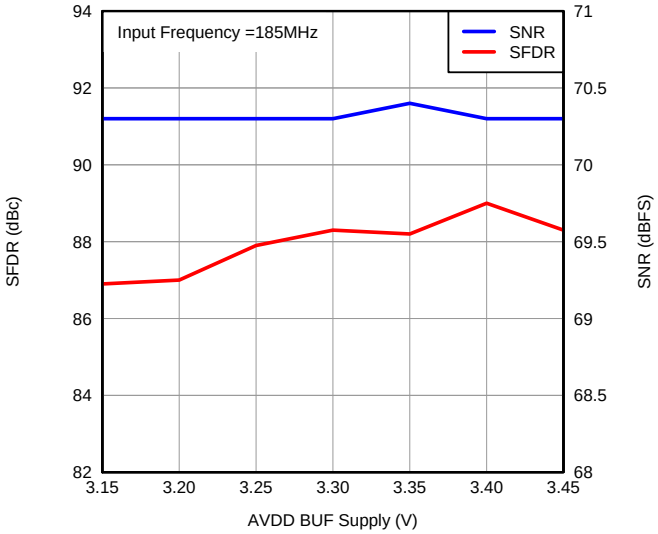


Figure 41.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

PERFORMANCE vs DIFFERENTIAL CLOCK AMPLITUDE

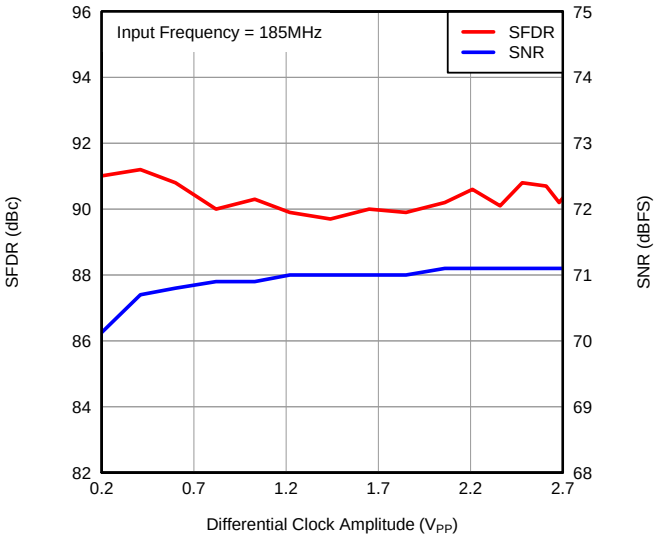


Figure 42.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

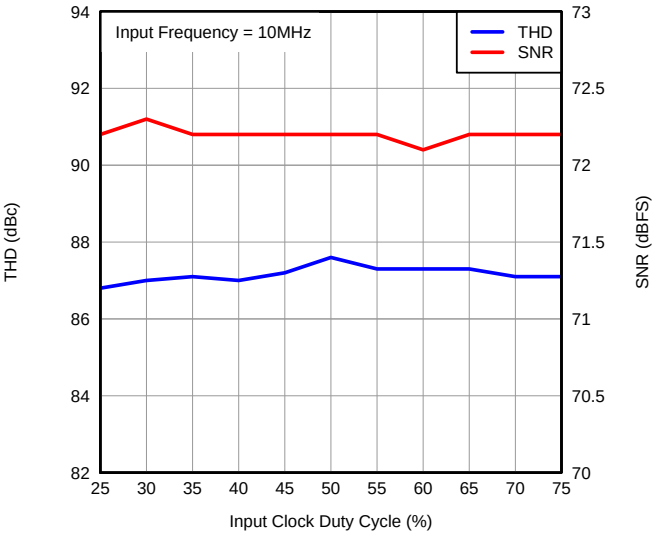


Figure 43.

TIME DOMAIN DATA WITH SNRBoost^{3G+} ENABLED

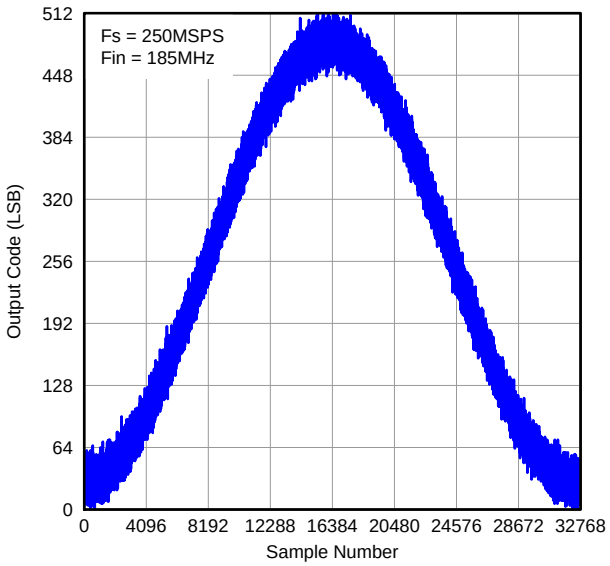


Figure 44.

TIME DOMAIN DATA WITH SNRBoost^{3G+} DISABLED

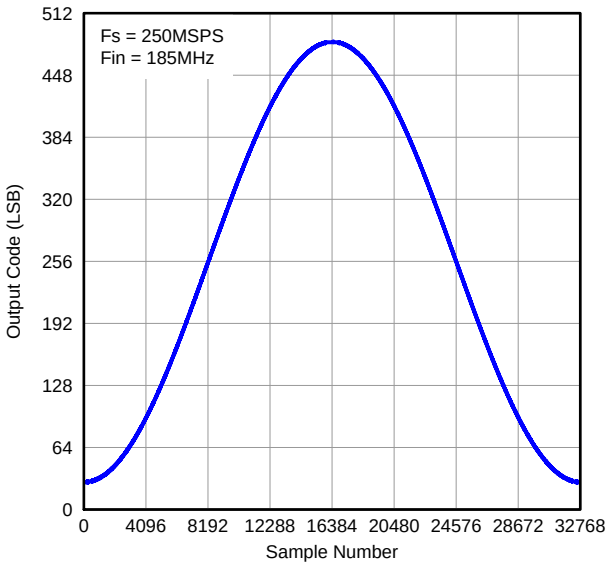


Figure 45.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

OUTPUT NOISE HISTOGRAM (WITH INPUTS SHORTED TO VCM)

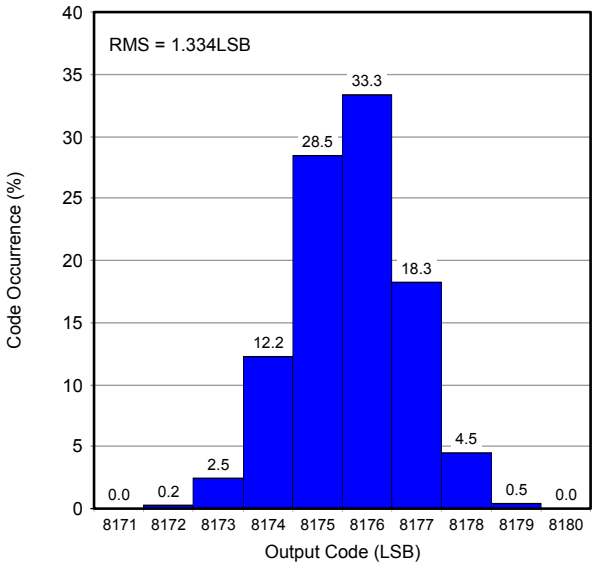


Figure 46.

CMRR vs FREQUENCY

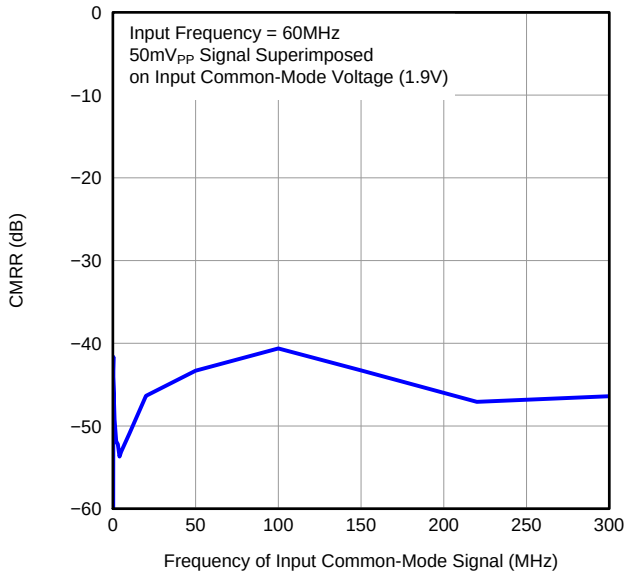


Figure 47.

CMRR SPECTRUM

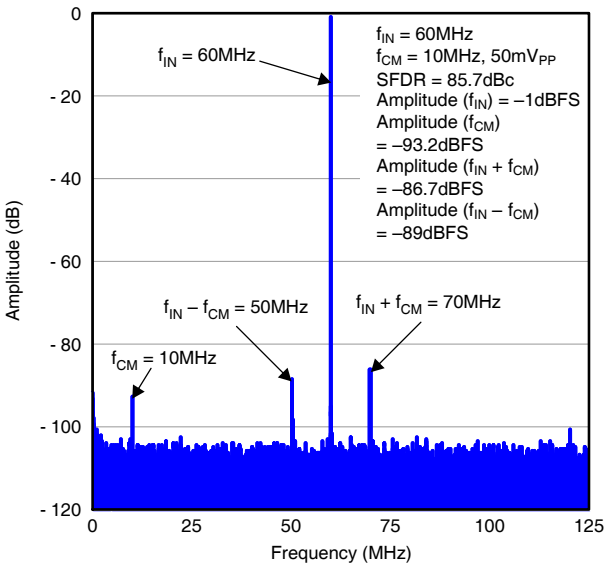


Figure 48.

PSRR vs FREQUENCY

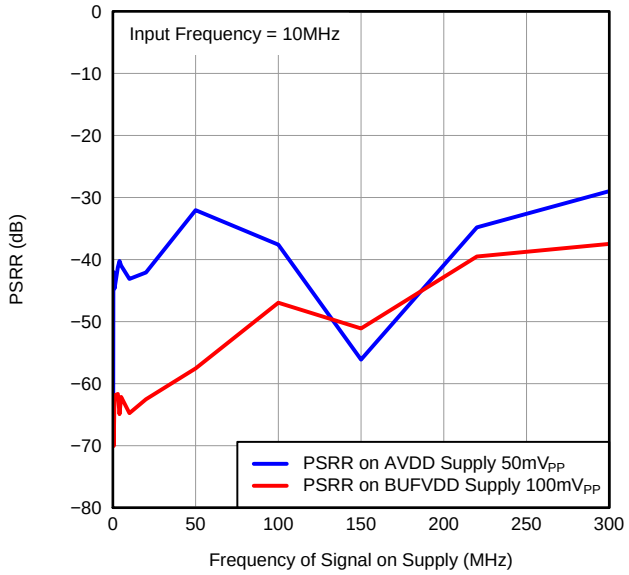


Figure 49.

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.9V, AVDD_BUF = 3.3V, DRVDD = 1.8V, rated sampling frequency, 0.5dB gain, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

ZOOMED VIEW OF PSRR SPECTRUM

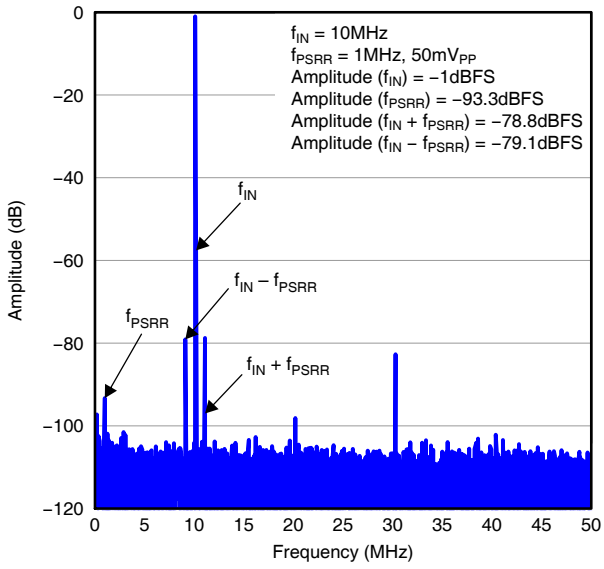


Figure 50.

TOTAL POWER vs SAMPLE RATE

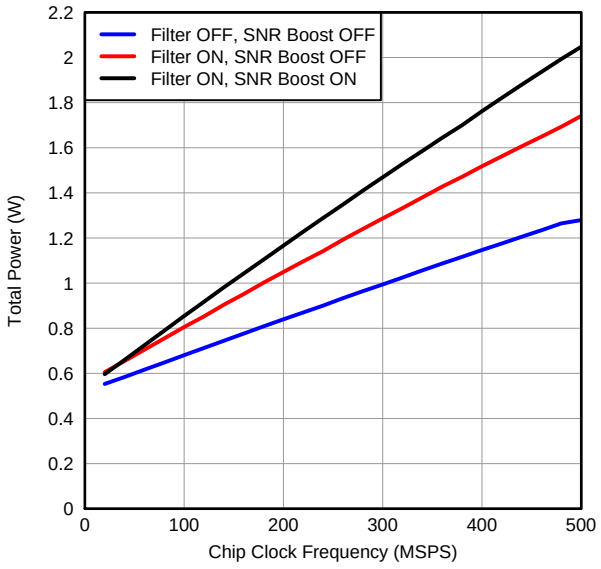


Figure 51.

ANALOG POWER vs SAMPLE RATE

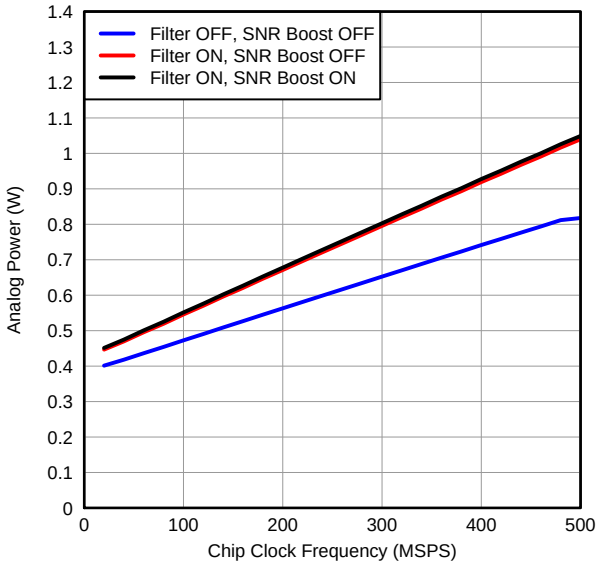


Figure 52.

LVDS DRVDD POWER vs SAMPLE RATE IN VARIOUS DIGITAL MODES

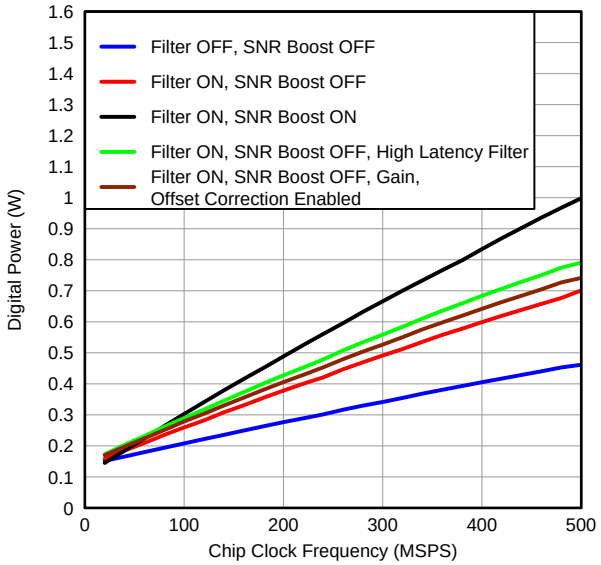


Figure 53.

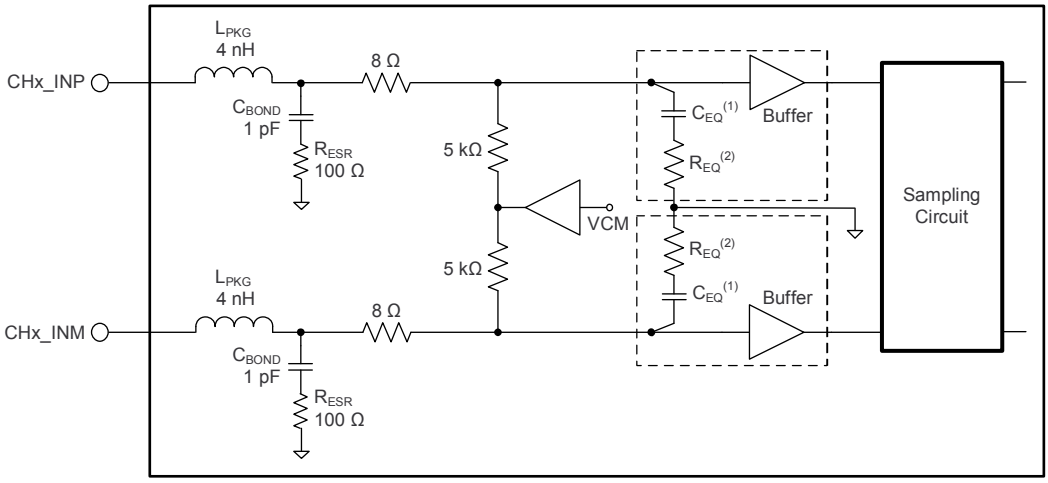
APPLICATION INFORMATION

THEORY OF OPERATION

The ADS58C20/23 are high performance, dual channel, low power IF receivers for communication applications.

ANALOG INPUT

The analog inputs include an analog buffer (running off the AVDD_BUF supply) that internally drives the differential sampling circuit. Due to the analog buffer, the input pins present high input impedance to the external driving source. The buffer helps to isolate the external driving source from the switching currents of the sampling circuit. With constant input impedance, the ADC is easier to drive and to reproduce data sheet measurements. For wide-band applications, like power amplifier linearization, the signal gain across frequency is more consistent. Spectral performance variation across sampling frequency is also reduced. The input common-mode is set internally using a 5-kΩ resistor from each input pin to 1.9V, so the input signal can be ac-coupled to the pins. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.45V and VCM – 0.45V, resulting in a $1.9V_{PP}$ differential input swing.



(1) C_{EQ} refers to the equivalent input capcitance of the buffer = 9.5pF

(2) R_{EQ} refers to the equivalent input resistance of the buffer = 20Ω

Figure 54. Analog Input Equivalent Circuit

The input sampling circuit has a high 3-dB bandwidth that extends up to 750 MHz (measured from the input pins to the sampled voltage).

Drive Circuit Requirements

The main advantage of the buffered analog inputs is the isolation of the external drive source from the switching currents of the sampling circuit. Using a simple drive circuit, it is possible to get uniform performance over a wide frequency range.

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A small resistor (5 to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 55 and Figure 56 show the differential impedance seen by looking into the ADC input pins.

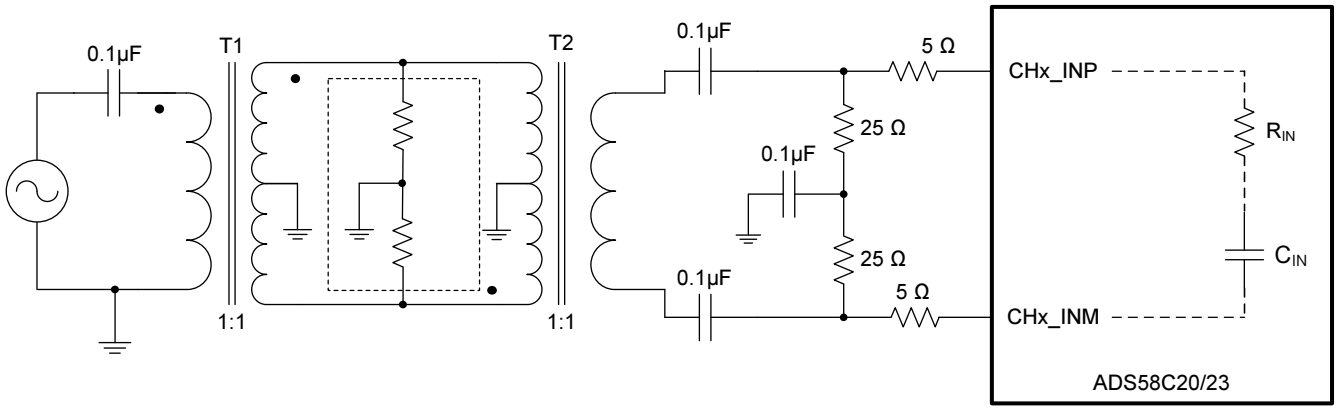


Figure 55. Input Drive Circuit

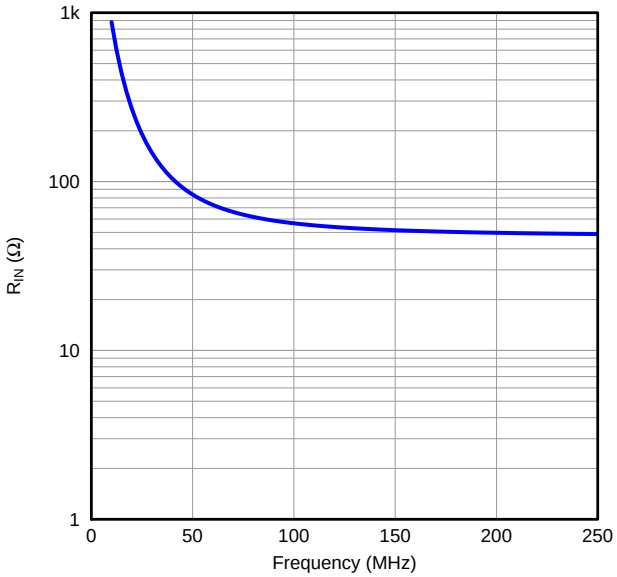


Figure 56. R_{IN} vs Input Frequency

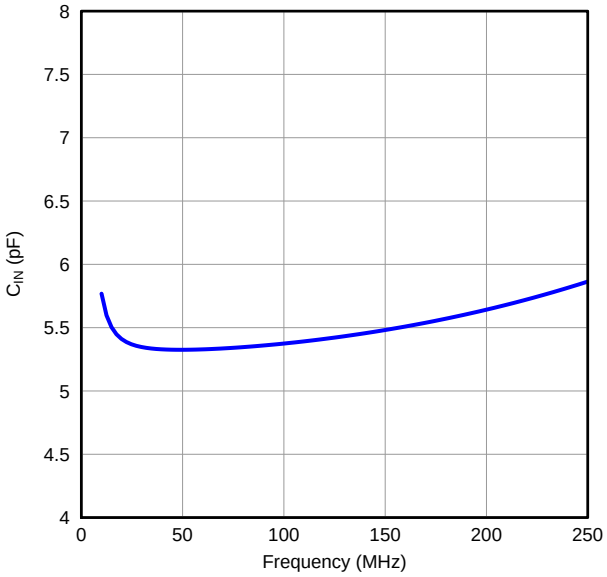
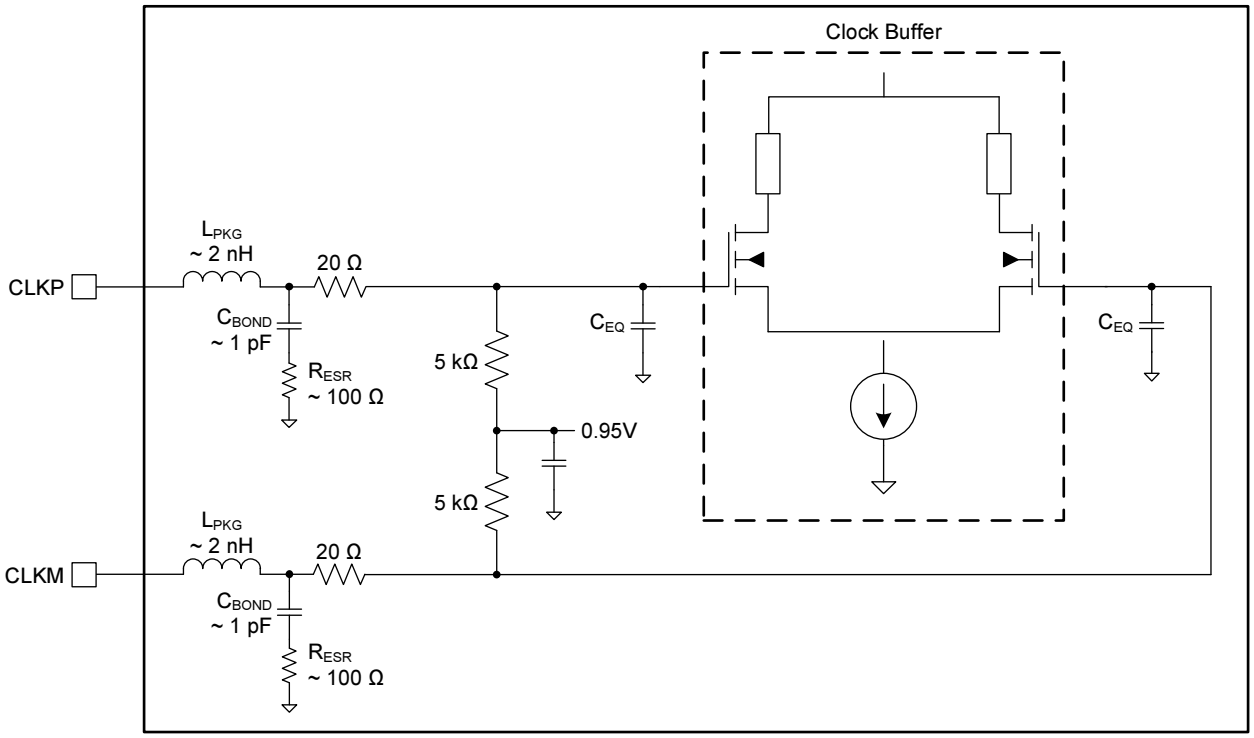


Figure 57. C_{IN} vs Input Frequency

CLOCK INPUT

The ADS58C20 clock inputs can be driven differentially by sine, LVPECL, or LVDS source with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95V using internal 5kΩ resistors as show in Figure 58. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources (see Figure 59, Figure 60, Figure 61, and Figure 61).



Note: C_{EQ} is 1pF to 3pF and is the equivalent input capacitance of the clock buffer.

Figure 58. Internal Clock Buffer

For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. It is recommended to keep differential voltage between clock inputs less than 1.8VPP to get best performance. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

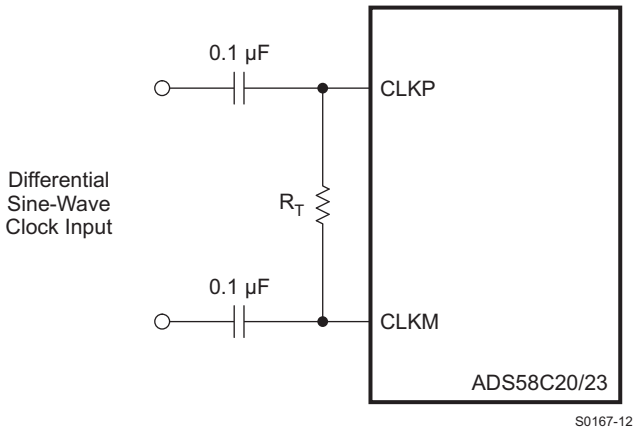


Figure 59. Differential Sine-Wave Clock Driving Circuit

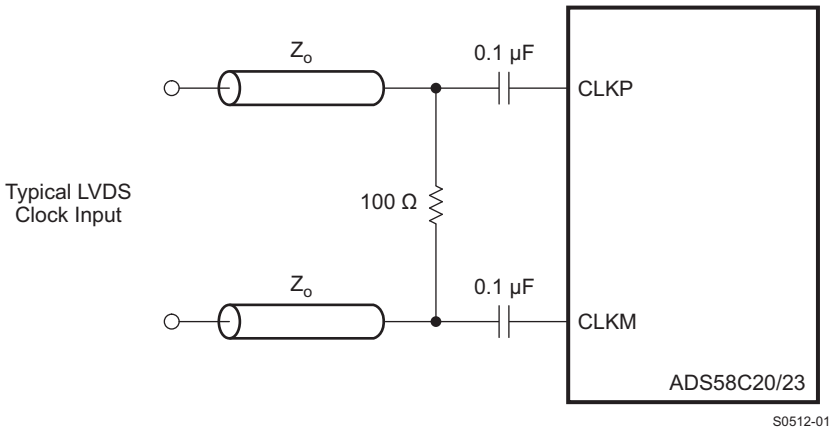


Figure 60. LVDS Clock Driving Circuit

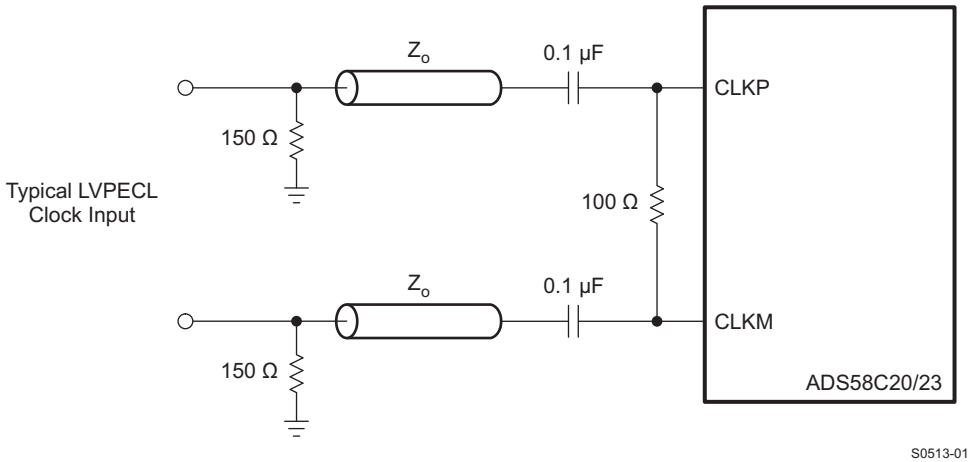
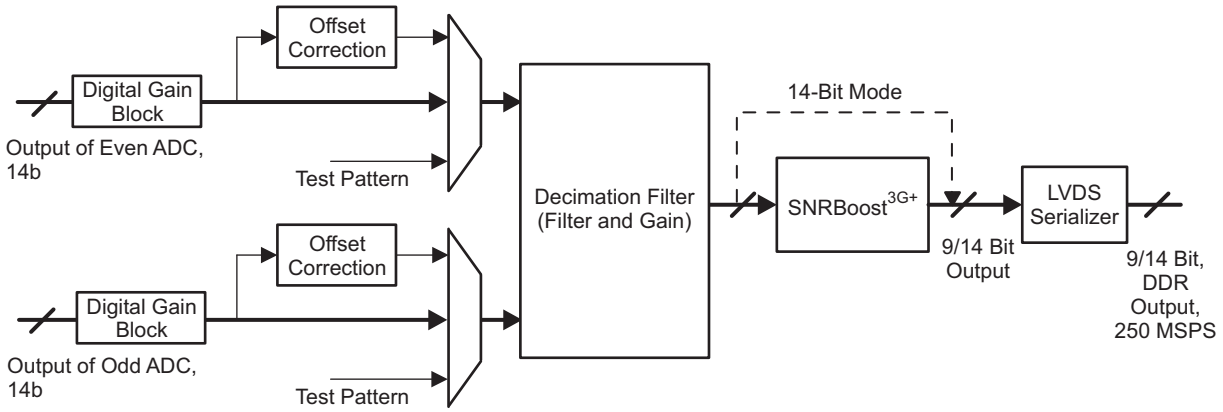


Figure 61. LVPECL Clock Driving Circuit

DIGITAL PROCESSING BLOCK

The block diagram for the digital processing block that follows the ADC core is shown in Figure 62.



Note: Both channels (1 and 2) have similar Digital Block Diagrams as shown above

Figure 62. Digital Block Diagram

There is a dedicated digital processing block for each channel. This block follows the output of two interleaving ADCs. Each ADC has a dedicated digital gain block, offset correction block and a test-patter generator. ADS58C20/23 gives flexibility to test data-path of each ADC independently through serial register bits by forcing the test-patterns of ADC to the channel's output data bits.

Decimation Filter Block in data-path works on interleaved data of even and odd ADCs of a channel. The filter can be programmed for low-pass or high–pass filtering operations. The filter can also be programmed to improve the pass-band ripple by choosing a higher order filter. The filter can also be used to gain up the digital output as described in table below. The decimation filter can also be bypassed for applications requiring full Nyquist bandwidth support. See Digital Filter.

The Decimation Filter Block is followed by SNRBoost^{3G+}block. The SNRBoost^{3G+} can only be used in 9-bit mode. When 14-bit mode option is selected, SNRBoost^{3G+} can not be used. The 9-bit (or 14-bit) output of ADS58C20/23 comes out from LVDS serializer block in DDR LVDS format with one dedicated output clock for each channel.

There are two ways of programming the gain:

- Filter Gain: Each channel can be programmed for a different amount of gain.
- Digital Gain Block: Each ADC of every channel can be programmed for a different amount of gain independent of filter's gain settings.

Programming Filter Gain

After reset, the decimation filter is enabled with a default gain of 1.6dB. The default gain value is changed to 1.9dB when 75MHz SNRBoost^{3G+}bandwidth is selected. Filter gain can be programmed from -3.1 to +3 dB. It can be performed as described in the following table.

SPI REGISTER ADDRESS (hex)			GAIN AMOUNT (dB)
ADDRESS FOR CH 1	ADDRESS FOR CH 2	VALUE (hex)	
2C	32	00	1.6dB (default) (1.9dB if 75MHz SNRBoost^{3G+} BW is selected)
2C	32	04	–3.1
2C	32	0C	–2.1
2C	32	14	–1.5
2C	32	1C	–1
2C	32	24	–0.5
2C	32	2C	0

SPI REGISTER ADDRESS (hex)			GAIN AMOUNT (dB)
ADDRESS FOR CH 1	ADDRESS FOR CH 2	VALUE (hex)	
2C	32	34	0.5
2C	32	3C	1
2C	32	44	1.5
2C	32	4C	2
2C	32	54	3

When the filter is bypassed, the above gain modes cannot be exercised.

Programming Digital Gain Block

There is a separate digital gain block following each ADC of every channel which works independent to filter-gain. Digital gain can be programmed individually for each ADC from 0 to 6dB in steps of 0.5dB. Bit <DIG GAIN EN COMMON> of register 0x42 has to be set to enable digital gain blocks of all ADCs. The following table lists the amount of gain versus programmed bits.

SPI REGISTER ADDRESS (hex)					GAIN AMOUNT (dB)
EVEN ADC OF CH 1	ODD ADC OF CH 1	EVEN ADC OF CH 2	ODD ADC OF CH 2	VALUE (hex)	
2B	25	31	37	00	0
2B	25	31	37	10	0.5
2B	25	31	37	20	1
2B	25	31	37	30	1.5
2B	25	31	37	40	2
2B	25	31	37	50	2.5
2B	25	31	37	60	3
2B	25	31	37	70	3.5
2B	25	31	37	80	4
2B	25	31	37	90	4.5
2B	25	31	37	A0	5
2B	25	31	37	B0	5.5
2B	25	31	37	C0	6.0

MAXIMUM APPLICABLE INPUT AND OUTPUT POWER

When SNRBoost^{3G+} is selected, it is required to limit the output codes swing. The maximum value of the output code swing depends on the bandwidth of the SNRBoost^{3G+} filter. Note that for a given max output code, corresponding input signal voltage depends on the channel gain.

If the overall data path from the ADC core to the final output sees *G* (gain), then Table 3 lists the maximum input voltage which can be differentially applied between INP and INM for a given SNRBoost^{3G+} BW.

Table 3. Output Power for Different SNRBoost BW

SNRBoost^{3G+} BW	MAXIMUM FUNDAMENTAL SIGNAL POWER IN OUTPUT CODE WITHOUT SATURATION	GAIN	MAXIMUM INPUT SIGNAL POWER
40 MHz	–1.6 dBFS	0dB	–1.6 dBFS (1.7V_{pp})
40 MHz	–1.6 dBFS	*G* (filter +digital block gain)	–1.6-G dBFS
75 MHz	–1.9 dBFS	0dB	–1.9 dBFS (1.6V_{pp})
75 MHz	–1.9 dBFS	*G* (filter +digital block gain)	–1.9-G dBFS

Digital Filter

Each channel has a digital filter in the data path as shown in Figure 62. The filter can be programmed as a low-pass or high-pass filter. The order of the filter can be chosen between 12^{th} or 20^{th} order with 12^{th} order being the default after reset. The higher order filter can be selected for better in-band ripple requirement. The normalized frequency responses of all four types of filters are shown in Figure 63.

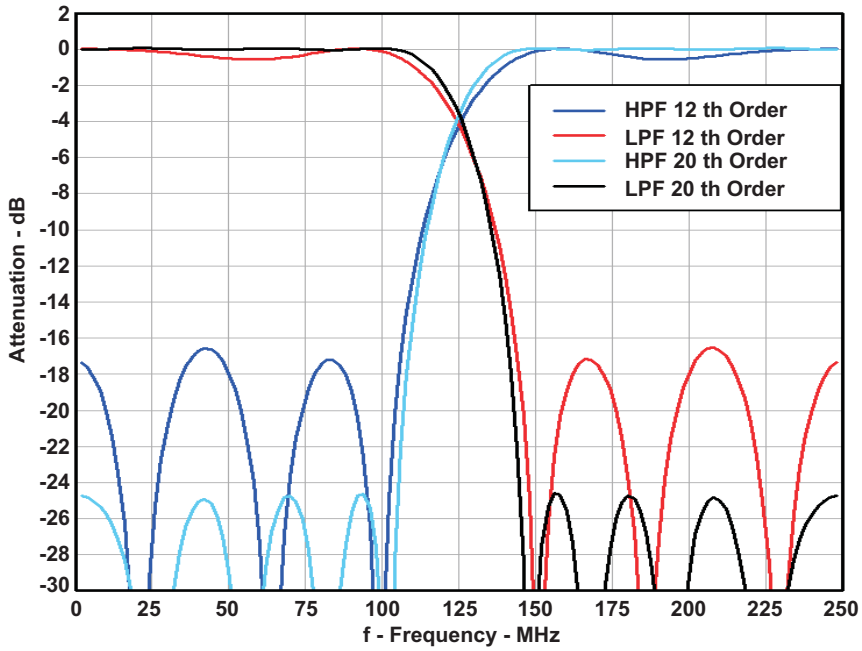


Figure 63. Normalized Frequency Responses of Filters

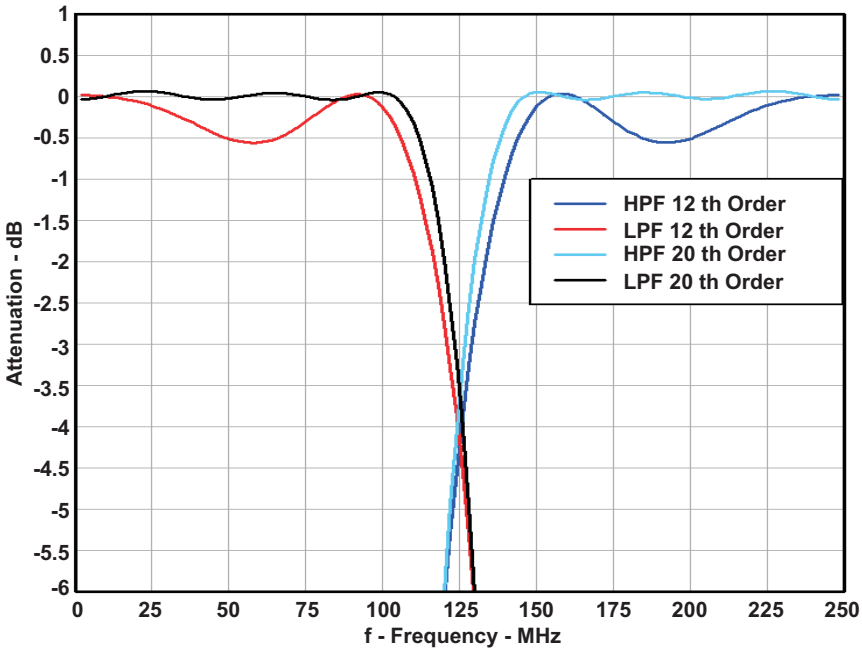


Figure 64. Zoomed View of Normalized Frequency Responses

Using SYNC pins

In the applications where it is required to synchronize sampling instant of multiple ADS58C20 chips running of same chip clock, sync pins can be used. In ADS58C20/23, the chip clock is divided by 2 and then it is given to EVEN and ODD ADCs of two channels. The phase difference between EVEN (or ODD) ADCs of two chips can be 0 or 180 degree depending upon state of chip clock divider after power up. In this case, a low to high going pulse can be applied differentially between SYNCP and SYNCM pins of all chips to ensure that all EVEN (or ODD) ADCs of all chips are phase aligned.

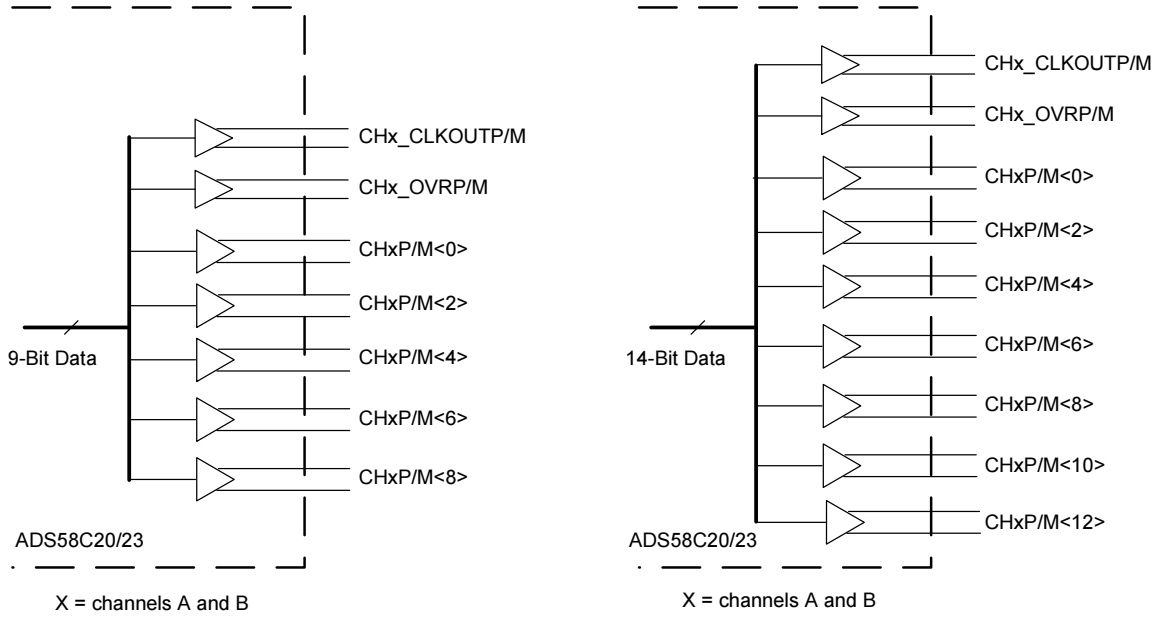
The SYNCP and SYNCM pins are self biased to 0.95V. So, these pins can be ac coupled to LVPECL or LVDS driver. When not used, the sync pins MUST NOT be floated or shorted to each other as any spurious noise signal between them can be interpreted as a sync pulse causing temporary glitches in ADC clocks, hence in output clocks. Therefore it is recommended to tie SYNCP to AVDD and SYNCM to ground when these pins are not used. Alternatively, the sync pins should be disabled by setting bit <DIS SYNC PIN>.

DIGITAL OUTPUT INFORMATION

The ADS58C20/23 provide a 9-bit/14-bit digital data with a dedicated output clock for each channel.

DDR LVDS Output Interface

The data bits and output clocks are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair.



A) ADS5820/23 LVDS Outputs in 9-Bit Mode

B) ADS5820/23 LVDS Outputs in 14-Bit Mode

Figure 65. DDR LVDS Interface

See Figure 2 for LVDS output bit order in 9-bit mode and Figure 3 for LVDS output bit order in 14-bit mode.

LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 66. After reset, the buffer presents an output impedance of 100Ω to match with the external 100Ω termination.

The V_{DIFF} voltage is nominally 350mV, resulting in an output swing of ±350mV with 100Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±120mV to ±600mV.

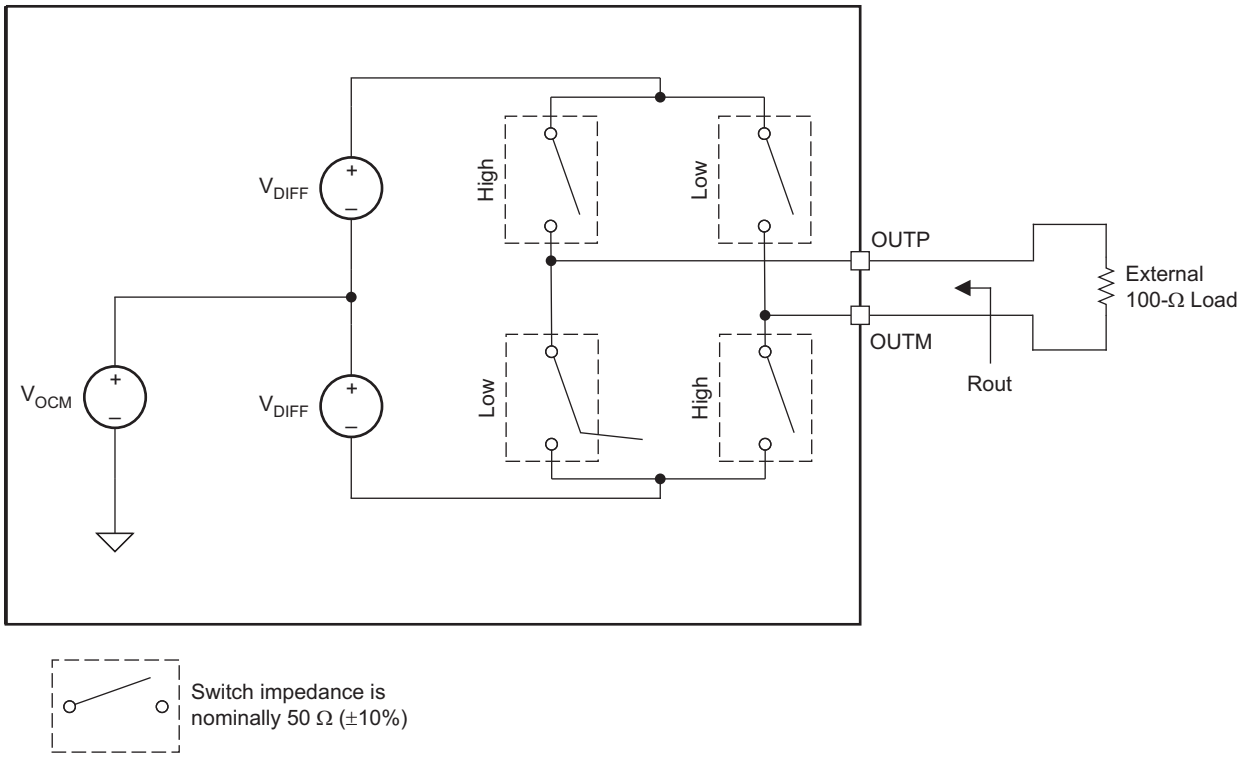


Figure 66. LVDS Buffer Equivalent Circuit

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error due to reference inaccuracy and error due to the channel. Both these errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first order approximation, the total gain error will be $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1\text{-}0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (PS) to the noise floor power (PN), excluding the power at DC and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB) – The ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{3}$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (PD).

$$\text{THD} = 10\text{Log}^{10} \frac{P_S}{P_N} \tag{4}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR) – The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

AC Power Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔVout is the resultant change of the ADC output code (referred to the input), then

$$\text{PSRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \tag{5}$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from their expected values) is noted.

Common Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔVcm_in is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then

$$\text{CMRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \tag{6}$$

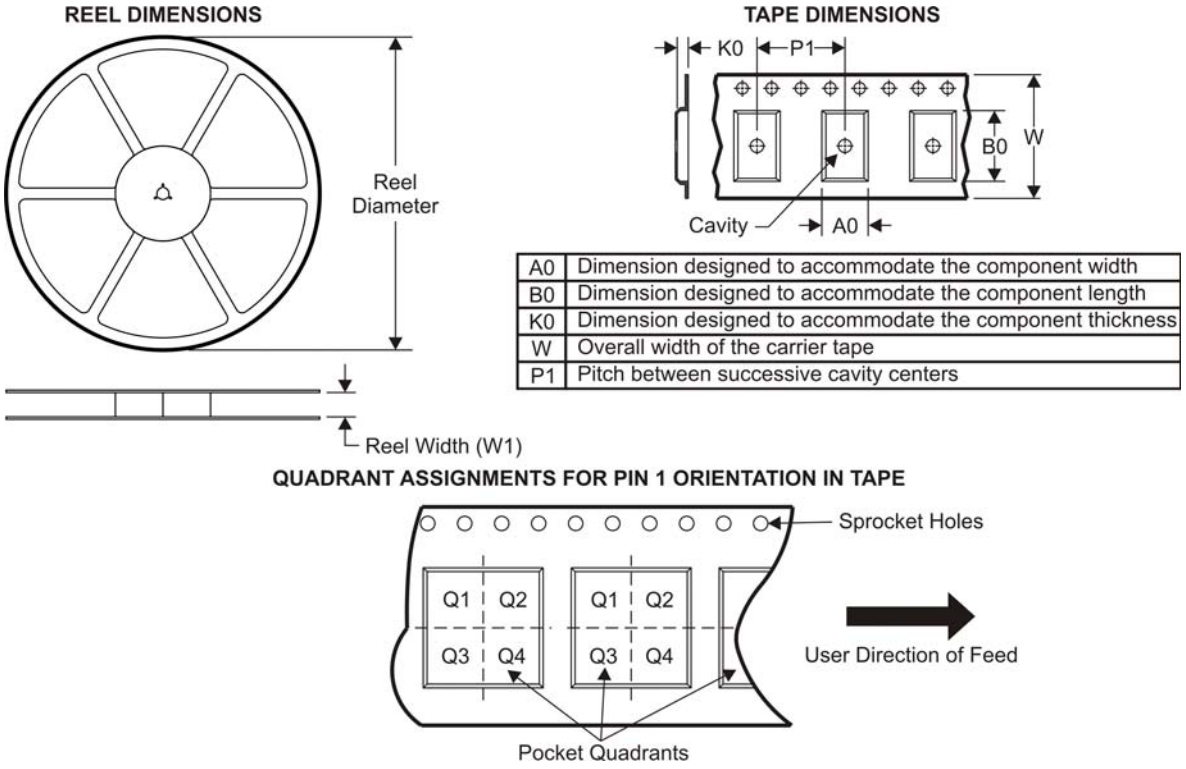
Cross-Talk (only for multi-channel ADC)– This is a measure of the internal coupling of a signal from adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Cross-talk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

PACKAGING INFORMATION

Orderable Device	Status (1)	Pack Type	Pack Drawing	Pins	Pack Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)
ADS58C20IPFP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS58C20IPFPR	ACTIVE	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS58C23IPFP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS58C23IPFPR	ACTIVE	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
(2) Eco Plan -The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) -please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and lead frame. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
(3) MSL, Peak Temp. --The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications and peak solder temperature.

TAPE AND REEL INFORMATION

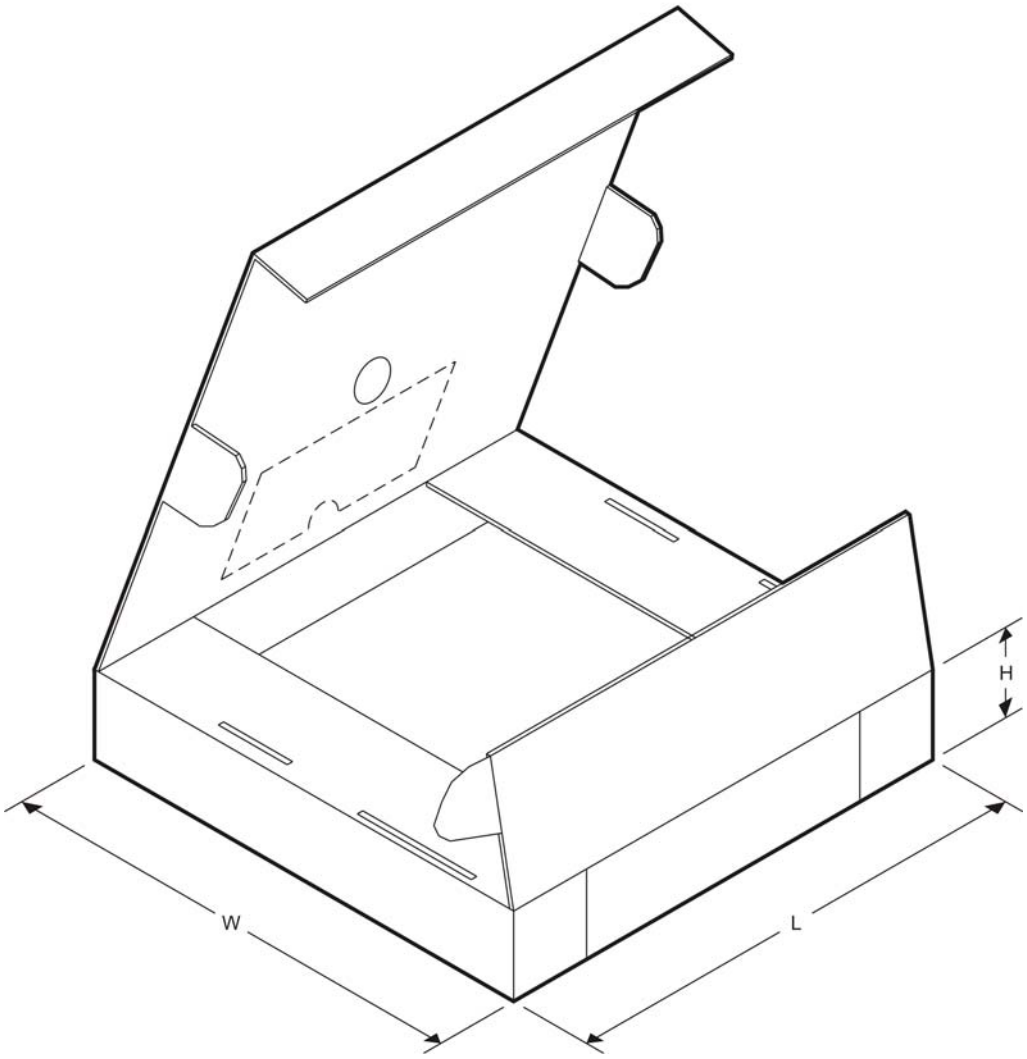


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS58C20IPFP	HTQFP	PFP	80	1000	300.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
ADS58C23IPFPR	HTQFP	PFP	80	1000	300.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2

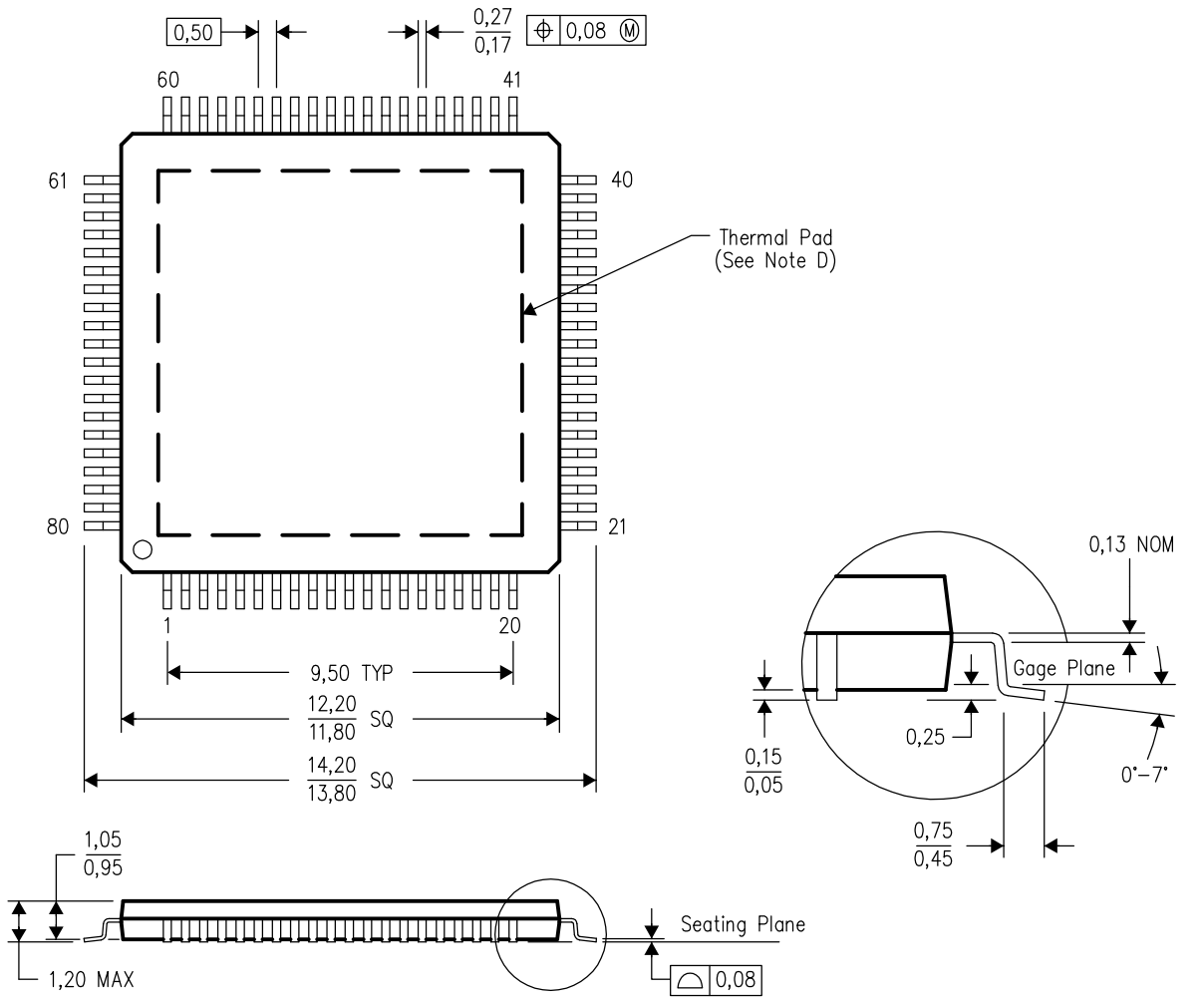
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS58C20IPFP	HTQFP	PFP	80	1000	346.0	346.0	41.0
ADS58C23IPFPR	HTQFP	PFP	80	1000	346..0	346.0	41.0

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

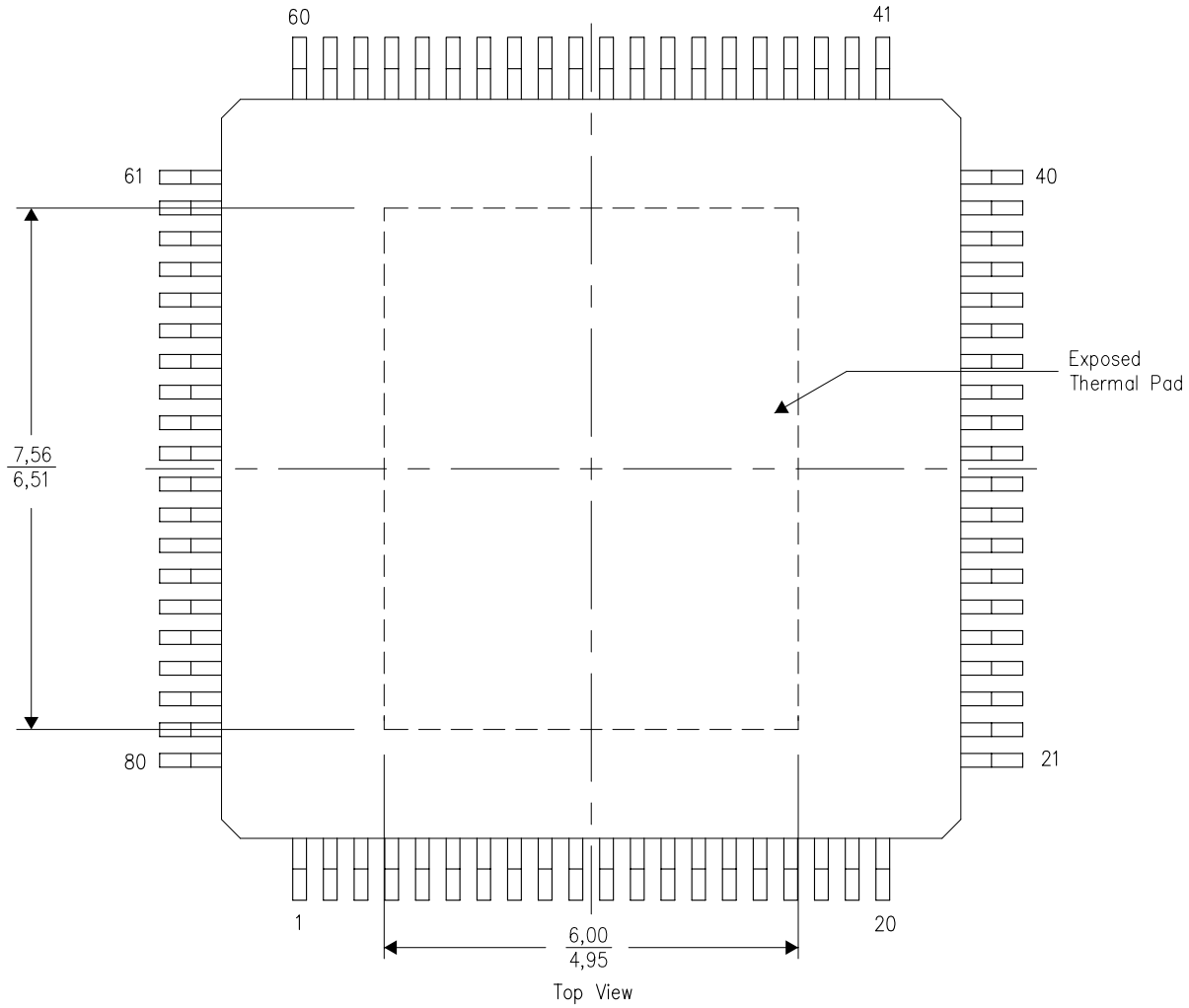
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206327–14/M 02/11

NOTE: A. All linear dimensions are in millimeters

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Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
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