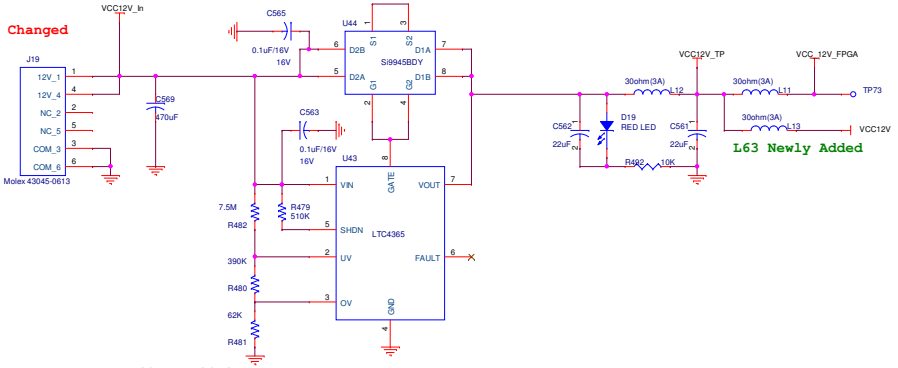
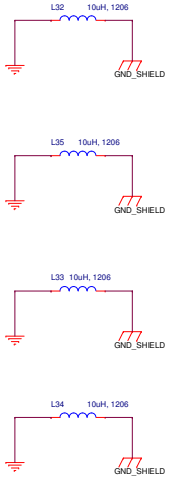
J17 Part Changed

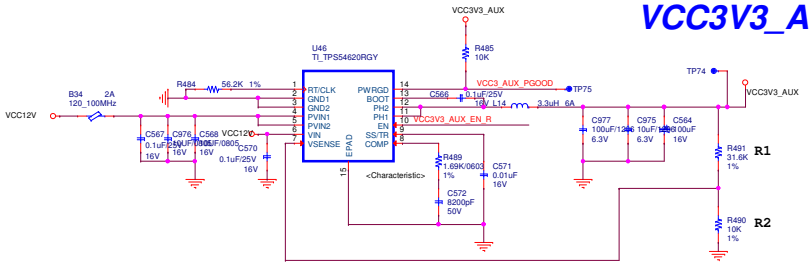


L63 Newly Added

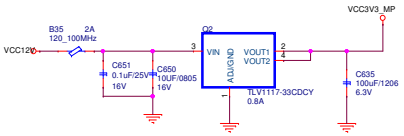


As per PI suggestion C3055, C3053 to be placed near U48 pin 6 and C3054 to be placed near U47 pin 1

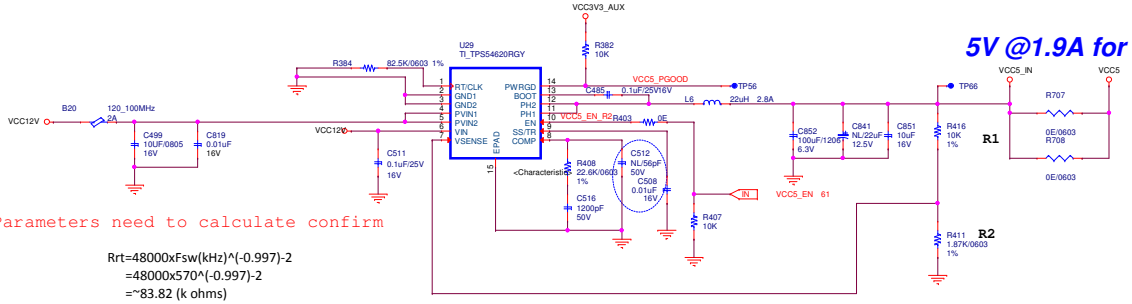
VCC3V3_AUX



VCC3V3_MP_ALT



5V @1.9A for USB

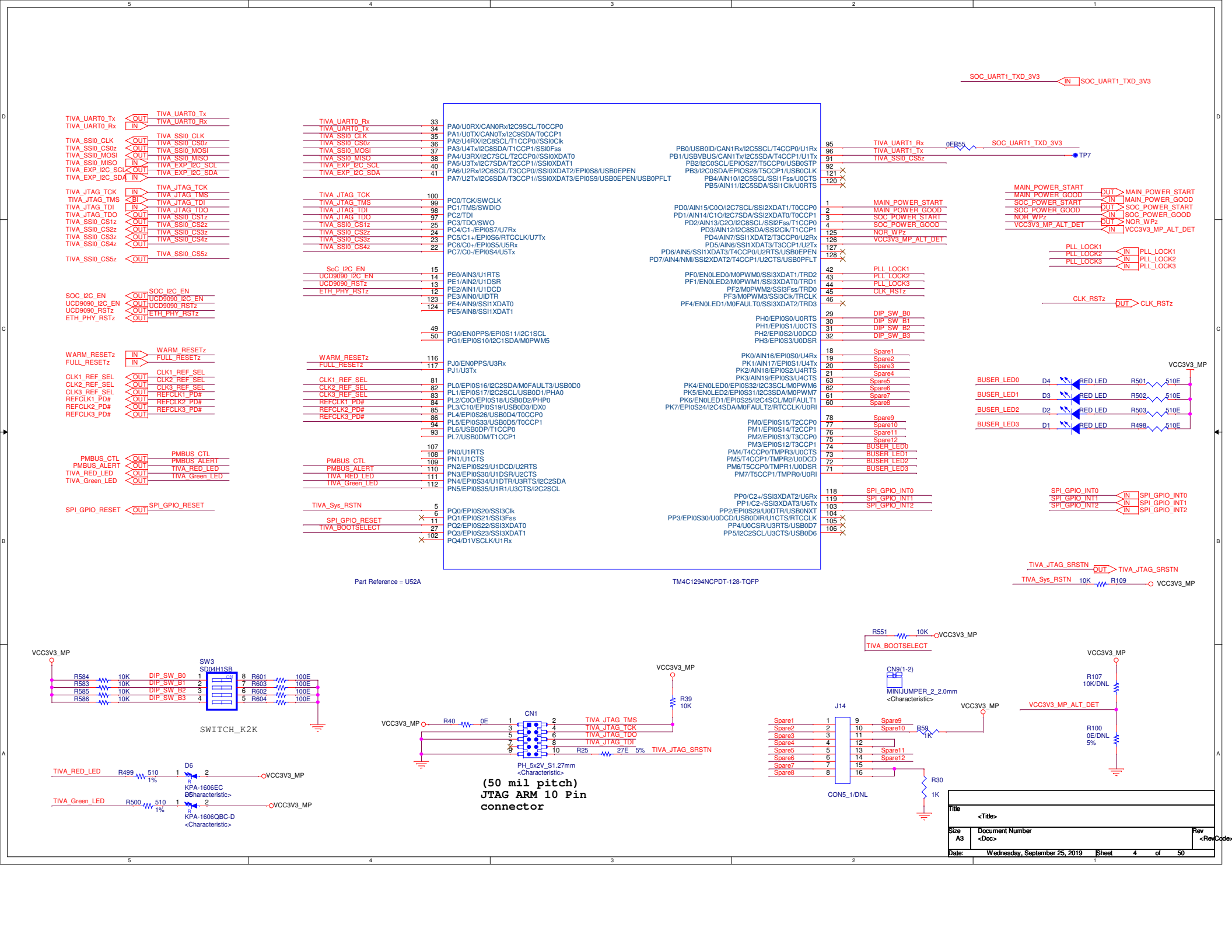


*Parameters need to calculate confirm

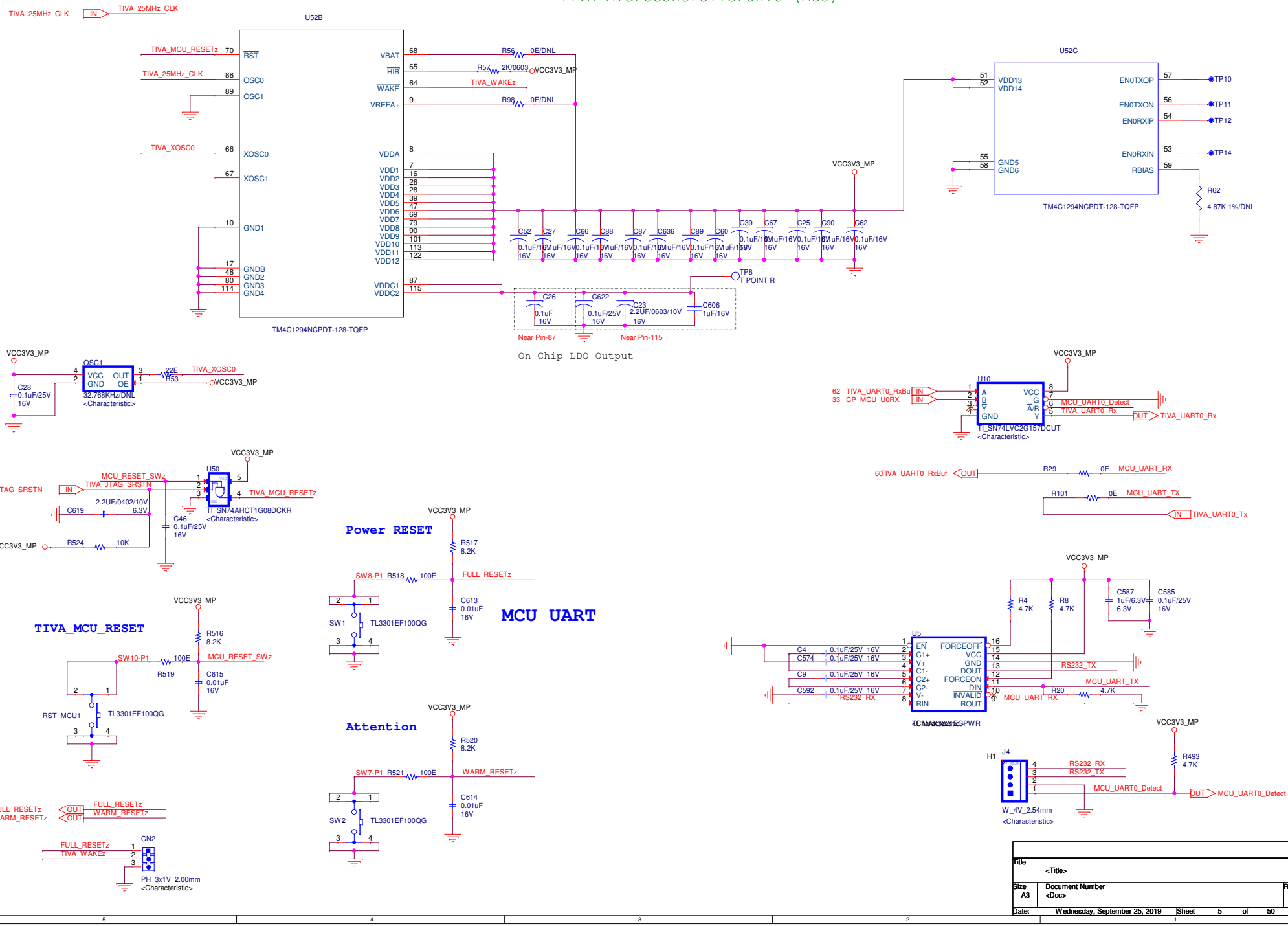
Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x570^(-0.997)-2
=~83.82 (k ohms)

Standby Power Control for UCD9090 Flash
Installed Jumper(Default): For correct Power sequence
Remove Jumper: For burned into UCD9090 register code

Title: <Title>		
Size: A2	Document Number: <Doc>	Rev: <RevCode>
Date: Wednesday, September 25, 2019	Sheet 3 of 50	

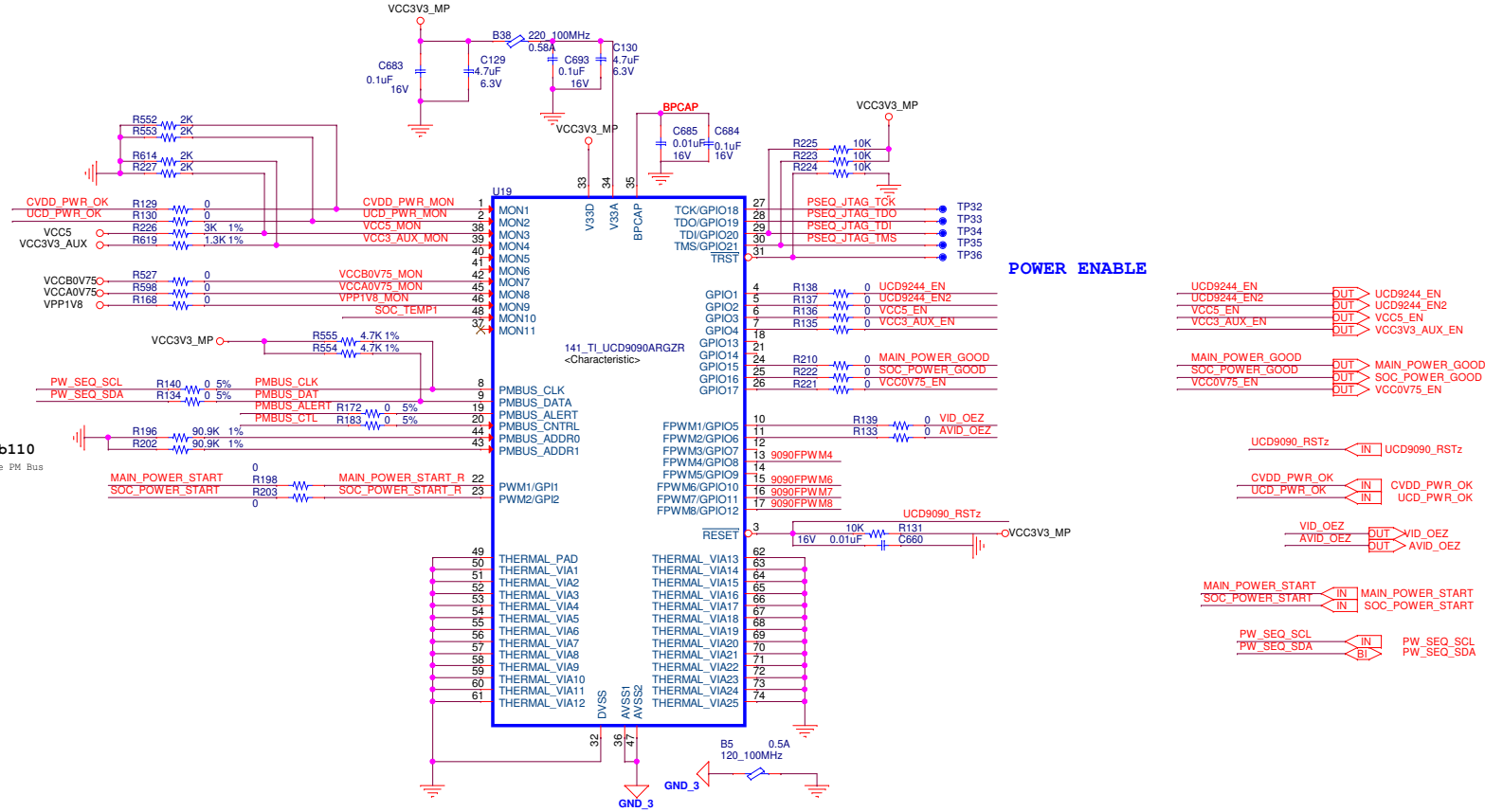

SOC_UART1_TXD_3V3
TIVA_UART0_Tx
TIVA_UART0_Rx
TIVA_SSI0_CLK
TIVA_SSI0_CS0z
TIVA_SSI0_MOSI
TIVA_SSI0_MISO
TIVA_EXP_I2C_SCL
TIVA_EXP_I2C_SDA
TIVA_JTAG_TCK
TIVA_JTAG_TMS
TIVA_JTAG_TDI
TIVA_JTAG_TDO
TIVA_SSI0_CS1z
TIVA_SSI0_CS2z
TIVA_SSI0_CS3z
TIVA_SSI0_CS4z
TIVA_SSI0_CS5z
SoC_I2C_EN
UCD9090_I2C_EN
UCD9090_RSTz
ETH_PHY_RSTz
WARM_RESETz
FULL_RESETz
CLK1_REF_SEL
CLK2_REF_SEL
CLK3_REF_SEL
REFCLK1_PD#
REFCLK2_PD#
REFCLK3_PD#
PMBUS_CTL
PMBUS_ALERT
TIVA_RED_LED
TIVA_Green_LED
SPI_GPIO_RESET
TIVA_Sys_RSTN
TIVA_BOOTSELECT
PA0/U0RX/CAN0Rx/I2C9SCL/T0CCP0
PA1/U0TX/CAN0Tx/I2C9SDA/T0CCP1
PA2/U4RX/I2C8SCL/T1CCP0//SSI0Clk
PA3/U4Tx/I2C8SDA/T1CCP1/SSI0Fss
PA4/U3RX/I2C7SCL/T2CCP0//SSI0XDAT0
PA5/U3Tx/I2C7SDA/T2CCP1//SSI0XDAT1
PA6/U2Rx/I2C6SCL/T3CCP0//SSI0XDAT2/EPI0S8/USB0EPEN
PA7/U2Tx/I2C6SDA/T3CCP1//SSI0XDAT3/EPI0S9/USB0EPEN/USB0PFLT
PC0/TCK/SWCLK
PC1/TMS/SWDIO
PC2/TDI
PC3/TDO/SWO
PC4/C1-/EPI0S7/U7Rx
PC5/C1+/EPI0S6/RTCCLK/U7Tx
PC6/C0+/EPI0S5/U5Rx
PC7/C0-/EPI0S4/U5Tx
PE0/AIN3/U1RTS
PE1/AIN2/U1DSR
PE2/AIN1/U1DCD
PE3/AIN0/UIDTR
PE4/AIN9/SSI1XDAT0
PE5/AIN8/SSI1XDAT1
PG0/EN0PPS/EPI0S11/I2C1SCL
PG1/EPI0S10/I2C1SDA/M0PWM5
PJ0/EN0PPS/U3Rx
PJ1/U3Tx
PL0/EPI0S16/I2C2SDA/M0FAULT3/USB0D0
PL1/EPI0S17/I2C2SCL/USB0D1/PHA0
PL2/C0O/EPI0S18/USB0D2/PHP0
PL3/C1O/EPI0S19/USB0D3/IDX0
PL4/EPI0S26/USB0D4/T0CCP0
PL5/EPI0S33/USB0D5/T0CCP1
PL6/USB0DP/T1CCP0
PL7/USB0DM/T1CCP1
PN0/U1RTS
PN1/U1CTS
PN2/EPI0S29/U1DCD/U2RTS
PN3/EPI0S30/U1DSR/U2CTS
PN4/EPI0S34/U1DTR/U3RTS/I2C2SDA
PN5/EPI0S35/U1R1/U3CTS/I2C2SCL
PQ0/EPI0S20/SSI3Clk
PQ1/EPI0S21/SSI3Fss
PQ2/EPI0S22/SSI3XDAT0
PQ3/EPI0S23/SSI3XDAT1
PQ4/D1VSCLK/U1Rx
PB0/USB0ID/CAN1Rx/I2C5SCL/T4CCP0/U1Rx
PB1/USBVBUS/CAN1Tx/I2C5SDA/T4CCP1/U1Tx
PB2/I2C0SCL/EPI0S27/T5CCP0/USB0STP
PB3/I2C0SDA/EPI0S28/T5CCP1/USB0CLK
PB4/AIN10/I2C5SCL/SSI1Fss/U0CTS
PB5/AIN11/I2C5SDA/SSI1Clk/U0RTS
PD0/AIN15/C0O/I2C7SCL/SSI2XDAT1/T0CCP0
PD1/AIN14/C1O/I2C7SDA/SSI2XDAT0/T0CCP1
PD2/AIN13/C2O/I2C8SCL/SSI2Fss/T1CCP0
PD3/AIN12/I2C8SDA/SSI2Clk/T1CCP1
PD4/AIN7/SSI1XDAT2/T3CCP0/U2Rx
PD5/AIN6/SSI1XDAT3/T3CCP1/U2Tx
PD6/AIN5/SSI1XDAT3/T4CCP0/U2RTS/USB0EPEN
PD7/AIN4/NMI/SSI2XDAT2/T4CCP1/U2CTS/USB0PFLT
PF0/EN0LED0/M0PWM0/SSI3XDAT1/TRD2
PF1/EN0LED2/M0PWM1/SSI3XDAT0/TRD1
PF2/M0PWM2/SSI3Fss/TRD0
PF3/M0PWM3/SSI3Clk/TRCLK
PF4/EN0LED1/M0FAULT0/SSI3XDAT2/TRD3
PH0/EPI0S0/U0RTS
PH1/EPI0S1/U0CTS
PH2/EPI0S2/U0DCD
PH3/EPI0S3/U0DSR
PK0/AIN16/EPI0S0/U4Rx
PK1/AIN17/EPI0S1/U4Tx
PK2/AIN18/EPI0S2/U4RTS
PK3/AIN19/EPI0S3/U4CTS
PK4/EN0LED0/EPI0S32/I2C3SCL/M0PWM6
PK5/EN0LED2/EPI0S31/I2C3SDA/M0PWM7
PK6/EN0LED1/EPI0S25/I2C4SCL/M0FAULT1
PK7/EPI0S24/I2C4SDA/M0FAULT2/RTCCLK/U0RI
PM0/EPI0S15/T2CCP0
PM1/EPI0S14/T2CCP1
PM2/EPI0S13/T3CCP0
PM3/EPI0S12/T3CCP1
PM4/T4CCP0/TMPR3/U0CTS
PM5/T4CCP1/TMPR2/U0DCD
PM6/T5CCP0/TMPR1/U0DSR
PM7/T5CCP1/TMPR0/U0RI
PP0/C2+/SSI3XDAT2/U6Rx
PP1/C2-/SSI3XDAT3/U6Tx
PP2/EPI0S29/U0DTR/USB0NXT
PP3/EPI0S30/U0DCD/USB0DIR/U1CTS/RTCCLK
PP4/U0CSR/U3RTS/USB0D7
PP5/I2C2SCL/U3CTS/USB0D6
Part Reference = U52A
TM4C1294NCPDT-128-TQFP
MAIN_POWER_START
MAIN_POWER_GOOD
SOC_POWER_START
SOC_POWER_GOOD
NOR_WPz
VCC3V3_MP_ALT_DET
PLL_LOCK1
PLL_LOCK2
PLL_LOCK3
CLK_RSTz
DIP_SW_B0
DIP_SW_B1
DIP_SW_B2
DIP_SW_B3
Spare1
Spare2
Spare3
Spare4
Spare5
Spare6
Spare7
Spare8
Spare9
Spare10
Spare11
Spare12
BUSER_LED0
BUSER_LED1
BUSER_LED2
BUSER_LED3
SPI_GPIO_INT0
SPI_GPIO_INT1
SPI_GPIO_INT2
TIVA_JTAG_SRSTN
VCC3V3_MP
0ER55
TP7
D4
D3
D2
D1
RED LED
R501
R502
R503
R498
510E
SW3
SD04H1SB
SWITCH_K2K
R584
R583
R585
R586
10K
DIP_SW_B0
DIP_SW_B1
DIP_SW_B2
DIP_SW_B3
R601
R603
R602
R604
100E
R499
R500
510
1%
D6
KPA-1606EC
KPA-1606QBC-D
<Characteristic>
CN1
PH_5x2V_S1.27mm
R40
0E
R39
R25
27E
5%
(50 mil pitch)
JTAG ARM 10 Pin
connector
R551
CN9(1-2)
MINIJUMPER_2_2.0mm
J14
CON5_1/DNL
R59
1K
R30
R107
10K/DNL
R100
0E/DNL
Title
<Title>
Size
A3
Document Number
<Doc>
Rev
<RevCode>
Date:
Wednesday, September 25, 2019
Sheet
4
of
50

TIVA MicroControllerUnit (MCU)



Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCode>
Date: Wednesday, September 25, 2019		Sheet 5 of 50	

Power Sequencing

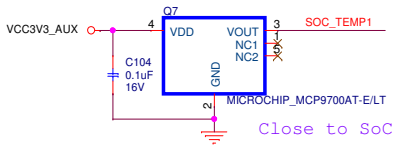


Slave I2C Address = 0x65
(Internal ADDR[7:5] = 0b110

With 90.9K resistor for the ADR, the PM Bus address is 0x68 (104d)

POWER ENABLE

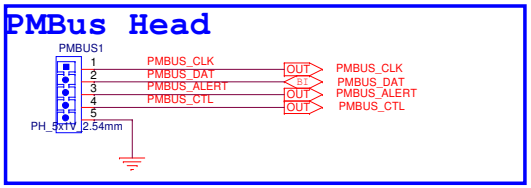
POWER DETECT

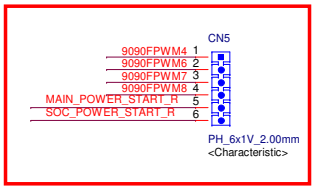


PMBus Address Bins

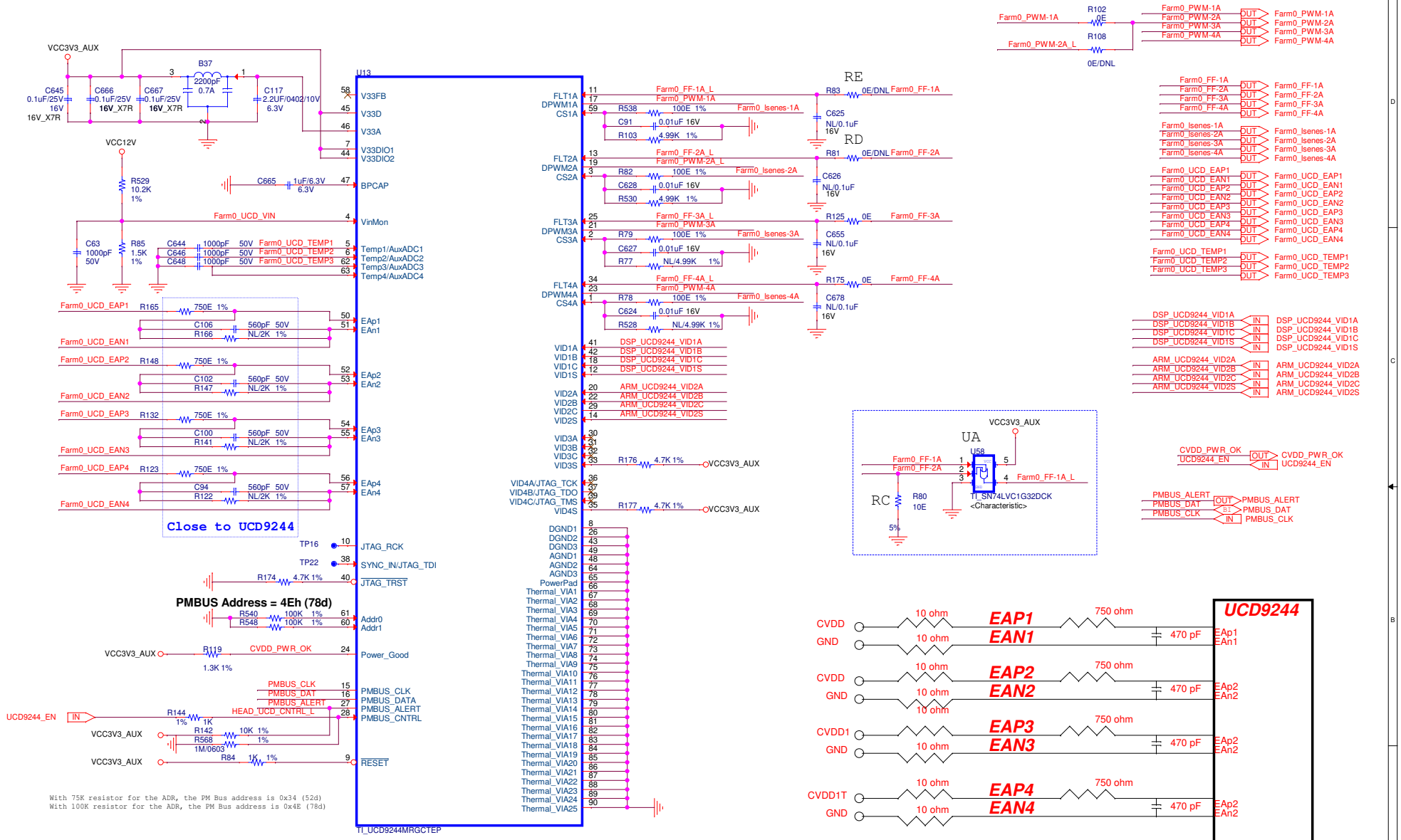
PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

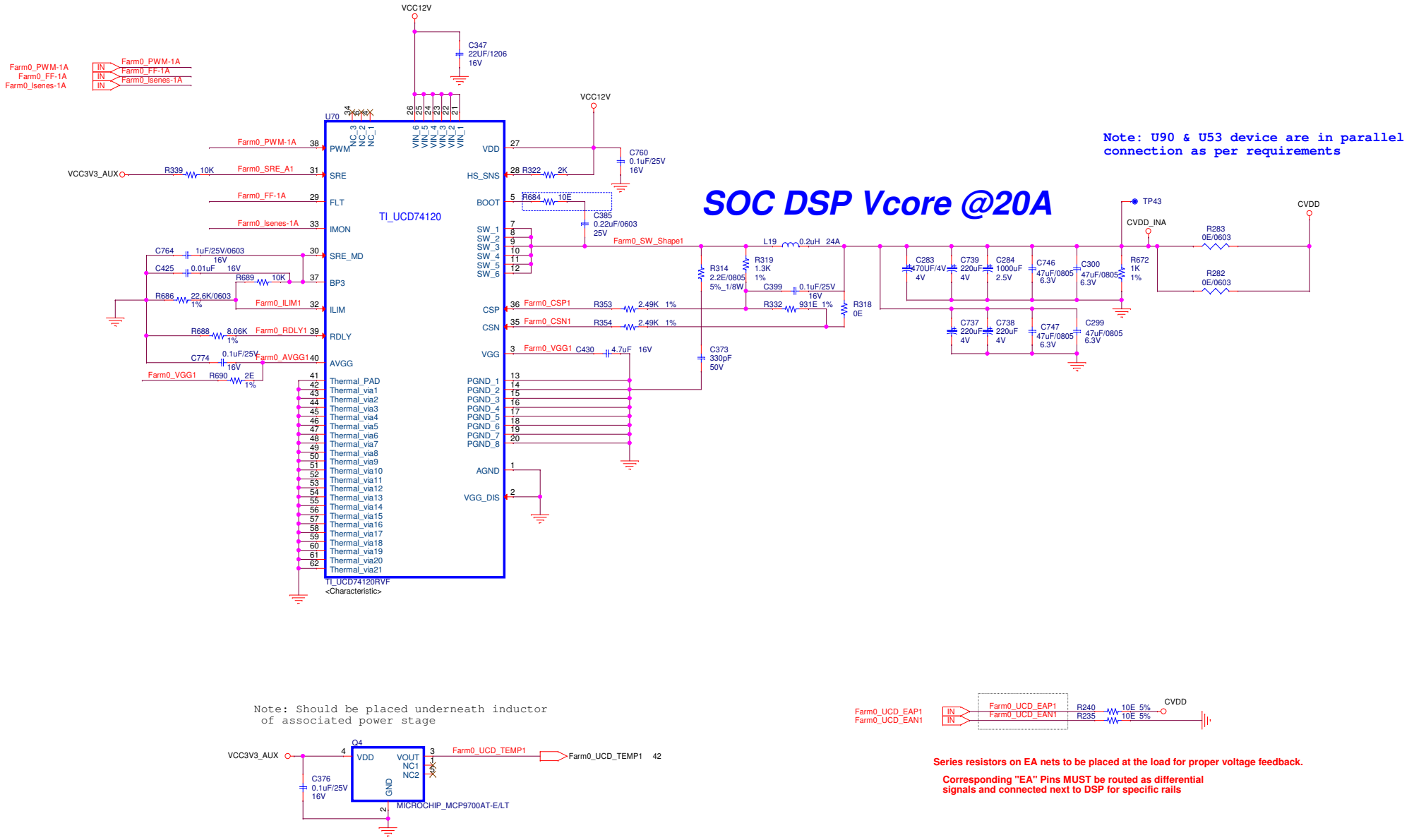
PMBus Head

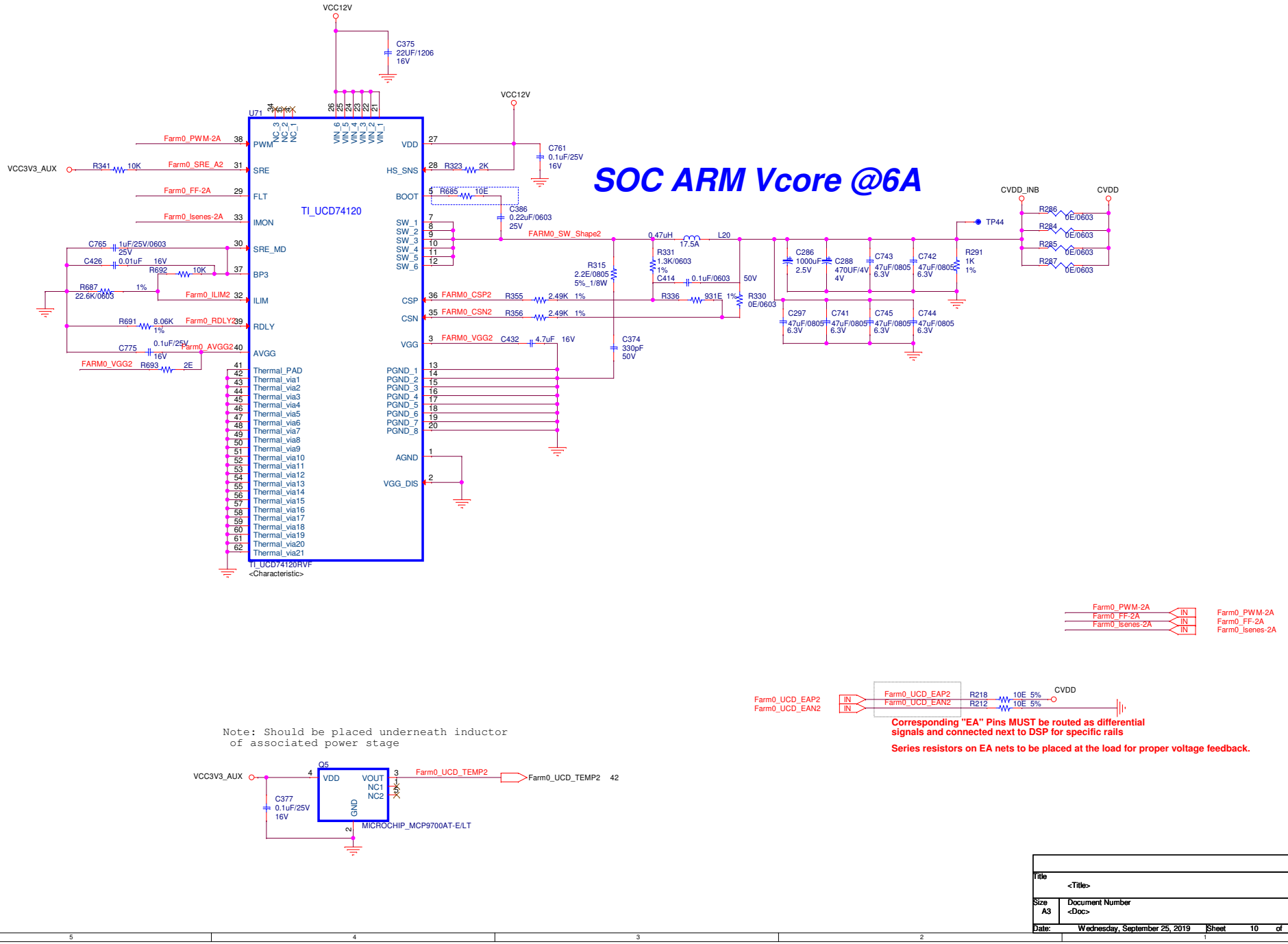




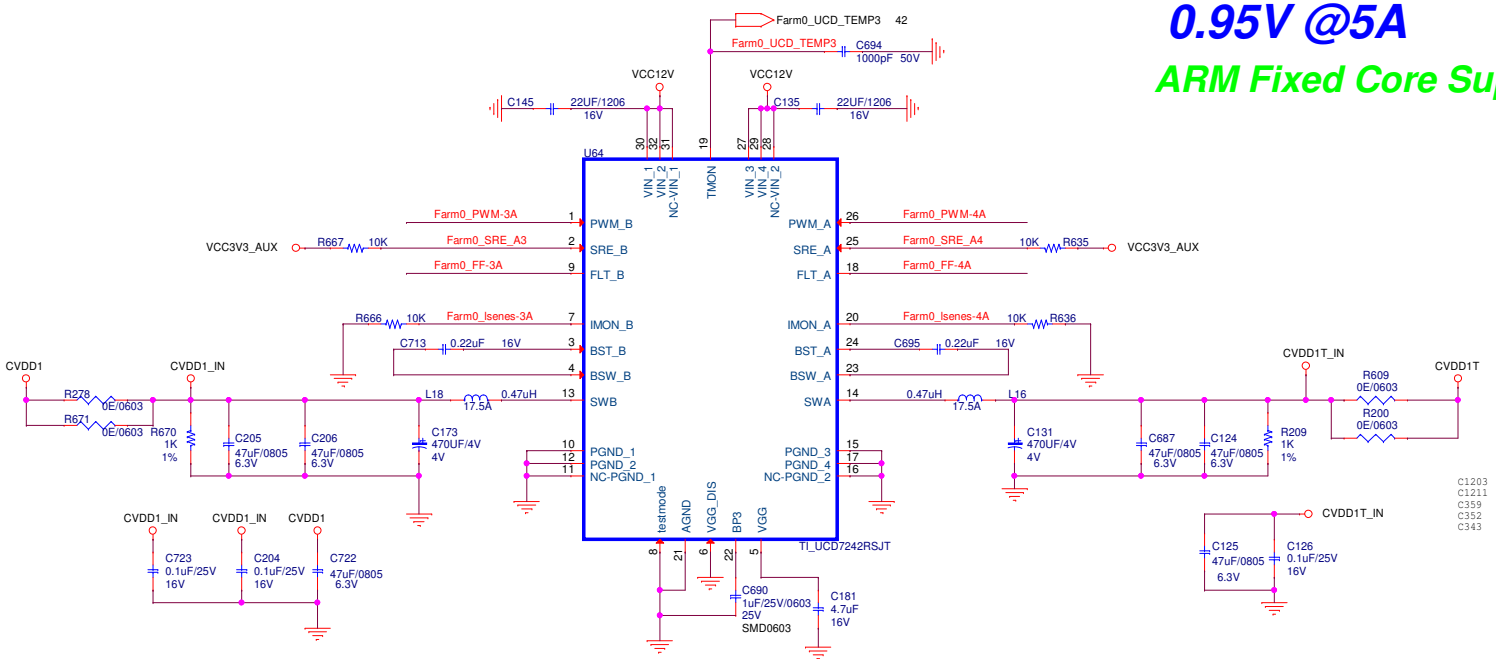
Title: <Title>			
Size: A3	Document Number: <Doc>		Rev: <RevCode>
Date: Wednesday, September 25, 2019	Sheet 7 of 50		


VCC3V3_AUX
B37
2200pF
0.7A
C645
0.1uF/25V
16V
16V_X7R
C666
0.1uF/25V
16V_X7R
C667
0.1uF/25V
16V_X7R
C117
2.2UF/0402/10V
6.3V
VCC12V
R529
10.2K
1%
C665
1uF/6.3V
6.3V
BPCAP
Farm0_UCD_VIN
VinMon
C63
1000pF
50V
R85
1.5K
1%
C644
1000pF
50V
Farm0_UCD_TEMP1
C646
1000pF
50V
Farm0_UCD_TEMP2
C648
1000pF
50V
Farm0_UCD_TEMP3
Temp1/AuxADC1
Temp2/AuxADC2
Temp3/AuxADC3
Temp4/AuxADC4
Farm0_UCD_EAP1
R165
750E 1%
C106
560pF 50V
R166
NL/2K 1%
Farm0_UCD_EAN1
EAp1
EAn1
Farm0_UCD_EAP2
R148
750E 1%
C102
560pF 50V
R147
NL/2K 1%
Farm0_UCD_EAN2
EAp2
EAn2
Farm0_UCD_EAP3
R132
750E 1%
C100
560pF 50V
R141
NL/2K 1%
Farm0_UCD_EAN3
EAp3
EAn3
Farm0_UCD_EAP4
R123
750E 1%
C94
560pF 50V
R122
NL/2K 1%
Farm0_UCD_EAN4
EAp4
EAn4
Close to UCD9244
TP16
JTAG_RCK
TP22
SYNC_IN/JTAG_TDI
R174
4.7K 1%
JTAG_TRST
PMBUS Address = 4Eh (78d)
R540
100K 1%
R548
100K 1%
Addr0
Addr1
VCC3V3_AUX
R119
1.3K 1%
CVDD_PWR_OK
Power_Good
PMBUS_CLK
PMBUS_DAT
PMBUS_ALERT
HEAD_UCD_CNTRL_L
PMBUS_CLK
PMBUS_DATA
PMBUS_ALERT
PMBUS_CNTRL
UCD9244_EN
IN
R144
1%
1K
VCC3V3_AUX
R142
10K 1%
R568
1%
1M/0603
VCC3V3_AUX
R84
1K 1%
RESET
With 75K resistor for the ADR, the PM Bus address is 0x34 (52d)
With 100K resistor for the ADR, the PM Bus address is 0x4E (78d)
U13
V33FB
V33D
V33A
V33DIO1
V33DIO2
TI_UCD9244MRGCTEP
FLT1A
DPWM1A
CS1A
Farm0_FF-1A_L
Farm0_PWM-1A
R538
100E 1%
Farm0_Isenes-1A
C91
0.01uF 16V
R103
4.99K 1%
FLT2A
DPWM2A
CS2A
Farm0_FF-2A_L
Farm0_PWM-2A_L
R82
100E 1%
Farm0_Isenes-2A
C628
0.01uF 16V
R530
4.99K 1%
FLT3A
DPWM3A
CS3A
Farm0_FF-3A_L
Farm0_PWM-3A
R79
100E 1%
Farm0_Isenes-3A
C627
0.01uF 16V
R77
NL/4.99K 1%
FLT4A
DPWM4A
CS4A
Farm0_FF-4A_L
Farm0_PWM-4A
R78
100E 1%
Farm0_Isenes-4A
C624
0.01uF 16V
R528
NL/4.99K 1%
RE
R83
0E/DNL
Farm0_FF-1A
C625
NL/0.1uF
16V
RD
R81
0E/DNL
Farm0_FF-2A
C626
NL/0.1uF
16V
R125
0E
Farm0_FF-3A
C655
NL/0.1uF
16V
R175
0E
Farm0_FF-4A
C678
NL/0.1uF
16V
VID1A
VID1B
VID1C
VID1S
DSP_UCD9244_VID1A
DSP_UCD9244_VID1B
DSP_UCD9244_VID1C
DSP_UCD9244_VID1S
VID2A
VID2B
VID2C
VID2S
ARM_UCD9244_VID2A
ARM_UCD9244_VID2B
ARM_UCD9244_VID2C
ARM_UCD9244_VID2S
VID3A
VID3B
VID3C
VID3S
R176
4.7K 1%
VCC3V3_AUX
VID4A/JTAG_TCK
VID4B/JTAG_TDO
VID4C/JTAG_TMS
VID4S
R177
4.7K 1%
VCC3V3_AUX
DGND1
DGND2
DGND3
AGND1
AGND2
AGND3
PowerPad
Thermal_VIA1
Thermal_VIA2
Thermal_VIA3
Thermal_VIA4
Thermal_VIA5
Thermal_VIA6
Thermal_VIA7
Thermal_VIA8
Thermal_VIA9
Thermal_VIA10
Thermal_VIA11
Thermal_VIA12
Thermal_VIA13
Thermal_VIA14
Thermal_VIA15
Thermal_VIA16
Thermal_VIA17
Thermal_VIA18
Thermal_VIA19
Thermal_VIA20
Thermal_VIA21
Thermal_VIA22
Thermal_VIA23
Thermal_VIA24
Thermal_VIA25
Farm0_PWM-1A
R102
0E
Farm0_PWM-2A_L
R108
0E/DNL
Farm0_PWM-1A
Farm0_PWM-2A
Farm0_PWM-3A
Farm0_PWM-4A
Farm0_FF-1A
Farm0_FF-2A
Farm0_FF-3A
Farm0_FF-4A
Farm0_Isenes-1A
Farm0_Isenes-2A
Farm0_Isenes-3A
Farm0_Isenes-4A
Farm0_UCD_EAP1
Farm0_UCD_EAN1
Farm0_UCD_EAP2
Farm0_UCD_EAN2
Farm0_UCD_EAP3
Farm0_UCD_EAN3
Farm0_UCD_EAP4
Farm0_UCD_EAN4
Farm0_UCD_TEMP1
Farm0_UCD_TEMP2
Farm0_UCD_TEMP3
DSP_UCD9244_VID1A
DSP_UCD9244_VID1B
DSP_UCD9244_VID1C
DSP_UCD9244_VID1S
ARM_UCD9244_VID2A
ARM_UCD9244_VID2B
ARM_UCD9244_VID2C
ARM_UCD9244_VID2S
UA
VCC3V3_AUX
U58
Farm0_FF-1A
Farm0_FF-2A
Farm0_FF-1A_L
TI_SN74LVC1G32DCK
<Characteristic>
RC
R80
10E
5%
CVDD_PWR_OK
UCD9244_EN
CVDD_PWR_OK
UCD9244_EN
PMBUS_ALERT
PMBUS_DAT
PMBUS_CLK
PMBUS_ALERT
PMBUS_DAT
PMBUS_CLK
CVDD
GND
10 ohm
EAP1
EAN1
750 ohm
470 pF
EAp1
EAn1
CVDD
GND
EAP2
EAN2
EAp2
EAn2
CVDD1
GND
EAP3
EAN3
EAp2
EAn2
CVDD1T
GND
EAP4
EAN4
EAp2
EAn2
UCD9244
Series resistors on EA nets to be placed at the load for proper voltage feedback.
HEAD_UCD_CNTRL_L
D20
NL/SBU05U20LPS-7
0.5A
CVDD_PWR_OK
Title
<Title>
Size
A3
Document Number
<Doc>
Rev
<RevCode>
Date:
Wednesday, September 25, 2019
Sheet
8
of
50


SOC DSP Vcore @20A
Note: U90 & U53 device are in parallel connection as per requirements
TI_UCD74120
TI_UCD74120RVF
<Characteristic>
VCC12V
VCC3V3_AUX
Farm0_PWM-1A
Farm0_FF-1A
Farm0_Isenes-1A
Farm0_SRE_A1
Farm0_ILIM1
Farm0_RDLY1
Farm0_AVGG1
Farm0_VGG1
Farm0_SW_Shape1
Farm0_CSP1
Farm0_CSN1
Farm0_VGG1
C347 22UF/1206 16V
C760 0.1uF/25V 16V
C385 0.22uF/0603 25V
L19 0.2uH 24A
R314 2.2E/0805 5%_1/8W
R319 1.3K 1%
C399 0.1uF/25V 16V
R332 931E 1%
R318 0E
C373 330pF 50V
C430 4.7uF 16V
C283 470UF/4V 4V
C739 220uF 4V
C284 1000uF 2.5V
C746 47uF/0805 6.3V
C300 47uF/0805 6.3V
C737 220uF 4V
C738 220uF 4V
C747 47uF/0805 6.3V
C299 47uF/0805 6.3V
R672 1K 1%
TP43
CVDD_INA
CVDD
R283 0E/0603
R282 0E/0603
Note: Should be placed underneath inductor of associated power stage
Q4
MICROCHIP_MCP9700AT-E/LT
C376 0.1uF/25V 16V
Farm0_UCD_TEMP1
Farm0_UCD_EAP1
Farm0_UCD_EAN1
R240 10E 5%
R235 10E 5%
Series resistors on EA nets to be placed at the load for proper voltage feedback.
Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails
Title
<Title>
Size A3
Document Number
<Doc>
Rev
<RevCode>
Date: Wednesday, September 25, 2019
Sheet 9 of 50


SOC ARM Vcore @6A
VCC12V
C375
22UF/1206
16V
U71
TI_UCD74120
TI_UCD74120RVF
<Characteristic>
Farm0_PWM-2A
VCC3V3_AUX
R341
10K
Farm0_SRE_A2
Farm0_FF-2A
Farm0_Isenes-2A
C765
1uF/25V/0603
25V
C426
0.01uF
16V
R692
10K
R687
22.6K/0603
1%
Farm0_ILIM2
R691
8.06K
1%
Farm0_RDLY2
C775
0.1uF/25V
16V
Farm0_AVGG2
FARM0_VGG2
R693
2E
PWM
SRE
FLT
IMON
SRE_MD
BP3
ILIM
RDLY
AVGG
Thermal_PAD
Thermal_via1
Thermal_via2
Thermal_via3
Thermal_via4
Thermal_via5
Thermal_via6
Thermal_via7
Thermal_via8
Thermal_via9
Thermal_via10
Thermal_via11
Thermal_via12
Thermal_via13
Thermal_via14
Thermal_via15
Thermal_via16
Thermal_via17
Thermal_via18
Thermal_via19
Thermal_via20
Thermal_via21
NC_3
NC_2
NC_1
VIN_6
VIN_5
VIN_4
VIN_3
VIN_2
VIN_1
VDD
HS_SNS
BOOT
SW_1
SW_2
SW_3
SW_4
SW_5
SW_6
CSP
CSN
VGG
PGND_1
PGND_2
PGND_3
PGND_4
PGND_5
PGND_6
PGND_7
PGND_8
AGND
VGG_DIS
C761
0.1uF/25V
16V
R323
2K
R685
10E
C386
0.22uF/0603
25V
FARM0_SW_Shape2
FARM0_CSP2
FARM0_CSN2
FARM0_VGG2
R355
2.49K
1%
R356
2.49K
1%
C432
4.7uF
16V
R315
2.2E/0805
5%_1/8W
C374
330pF
50V
0.47uH
17.5A
L20
R331
1.3K/0603
1%
C414
0.1uF/0603
50V
R336
931E
1%
R330
0E/0603
C286
1000uF
2.5V
C288
470UF/4V
4V
C743
47uF/0805
6.3V
C742
47uF/0805
6.3V
R291
1K
1%
C297
47uF/0805
6.3V
C741
47uF/0805
6.3V
C745
47uF/0805
6.3V
C744
47uF/0805
6.3V
TP44
CVDD_INB
CVDD
R286
0E/0603
R284
0E/0603
R285
0E/0603
R287
0E/0603
Farm0_PWM-2A
Farm0_FF-2A
Farm0_Isenes-2A
IN
Farm0_UCD_EAP2
Farm0_UCD_EAN2
R218
10E 5%
R212
10E 5%
CVDD
Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails
Series resistors on EA nets to be placed at the load for proper voltage feedback.
Note: Should be placed underneath inductor of associated power stage
Q5
VDD
VOUT
NC1
NC2
GND
MICROCHIP_MCP9700AT-E/LT
C377
0.1uF/25V
16V
Farm0_UCD_TEMP2
42
Title
<Title>
Size
A3
Document Number
<Doc>
Rev
<RevCode>
Date:
Wednesday, September 25, 2019
Sheet
10
of
50

0.95V @5A
DSP Fixed Core Supply
0.95V @5A
ARM Fixed Core Supply



Note: Analog GND to same point

Farm0_PWM-3A IN Farm0_PWM-3A
Farm0_FF-3A IN Farm0_FF-3A
Farm0_Isenes-3A IN Farm0_Isenes-3A

Farm0_PWM-4A IN Farm0_PWM-4A
Farm0_FF-4A IN Farm0_FF-4A
Farm0_Isenes-4A IN Farm0_Isenes-4A

Farm0_UCD_EAP3 IN Farm0_UCD_EAP3 R292 10E 5% CVDD1
Farm0_UCD_EAN3 IN Farm0_UCD_EAN3 R293 10E 5%

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

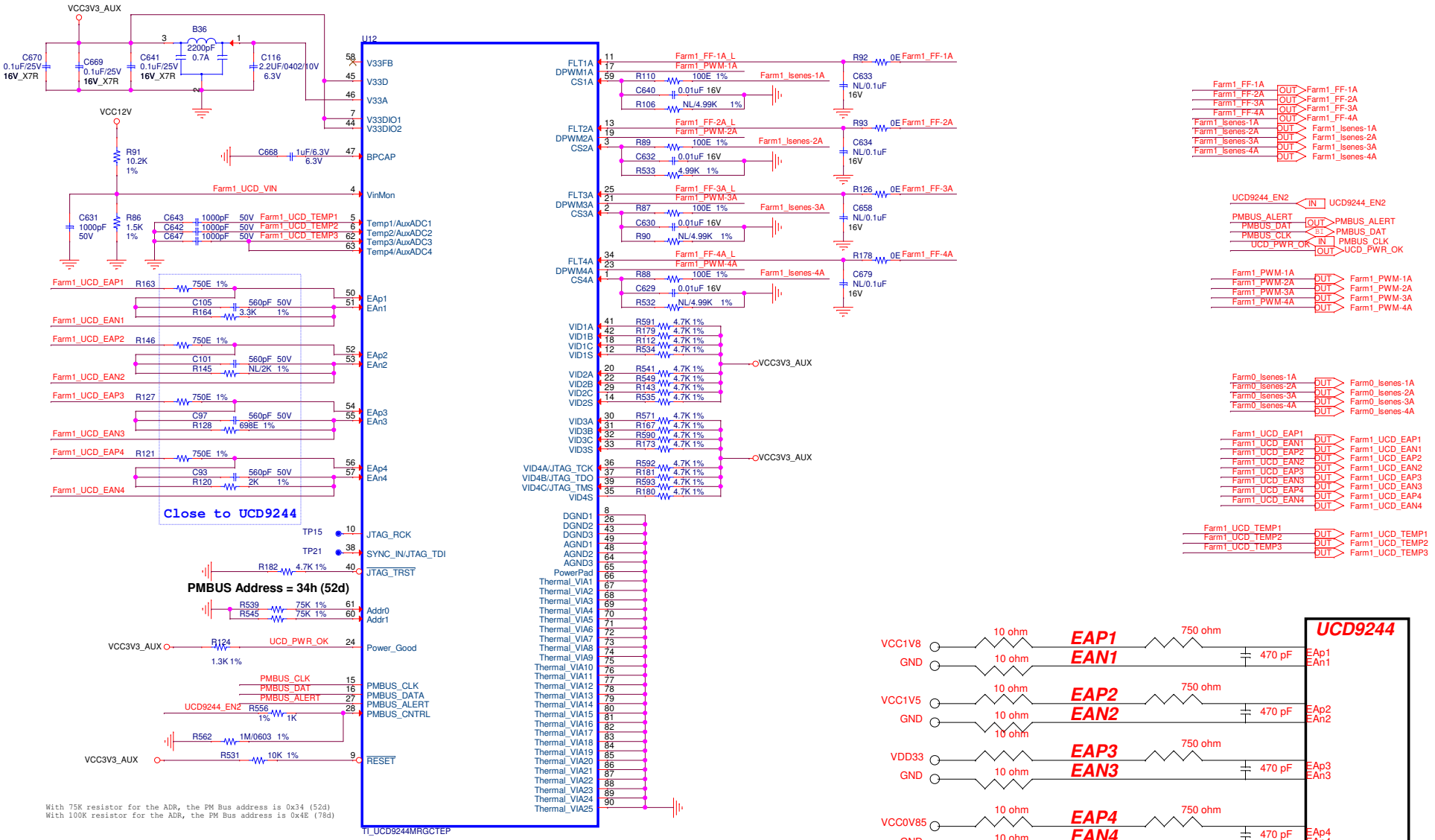
Series resistors on EA nets to be placed at the load for proper voltage feedback.

Farm0_UCD_EAP4 IN Farm0_UCD_EAP4 R204 10E 5% CVDD1T
Farm0_UCD_EAN4 IN Farm0_UCD_EAN4 R197 10E 5%

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

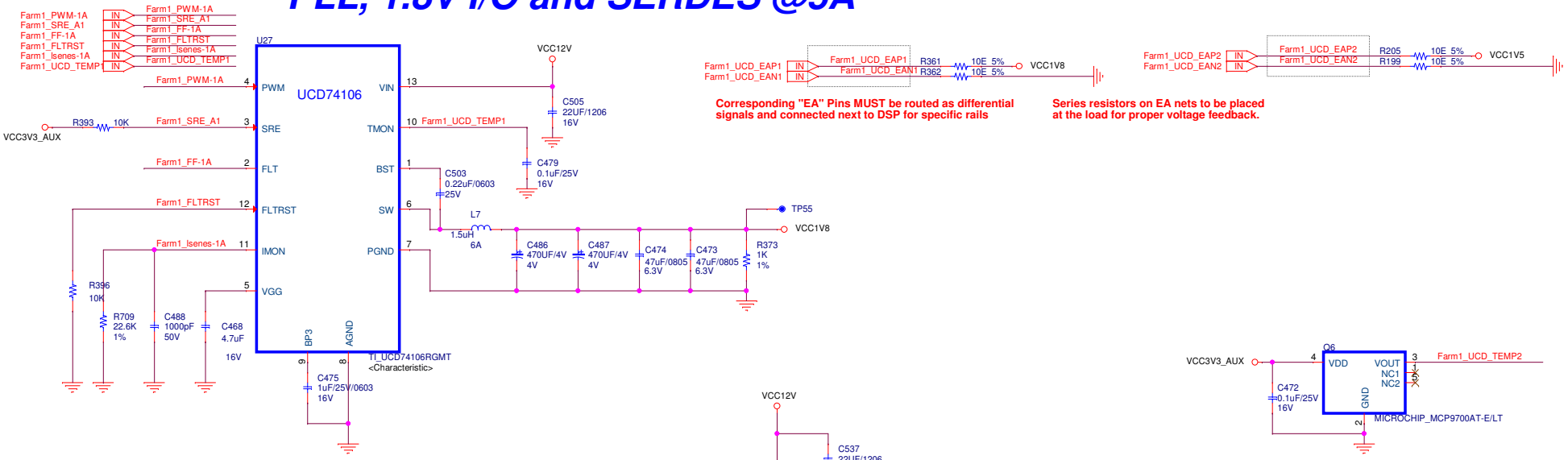
Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, September 25, 2019	Sheet 11 of 50	



Series resistors on EA nets to be placed at the load for proper voltage feedback.

Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, September 25, 2019	Sheet 12 of 50	

PLL, 1.8V I/O and SERDES @5A



Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

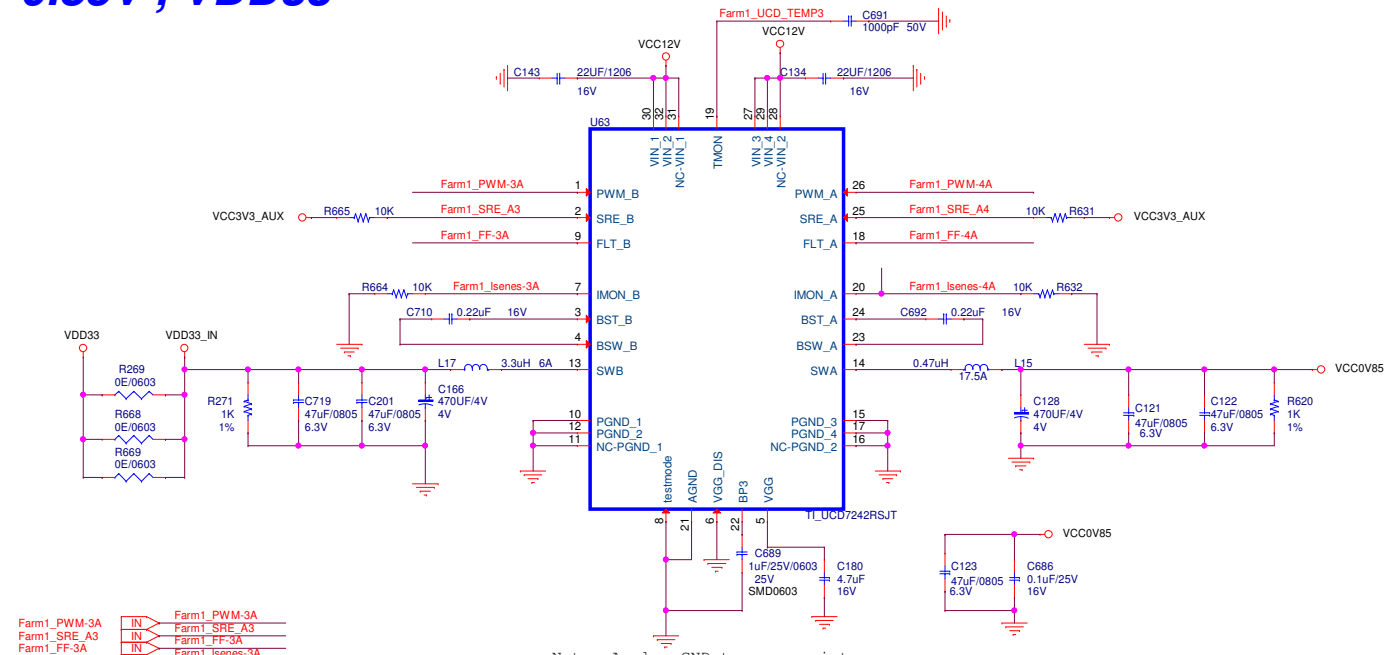
Series resistors on EA nets to be placed at the load for proper voltage feedback.

Note: Should be placed underneath inductor of associated power stage

DDR3 1.5V@12.5A

Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCode>
Date: Wednesday, September 25, 2019		Sheet 13 of 50	

SOC USB and SERDES
0.85V , VDD33



Note: Analog GND to same point

Farm1_PWM-3A IN Farm1_PWM-3A
Farm1_SRE_A3 IN Farm1_SRE_A3
Farm1_FF-3A IN Farm1_FF-3A
Farm1_Isenes-3A IN Farm1_Isenes-3A
Farm1_PWM-4A IN Farm1_PWM-4A
Farm1_SRE_A4 IN Farm1_SRE_A4
Farm1_FF-4A IN Farm1_FF-4A
Farm1_Isenes-4A IN Farm1_Isenes-4A
Farm1_UCD_TEMP3 IN Farm1_UCD_TEMP3

Farm1_UCD_EAP3 IN Farm1_UCD_EAP3 R345 10E 5% VDD33
Farm1_UCD_EAN3 IN Farm1_UCD_EAN3 R337 10E 5%

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

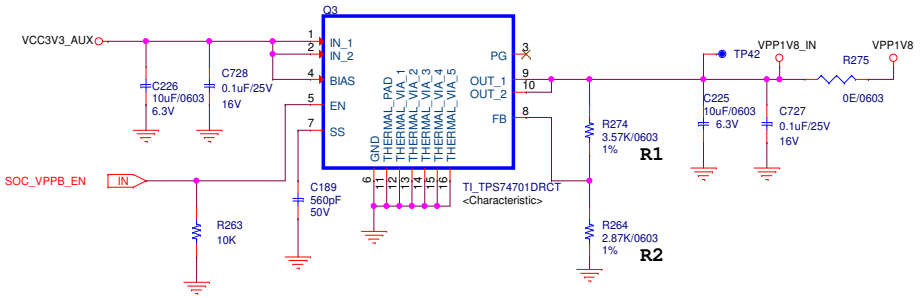
Farm1_UCD_EAP4 IN Farm1_UCD_EAP4 R326 10E 5% VCC0V85
Farm1_UCD_EAN4 IN Farm1_UCD_EAN4 R317 10E 5%

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, September 25, 2019	Sheet 14 of 50	

VPP1V8



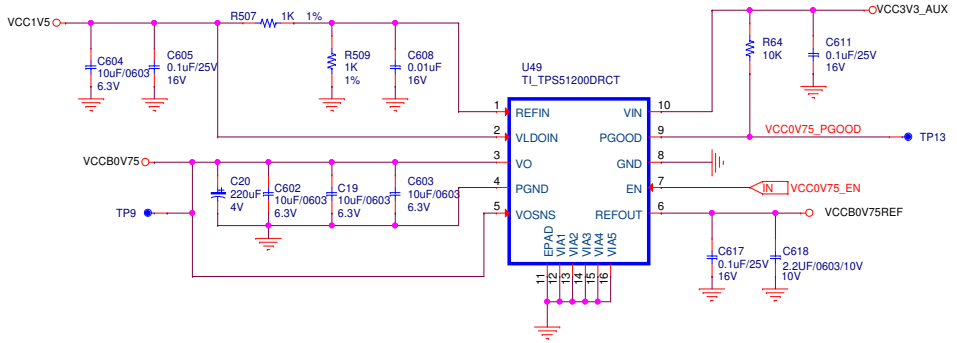
Vout=0.8*(1+R1/R2)

1.79512V =0.8*(1+3.57k/2.87k)

Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, September 25, 2019	Sheet 15 of 50	

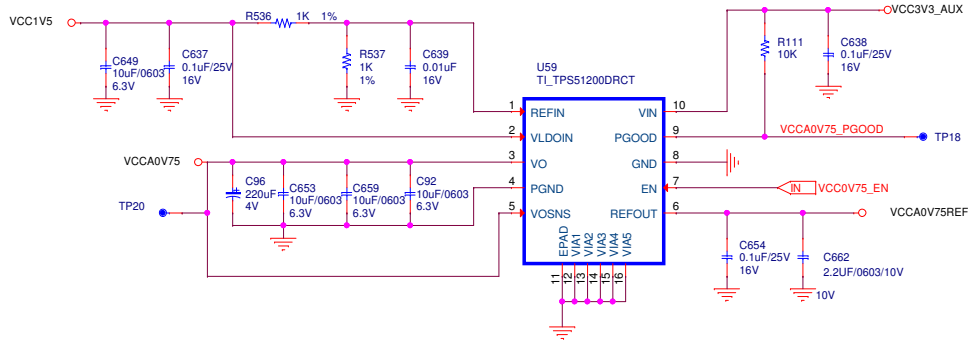
VCCB0V75

DDR3-1600
DiscreteSDRAM ArrayI



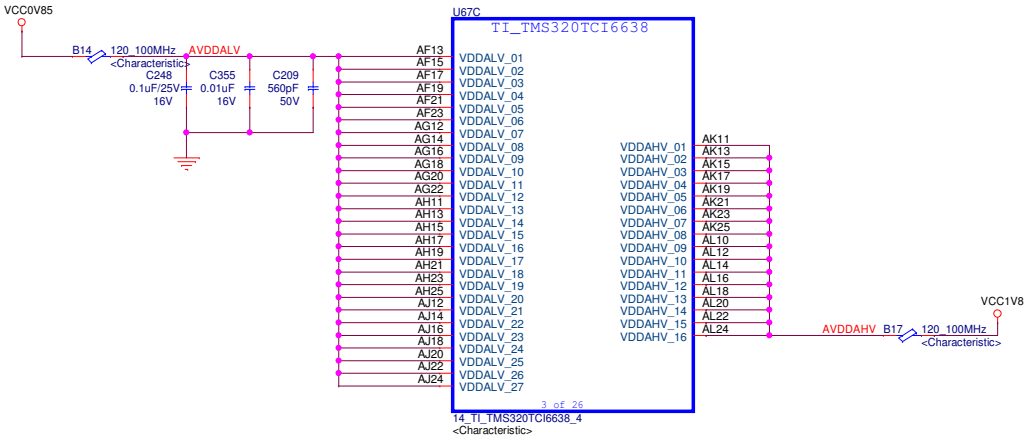
VCCA0V75

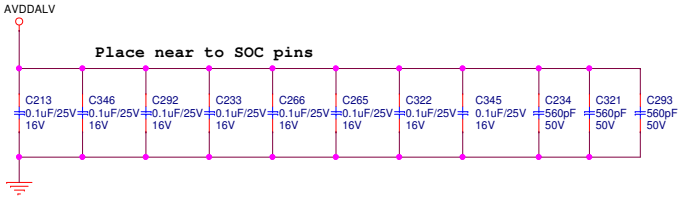
For DDR3-1600 SO-DIMM

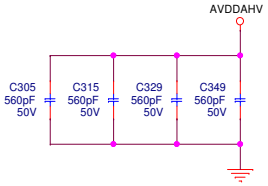


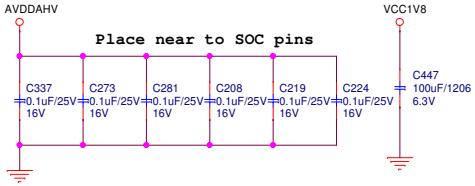
Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, September 25, 2019	Sheet 16 of 50	

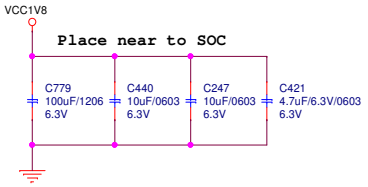
Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, September 25, 2019	Sheet 17 of 50	

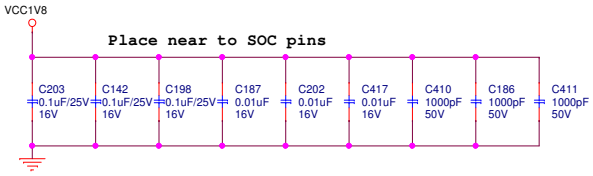


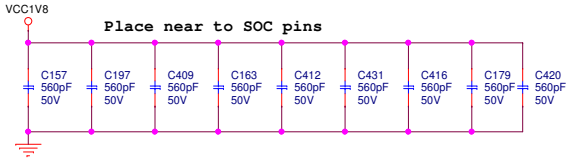


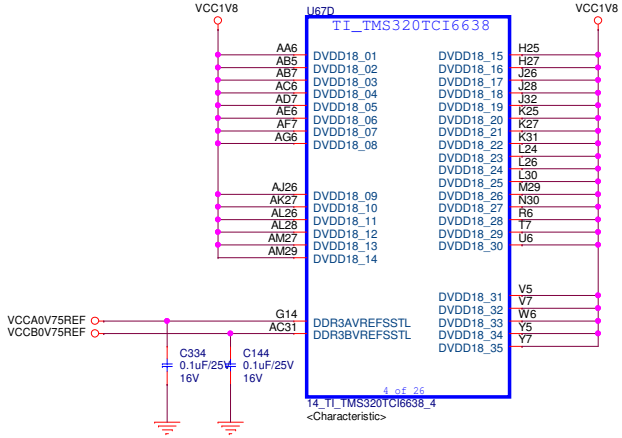




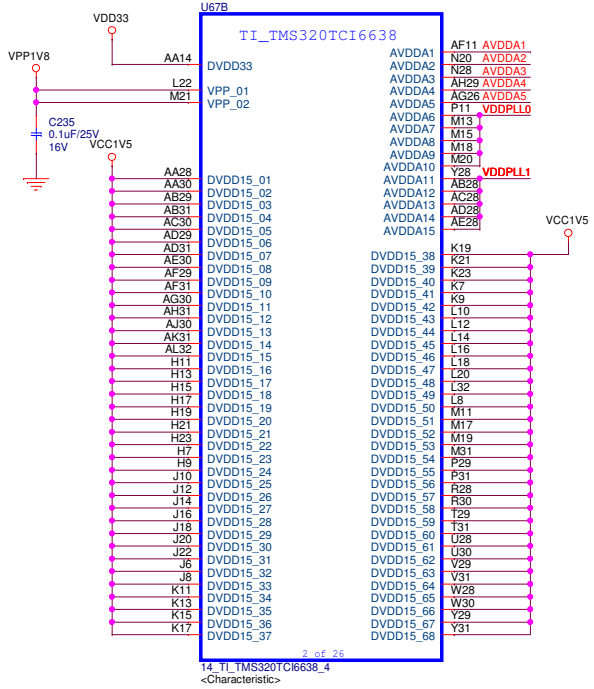


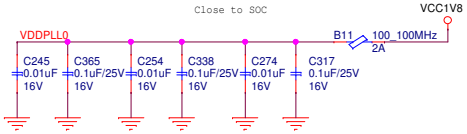


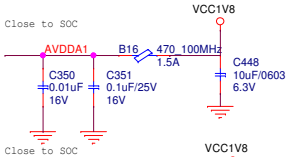


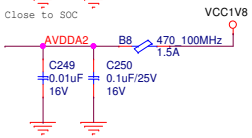


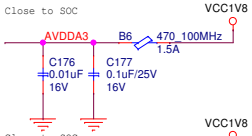
Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, September 25, 2019	Sheet 18 of 50	

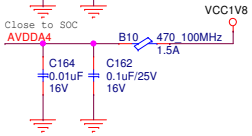


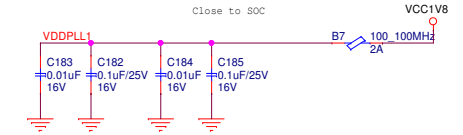


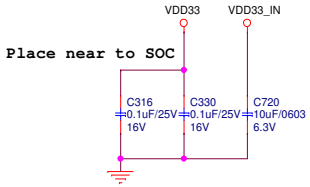


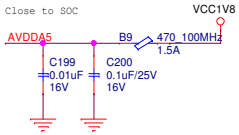


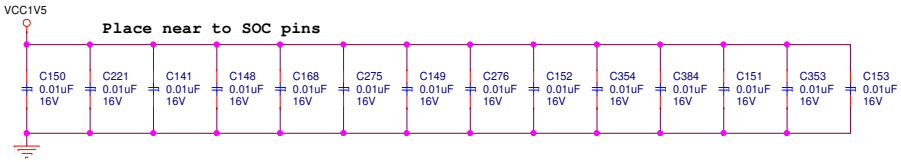


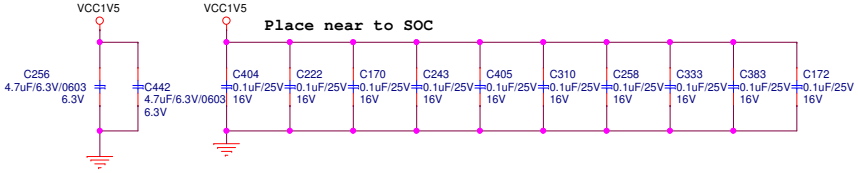


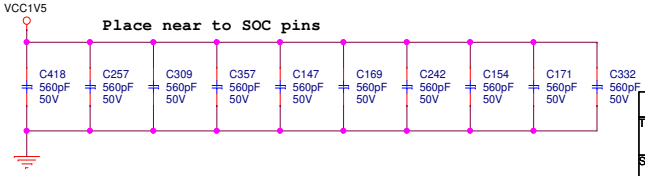




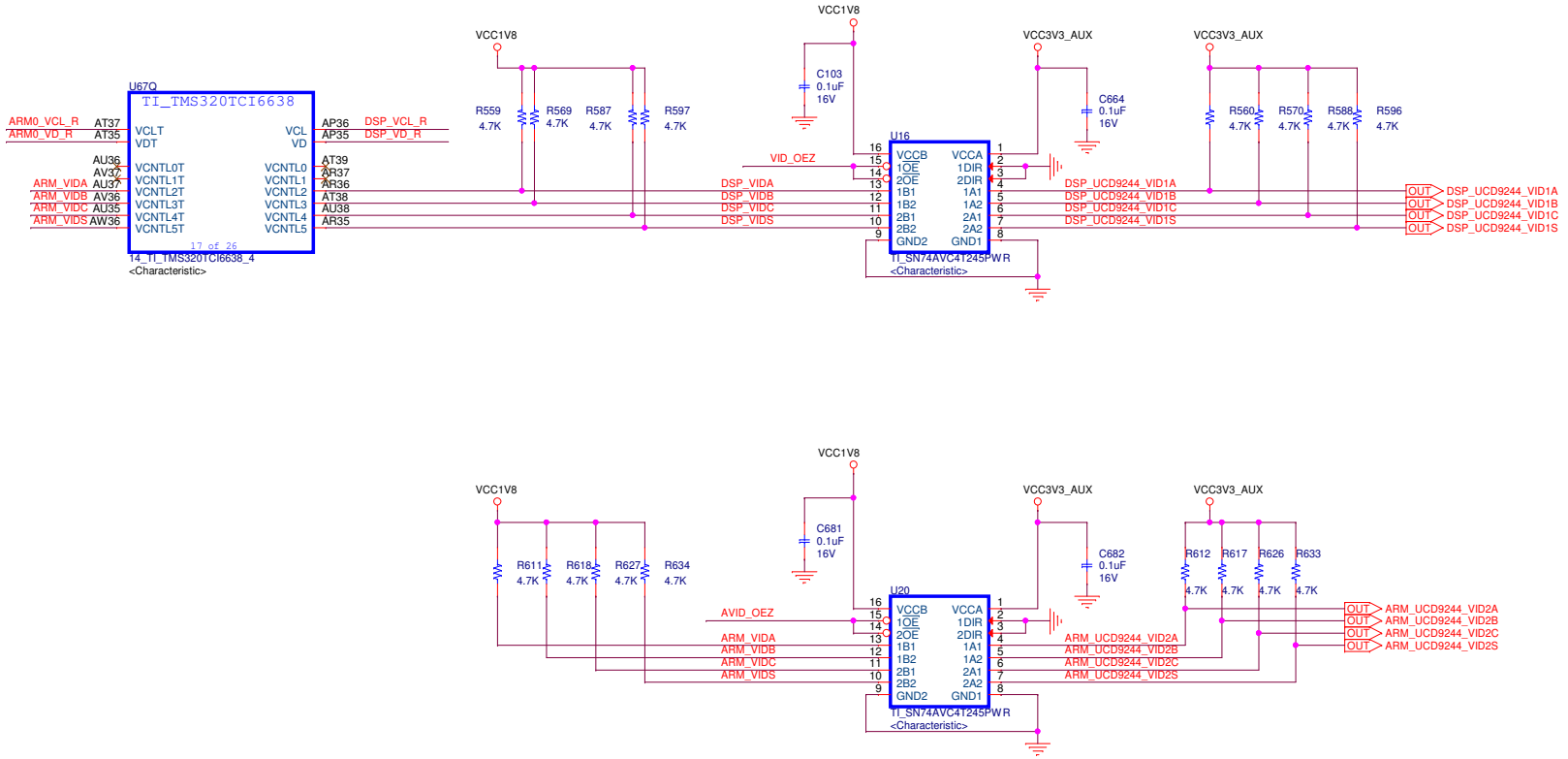




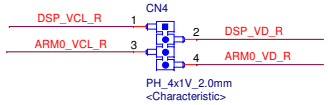




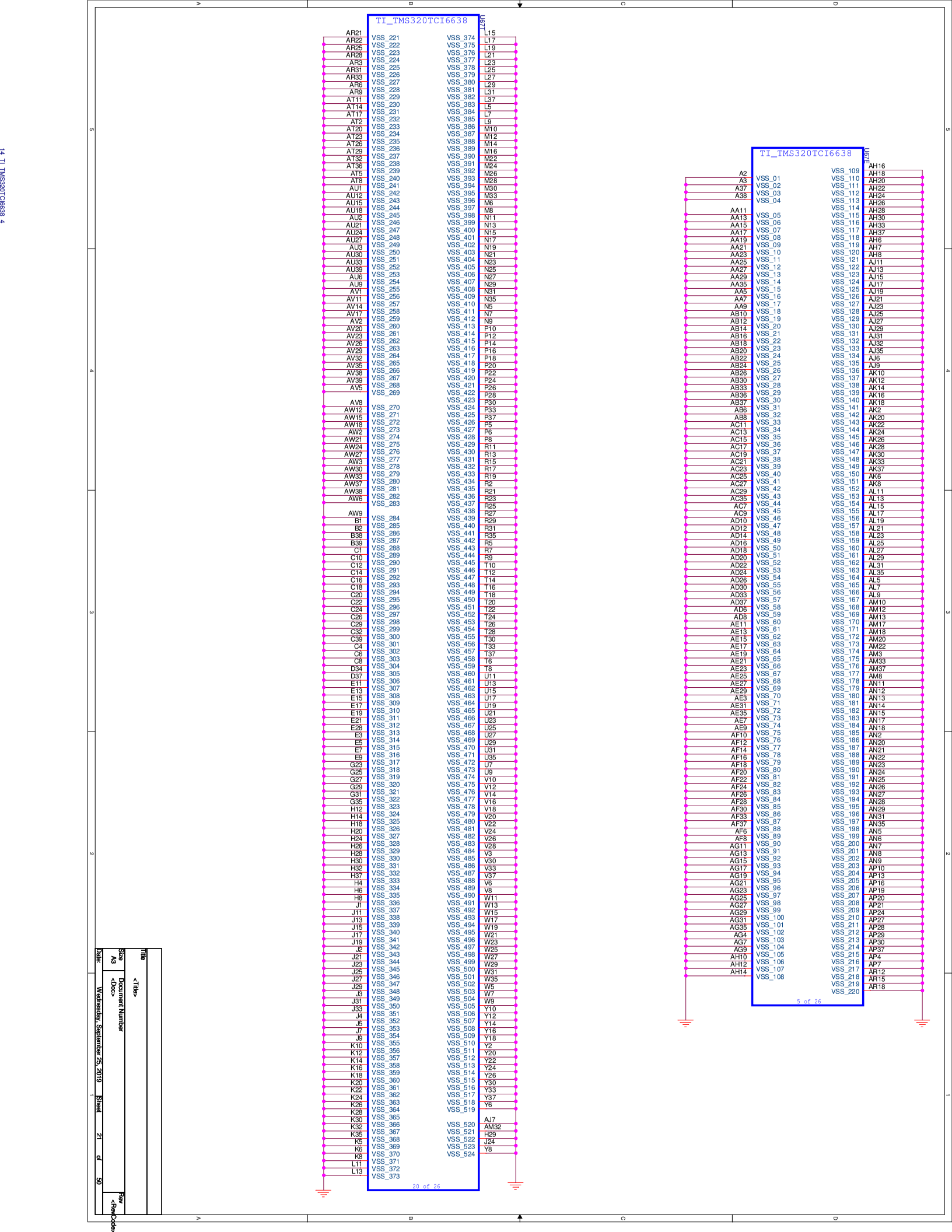
Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, September 25, 2019	Sheet 19 of 50	



4-pin header for Smart Reflex signal measuring



Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCode>
Date: Wednesday, September 25, 2019		Sheet 20 of 50	


TI_TMS320TCI6638
U62J
AR21 AR22 AR25 AR28 AR3 AR31 AR33 AR6 AR9 AT11 AT14 AT17 AT2 AT20 AT23 AT26 AT29 AT32 AT36 AT5 AT8 AU1 AU12 AU15 AU18 AU2 AU21 AU24 AU27 AU3 AU30 AU33 AU39 AU6 AU9 AV1 AV11 AV14 AV17 AV2 AV20 AV23 AV26 AV29 AV32 AV35 AV38 AV39 AV5 AV8 AW12 AW15 AW18 AW2 AW21 AW24 AW27 AW3 AW30 AW33 AW37 AW38 AW6 AW9 B1 B2 B38 B39 C1 C10 C12 C14 C16 C18 C20 C22 C24 C26 C29 C32 C39 C4 C6 C8 D34 D37 E11 E13 E15 E17 E19 E21 E28 E3 E5 E7 E9 G23 G25 G27 G29 G31 G35 H12 H14 H18 H20 H24 H26 H28 H30 H32 H37 H4 H6 H8 J1 J11 J13 J15 J17 J19 J2 J21 J23 J25 J27 J29 J3 J31 J33 J4 J5 J7 J9 K10 K12 K14 K16 K18 K20 K22 K24 K26 K28 K30 K32 K35 K5 K6 K8 L11 L13
VSS_221 VSS_222 VSS_223 VSS_224 VSS_225 VSS_226 VSS_227 VSS_228 VSS_229 VSS_230 VSS_231 VSS_232 VSS_233 VSS_234 VSS_235 VSS_236 VSS_237 VSS_238 VSS_239 VSS_240 VSS_241 VSS_242 VSS_243 VSS_244 VSS_245 VSS_246 VSS_247 VSS_248 VSS_249 VSS_250 VSS_251 VSS_252 VSS_253 VSS_254 VSS_255 VSS_256 VSS_257 VSS_258 VSS_259 VSS_260 VSS_261 VSS_262 VSS_263 VSS_264 VSS_265 VSS_266 VSS_267 VSS_268 VSS_269 VSS_270 VSS_271 VSS_272 VSS_273 VSS_274 VSS_275 VSS_276 VSS_277 VSS_278 VSS_279 VSS_280 VSS_281 VSS_282 VSS_283 VSS_284 VSS_285 VSS_286 VSS_287 VSS_288 VSS_289 VSS_290 VSS_291 VSS_292 VSS_293 VSS_294 VSS_295 VSS_296 VSS_297 VSS_298 VSS_299 VSS_300 VSS_301 VSS_302 VSS_303 VSS_304 VSS_305 VSS_306 VSS_307 VSS_308 VSS_309 VSS_310 VSS_311 VSS_312 VSS_313 VSS_314 VSS_315 VSS_316 VSS_317 VSS_318 VSS_319 VSS_320 VSS_321 VSS_322 VSS_323 VSS_324 VSS_325 VSS_326 VSS_327 VSS_328 VSS_329 VSS_330 VSS_331 VSS_332 VSS_333 VSS_334 VSS_335 VSS_336 VSS_337 VSS_338 VSS_339 VSS_340 VSS_341 VSS_342 VSS_343 VSS_344 VSS_345 VSS_346 VSS_347 VSS_348 VSS_349 VSS_350 VSS_351 VSS_352 VSS_353 VSS_354 VSS_355 VSS_356 VSS_357 VSS_358 VSS_359 VSS_360 VSS_361 VSS_362 VSS_363 VSS_364 VSS_365 VSS_366 VSS_367 VSS_368 VSS_369 VSS_370 VSS_371 VSS_372 VSS_373
VSS_374 VSS_375 VSS_376 VSS_377 VSS_378 VSS_379 VSS_380 VSS_381 VSS_382 VSS_383 VSS_384 VSS_385 VSS_386 VSS_387 VSS_388 VSS_389 VSS_390 VSS_391 VSS_392 VSS_393 VSS_394 VSS_395 VSS_396 VSS_397 VSS_398 VSS_399 VSS_400 VSS_401 VSS_402 VSS_403 VSS_404 VSS_405 VSS_406 VSS_407 VSS_408 VSS_409 VSS_410 VSS_411 VSS_412 VSS_413 VSS_414 VSS_415 VSS_416 VSS_417 VSS_418 VSS_419 VSS_420 VSS_421 VSS_422 VSS_423 VSS_424 VSS_425 VSS_426 VSS_427 VSS_428 VSS_429 VSS_430 VSS_431 VSS_432 VSS_433 VSS_434 VSS_435 VSS_436 VSS_437 VSS_438 VSS_439 VSS_440 VSS_441 VSS_442 VSS_443 VSS_444 VSS_445 VSS_446 VSS_447 VSS_448 VSS_449 VSS_450 VSS_451 VSS_452 VSS_453 VSS_454 VSS_455 VSS_456 VSS_457 VSS_458 VSS_459 VSS_460 VSS_461 VSS_462 VSS_463 VSS_464 VSS_465 VSS_466 VSS_467 VSS_468 VSS_469 VSS_470 VSS_471 VSS_472 VSS_473 VSS_474 VSS_475 VSS_476 VSS_477 VSS_478 VSS_479 VSS_480 VSS_481 VSS_482 VSS_483 VSS_484 VSS_485 VSS_486 VSS_487 VSS_488 VSS_489 VSS_490 VSS_491 VSS_492 VSS_493 VSS_494 VSS_495 VSS_496 VSS_497 VSS_498 VSS_499 VSS_500 VSS_501 VSS_502 VSS_503 VSS_504 VSS_505 VSS_506 VSS_507 VSS_508 VSS_509 VSS_510 VSS_511 VSS_512 VSS_513 VSS_514 VSS_515 VSS_516 VSS_517 VSS_518 VSS_519 VSS_520 VSS_521 VSS_522 VSS_523 VSS_524
L15 L17 L19 L21 L23 L25 L27 L29 L31 L37 L5 L7 L9 M10 M12 M14 M16 M22 M24 M26 M28 M30 M33 M6 M8 N11 N13 N15 N17 N19 N21 N23 N25 N27 N29 N31 N35 N5 N7 N9 P10 P12 P14 P16 P18 P20 P22 P24 P26 P28 P30 P33 P37 P5 P6 P8 R11 R13 R15 R17 R19 R2 R21 R23 R25 R27 R29 R31 R35 R5 R7 R9 T10 T12 T14 T16 T18 T20 T22 T24 T26 T28 T30 T33 T37 T6 T8 U11 U13 U15 U17 U19 U21 U23 U25 U27 U29 U31 U35 U7 U9 V10 V12 V14 V16 V18 V20 V22 V24 V26 V28 V3 V30 V33 V37 V6 V8 W11 W13 W15 W17 W19 W21 W23 W25 W27 W29 W31 W35 W5 W7 W9 Y10 Y12 Y14 Y16 Y18 Y2 Y20 Y22 Y24 Y26 Y30 Y33 Y37 Y6 AJ7 AM32 H29 J24 Y8
20 of 26
TI_TMS320TCI6638
U62Z
A2 A3 A37 A38 AA11 AA13 AA15 AA17 AA19 AA21 AA23 AA25 AA27 AA29 AA35 AA5 AA7 AA9 AB10 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AB26 AB30 AB33 AB36 AB37 AB6 AB8 AC11 AC13 AC15 AC17 AC19 AC21 AC23 AC25 AC27 AC29 AC35 AC7 AC9 AD10 AD12 AD14 AD16 AD18 AD20 AD22 AD24 AD26 AD30 AD33 AD37 AD6 AD8 AE11 AE13 AE15 AE17 AE19 AE21 AE23 AE25 AE27 AE29 AE3 AE31 AE35 AE7 AE9 AF10 AF12 AF14 AF16 AF18 AF20 AF22 AF24 AF26 AF28 AF30 AF33 AF37 AF6 AF8 AG11 AG13 AG15 AG17 AG19 AG21 AG23 AG25 AG27 AG29 AG31 AG35 AG4 AG7 AG9 AH10 AH12 AH14
VSS_01 VSS_02 VSS_03 VSS_04 VSS_05 VSS_06 VSS_07 VSS_08 VSS_09 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99 VSS_100 VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108
VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128 VSS_129 VSS_130 VSS_131 VSS_132 VSS_133 VSS_134 VSS_135 VSS_136 VSS_137 VSS_138 VSS_139 VSS_140 VSS_141 VSS_142 VSS_143 VSS_144 VSS_145 VSS_146 VSS_147 VSS_148 VSS_149 VSS_150 VSS_151 VSS_152 VSS_153 VSS_154 VSS_155 VSS_156 VSS_157 VSS_158 VSS_159 VSS_160 VSS_161 VSS_162 VSS_163 VSS_164 VSS_165 VSS_166 VSS_167 VSS_168 VSS_169 VSS_170 VSS_171 VSS_172 VSS_173 VSS_174 VSS_175 VSS_176 VSS_177 VSS_178 VSS_179 VSS_180 VSS_181 VSS_182 VSS_183 VSS_184 VSS_185 VSS_186 VSS_187 VSS_188 VSS_189 VSS_190 VSS_191 VSS_192 VSS_193 VSS_194 VSS_195 VSS_196 VSS_197 VSS_198 VSS_199 VSS_200 VSS_201 VSS_202 VSS_203 VSS_204 VSS_205 VSS_206 VSS_207 VSS_208 VSS_209 VSS_210 VSS_211 VSS_212 VSS_213 VSS_214 VSS_215 VSS_216 VSS_217 VSS_218 VSS_219 VSS_220
AH16 AH18 AH20 AH22 AH24 AH26 AH28 AH30 AH33 AH37 AH6 AH7 AH8 AJ11 AJ13 AJ15 AJ17 AJ19 AJ21 AJ23 AJ25 AJ27 AJ29 AJ31 AJ32 AJ35 AJ6 AJ9 AK10 AK12 AK14 AK16 AK18 AK2 AK20 AK22 AK24 AK26 AK28 AK30 AK33 AK37 AK6 AK8 AL11 AL13 AL15 AL17 AL19 AL21 AL23 AL25 AL27 AL29 AL31 AL35 AL5 AL7 AL9 AM10 AM12 AM13 AM17 AM18 AM20 AM22 AM3 AM33 AM37 AM8 AN11 AN12 AN13 AN14 AN15 AN17 AN18 AN2 AN20 AN21 AN22 AN23 AN24 AN25 AN26 AN27 AN28 AN29 AN31 AN35 AN5 AN6 AN7 AN8 AN9 AP10 AP13 AP16 AP19 AP20 AP21 AP24 AP27 AP28 AP29 AP30 AP37 AP4 AP7 AR12 AR15 AR18
5 of 26
Title
<Title>
Size A3
Document Number <Doc>
Rev <RevCode>
Date: Wednesday, September 25, 2019
Sheet 21 of 50
14_TI_TMS320TCI6638_4