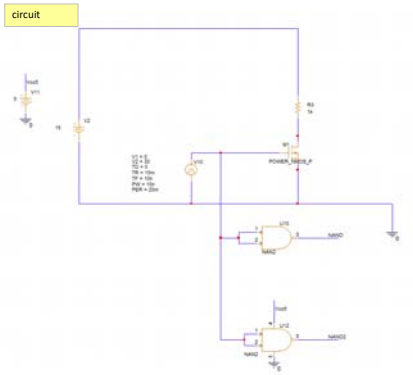
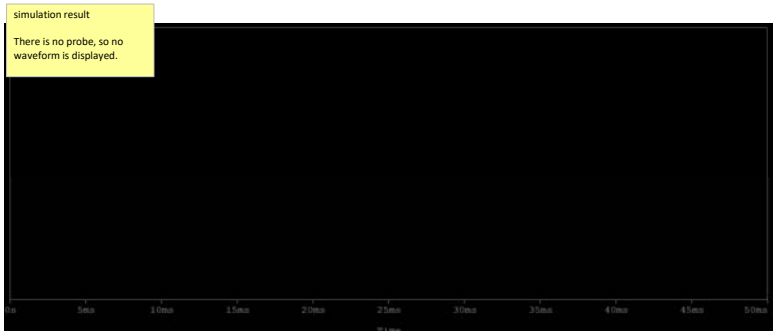
STEP1

circuit



simulation result

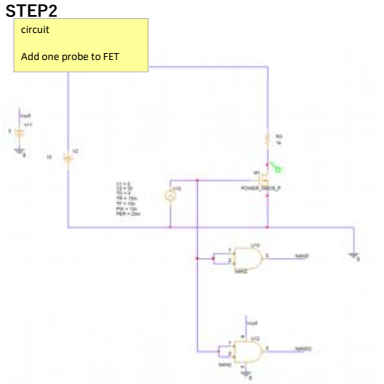
There is no probe, so no waveform is displayed.



STEP2

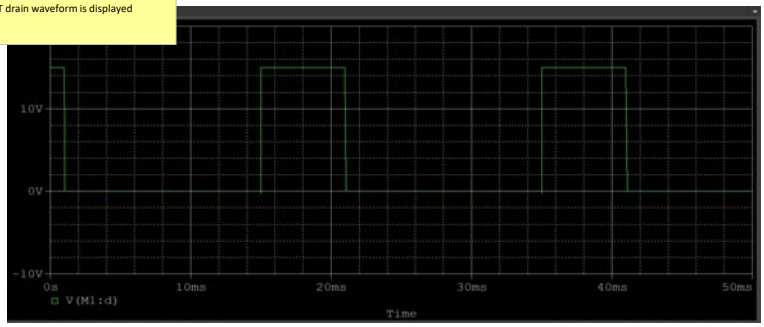
circuit

Add one probe to FET



simulation result

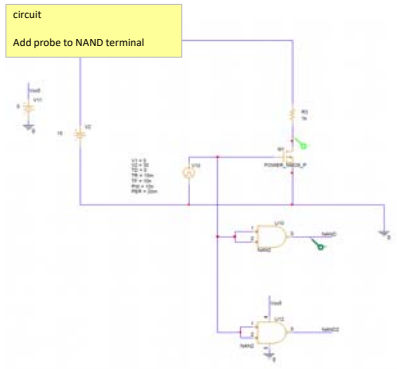
FET drain waveform is displayed



STEP 3

circuit

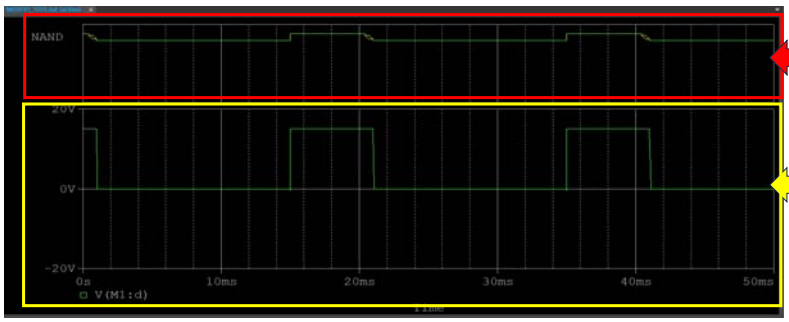
Add probe to NAND terminal



simulation result

The waveform of the NAND terminal is displayed in a separate frame.

question



1. Why is this frame displayed?
2. What does this table represent?

3.Why is the NAND terminal not displayed in this frame?