

IO LINK/BREAKOUT BOARD

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REV	E1
VER	0.4

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REVISION HISTORY

REV #	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.1	17-07-2020	INITIAL DRAFT	Mistral Design Team	RAKESH RAJDEV	AJIT MB
E1	0.2	03-09-2020	M12 connector parts changed, Level translators removed.	Mistral Design Team	RAKESH RAJDEV	AJIT MB
E1	0.3	15-09-2021	RELEASED FOR TI REVIEW	Mistral Design Team	RAKESH RAJDEV	AJIT MB
E1	0.4	29-09-2021	Rearranged Signals as per TI Review Comments	Mistral Design Team	RAKESH RAJDEV	AJIT MB

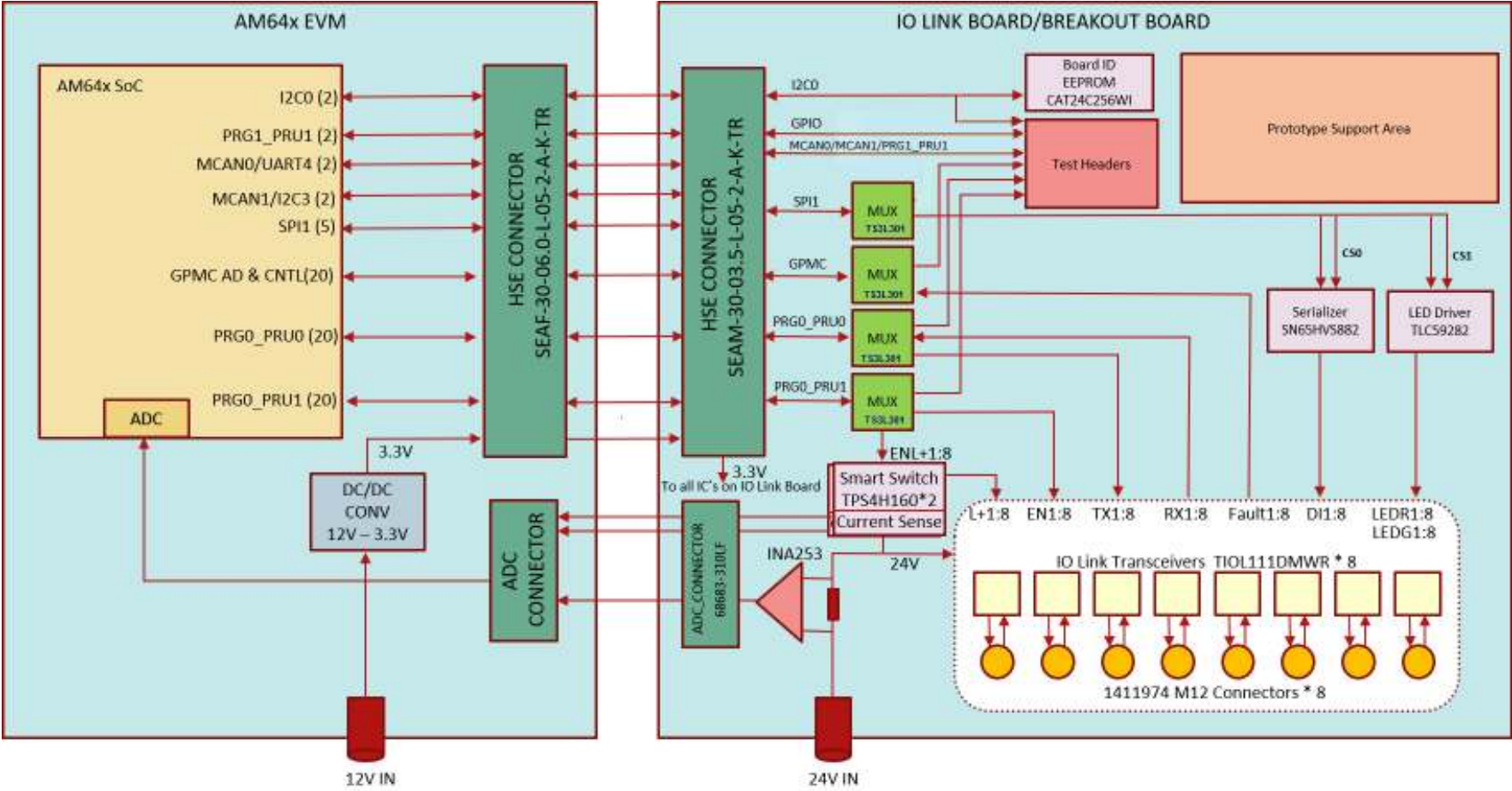
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BLOCK DIAGRAM



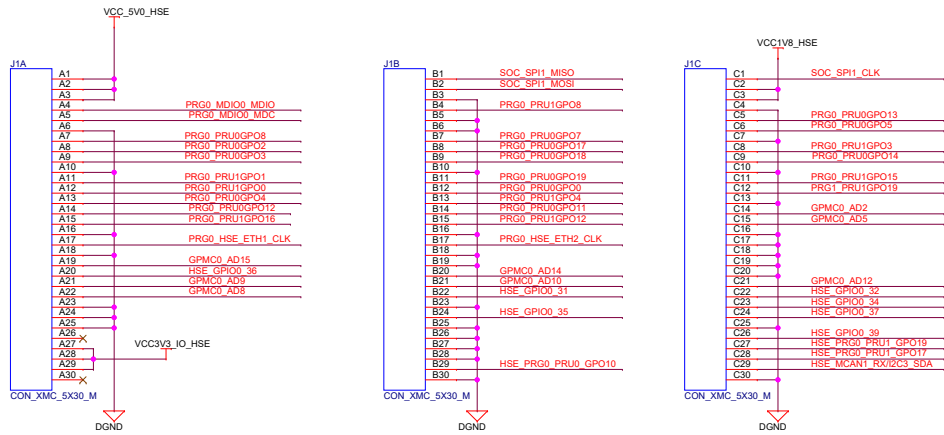
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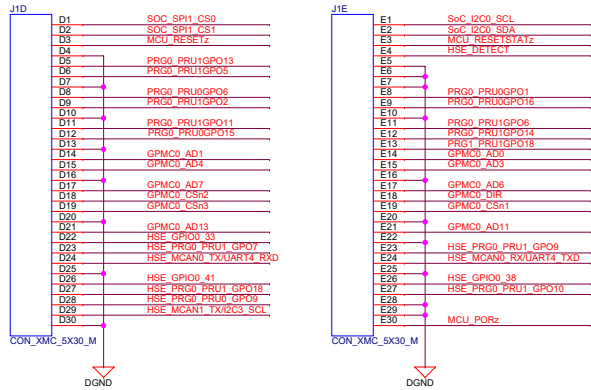
Title BLOCK DIAGRAM

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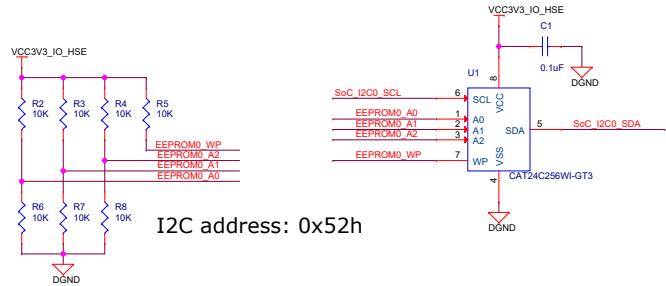
HSE CONNECTOR



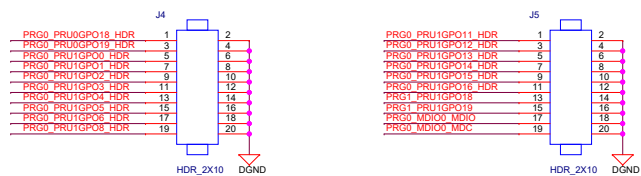
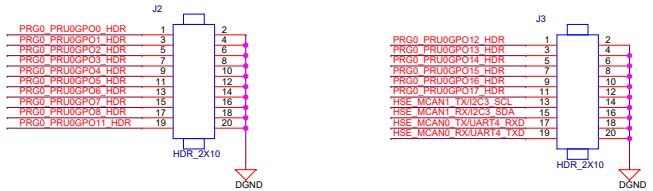
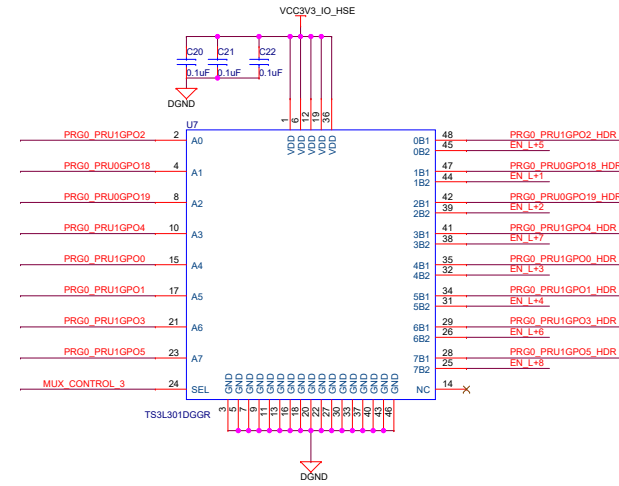
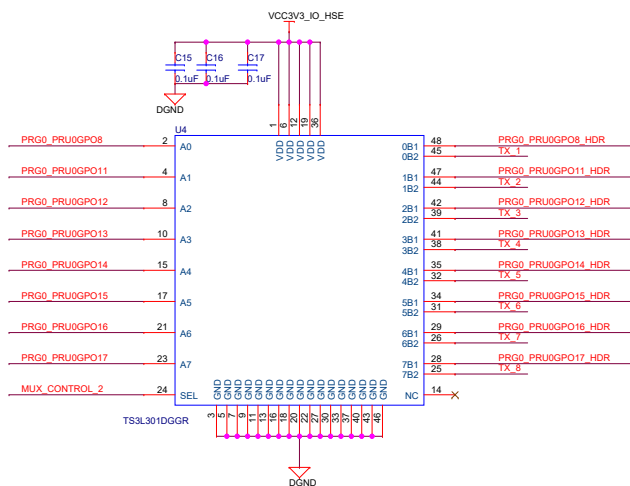
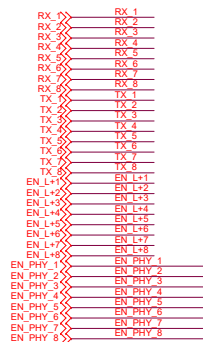
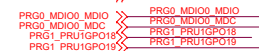
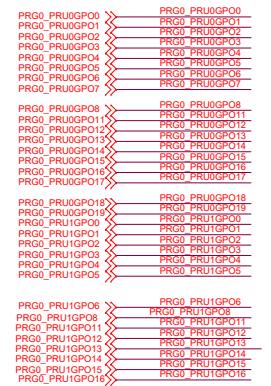
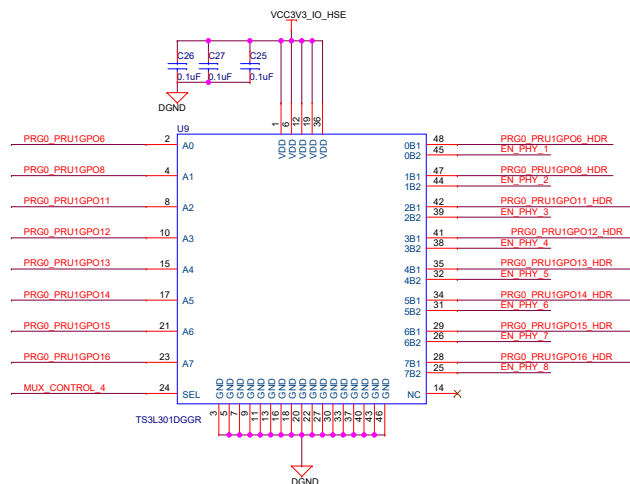
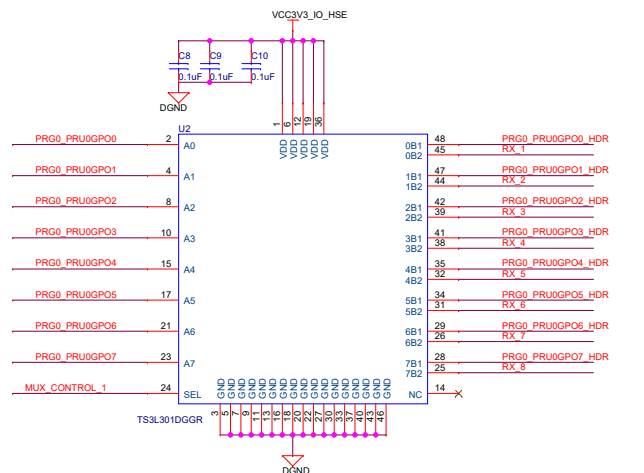
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PRG0_PRUIGP01	PRG0_PRUIGP01
PRG0_PRUIGP02	PRG0_PRUIGP02
PRG0_PRUIGP03	PRG0_PRUIGP03
PRG0_PRUIGP04	PRG0_PRUIGP04
PRG0_PRUIGP05	PRG0_PRUIGP05
PRG0_PRUIGP06	PRG0_PRUIGP06
PRG0_PRUIGP07	PRG0_PRUIGP07
PRG0_PRUIGP08	PRG0_PRUIGP08
PRG0_PRUIGP011	PRG0_PRUIGP011
PRG0_PRUIGP012	PRG0_PRUIGP012
PRG0_PRUIGP013	PRG0_PRUIGP013
PRG0_PRUIGP014	PRG0_PRUIGP014
PRG0_PRUIGP015	PRG0_PRUIGP015
PRG0_PRUIGP016	PRG0_PRUIGP016
PRG0_PRUIGP017	PRG0_PRUIGP017
PRG0_PRUIGP018	PRG0_PRUIGP018
PRG0_PRUIGP019	PRG0_PRUIGP019
PRG0_PRUIGP00	PRG0_PRUIGP00
PRG0_PRUIGP01	PRG0_PRUIGP01
PRG0_PRUIGP02	PRG0_PRUIGP02
PRG0_PRUIGP03	PRG0_PRUIGP03
PRG0_PRUIGP04	PRG0_PRUIGP04
PRG0_PRUIGP05	PRG0_PRUIGP05
PRG0_PRUIGP06	PRG0_PRUIGP06
PRG0_PRUIGP08	PRG0_PRUIGP08
PRG0_PRUIGP011	PRG0_PRUIGP011
PRG0_PRUIGP012	PRG0_PRUIGP012
PRG0_PRUIGP013	PRG0_PRUIGP013
PRG0_PRUIGP014	PRG0_PRUIGP014
PRG0_PRUIGP015	PRG0_PRUIGP015
PRG0_PRUIGP016	PRG0_PRUIGP016
PRG0_PRUIGP018	PRG0_PRUIGP018
PRG0_PRUIGP019	PRG0_PRUIGP019



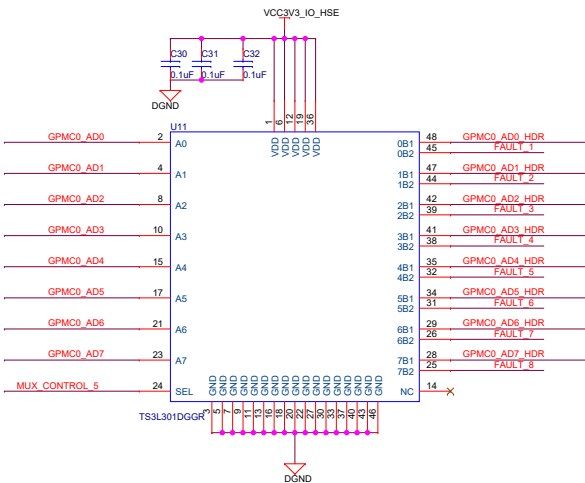
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GPMC0_AD2	GPMC0_AD2
GPMC0_AD3	GPMC0_AD3
GPMC0_AD4	GPMC0_AD4
GPMC0_AD5	GPMC0_AD5
GPMC0_AD6	GPMC0_AD6
GPMC0_AD7	GPMC0_AD7
GPMC0_AD8	GPMC0_AD8
GPMC0_AD9	GPMC0_AD9
GPMC0_AD10	GPMC0_AD10
GPMC0_AD11	GPMC0_AD11
GPMC0_AD12	GPMC0_AD12
GPMC0_AD13	GPMC0_AD13
GPMC0_AD14	GPMC0_AD14
GPMC0_AD15	GPMC0_AD15
GPMC0_CSn2	GPMC0_CSn2
GPMC0_CSn3	GPMC0_CSn3
GPMC0_CSn1	GPMC0_CSn1
GPMC0_DIR	GPMC0_DIR
HSE_GPIO0_31	HSE_GPIO0_31
HSE_GPIO0_32	HSE_GPIO0_32
HSE_GPIO0_33	HSE_GPIO0_33
HSE_GPIO0_34	HSE_GPIO0_34
HSE_GPIO0_35	HSE_GPIO0_35
HSE_GPIO0_36	HSE_GPIO0_36
HSE_GPIO0_37	HSE_GPIO0_37
HSE_GPIO0_38	HSE_GPIO0_38
HSE_GPIO0_39	HSE_GPIO0_39
HSE_GPIO0_41	HSE_GPIO0_41
SOC_SPI1_MISO	SOC_SPI1_MISO
SOC_SPI1_MOSI	SOC_SPI1_MOSI
SOC_SPI1_CLK	SOC_SPI1_CLK
SOC_SPI1_CS0	SOC_SPI1_CS0
SOC_SPI1_CS1	SOC_SPI1_CS1
PRG0_MDIO0_MDI0	PRG0_MDIO0_MDI0
PRG0_MDIO0_MDC	PRG0_MDIO0_MDC
HSE_MCANT1_TXI2C3_SCL	HSE_MCANT1_TXI2C3_SCL
HSE_MCANT1_RXI2C3_SDA	HSE_MCANT1_RXI2C3_SDA
HSE_MCANT1_TXUART4_RXD	HSE_MCANT1_TXUART4_RXD
HSE_MCANT1_RXUART4_TXD	HSE_MCANT1_RXUART4_TXD
MCU_RESETz	MCU_RESETz
MCU_RESETSTATz	MCU_RESETSTATz
MCU_PORz	MCU_PORz
PRG0_HSE_ETH2_CLK	PRG0_HSE_ETH2_CLK
PRG0_HSE_ETH1_CLK	PRG0_HSE_ETH1_CLK
PRG1_PRUIGP019	PRG1_PRUIGP019
PRG1_PRUIGP018	PRG1_PRUIGP018



PRG SIGNALS

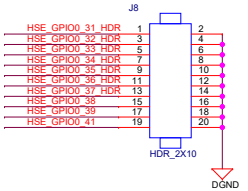
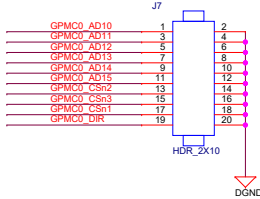
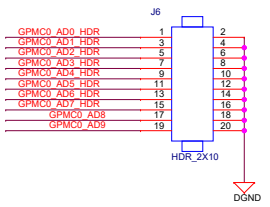
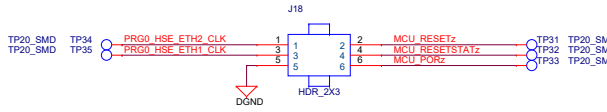
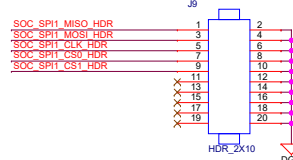
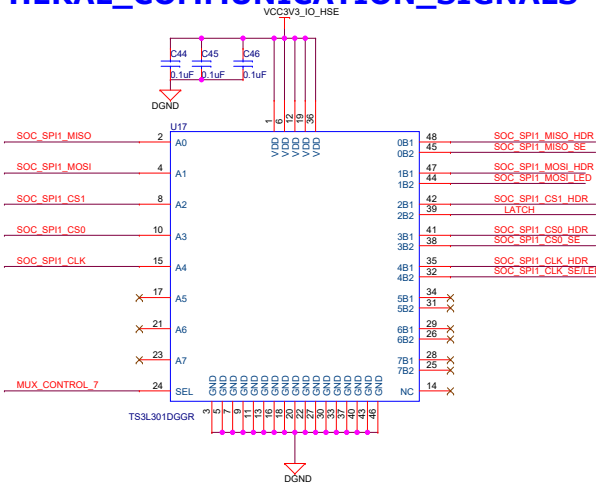


GPMC SIGNALS



GPMC0_AD0	GPMC0_AD0
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GPMC0_AD2	GPMC0_AD2
GPMC0_AD3	GPMC0_AD3
GPMC0_AD4	GPMC0_AD4
GPMC0_AD5	GPMC0_AD5
GPMC0_AD6	GPMC0_AD6
GPMC0_AD7	GPMC0_AD7
GPMC0_AD8	GPMC0_AD8
GPMC0_AD9	GPMC0_AD9
GPMC0_AD10	GPMC0_AD10
GPMC0_AD11	GPMC0_AD11
GPMC0_AD12	GPMC0_AD12
GPMC0_AD13	GPMC0_AD13
GPMC0_AD14	GPMC0_AD14
GPMC0_AD15	GPMC0_AD15
GPMC0_CSn2	GPMC0_CSn2
GPMC0_CSn3	GPMC0_CSn3
GPMC0_CSn1	GPMC0_CSn1
GPMC0_DIR	GPMC0_DIR
HSE_GPIO0_31	HSE_GPIO0_31
HSE_GPIO0_32	HSE_GPIO0_32
HSE_GPIO0_33	HSE_GPIO0_33
HSE_GPIO0_34	HSE_GPIO0_34
HSE_GPIO0_35	HSE_GPIO0_35
HSE_GPIO0_36	HSE_GPIO0_36
HSE_GPIO0_37	HSE_GPIO0_37
HSE_GPIO0_38	HSE_GPIO0_38
HSE_GPIO0_39	HSE_GPIO0_39
HSE_GPIO0_41	HSE_GPIO0_41
FAULT_1	FAULT_1
FAULT_2	FAULT_2
FAULT_3	FAULT_3
FAULT_4	FAULT_4
FAULT_5	FAULT_5
FAULT_6	FAULT_6
FAULT_7	FAULT_7
FAULT_8	FAULT_8
MUX_CONTROL_5	MUX_CONTROL_5
MUX_CONTROL_6	MUX_CONTROL_6
MUX_CONTROL_7	MUX_CONTROL_7
LOAD_PULSE_SE	LOAD_PULSE_SE
H_SEL	H_SEL
H_FAULT	H_FAULT
L_SEL	L_SEL
L_FAULT	L_FAULT
SOC_SPH1_MISO	SOC_SPH1_MISO
SOC_SPH1_MISO_SE	SOC_SPH1_MISO_SE
SOC_SPH1_CLK	SOC_SPH1_CLK
SOC_SPH1_CS0	SOC_SPH1_CS0
SOC_SPH1_CS1	SOC_SPH1_CS1
PRG0_HSE_ETH1_CLK	PRG0_HSE_ETH1_CLK
PRG0_HSE_ETH2_CLK	PRG0_HSE_ETH2_CLK
MCU_RESETz	MCU_RESETz
MCU_RESETSTATz	MCU_RESETSTATz
MCU_PORz	MCU_PORz
SOC_SPH1_MISO_SE	SOC_SPH1_MISO_SE
SOC_SPH1_CS0_SE	SOC_SPH1_CS0_SE
LOAD_PULSE_SE	LOAD_PULSE_SE
LATCH	LATCH
SOC_SPH1_MISO_LED	SOC_SPH1_MISO_LED
SOC_SPH1_CLK_SELED	SOC_SPH1_CLK_SELED

PERIPHERAL_COMMUNICATION_SIGNALS



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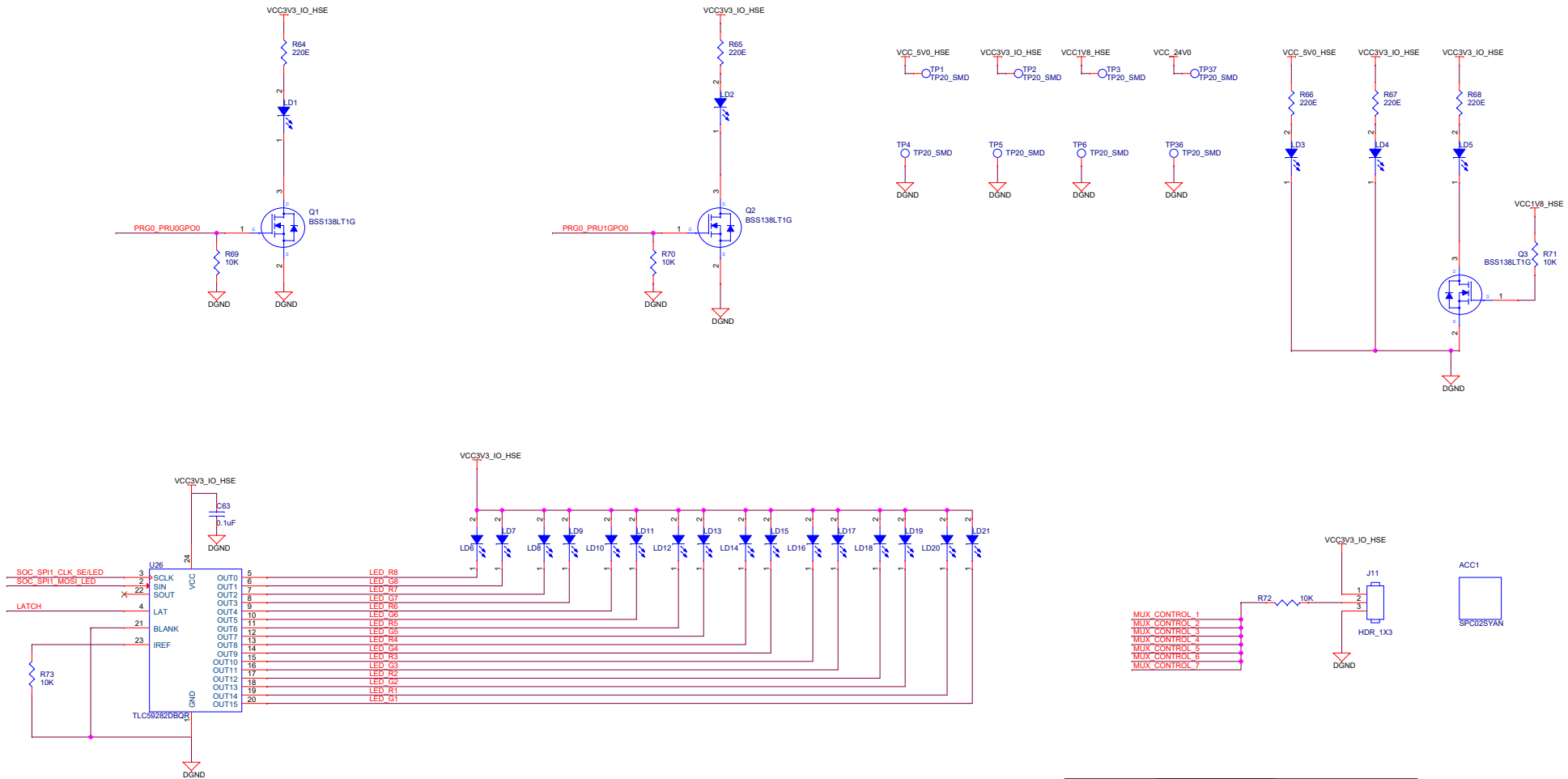


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LED'S

PRG0_LED

Test Points



SEL	INPUT/OUTPUT An	FUNCTION
L	nB1	An=nB1
H	nB2	An=nB2

HEADER SIDE IS
ACTIVATED

IO LINK IS
ACTIVATED

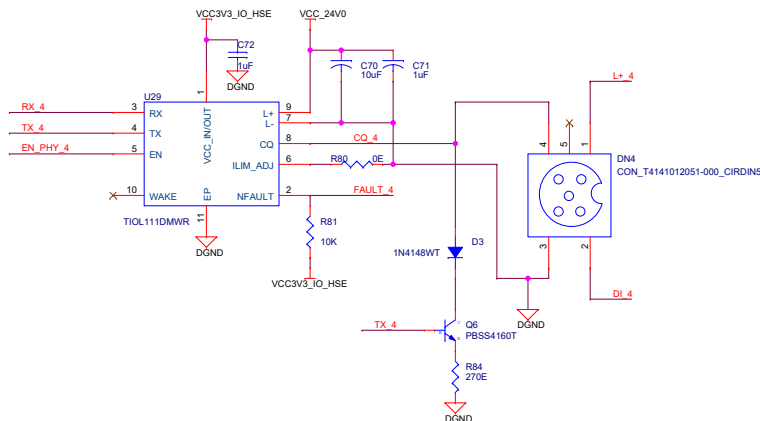
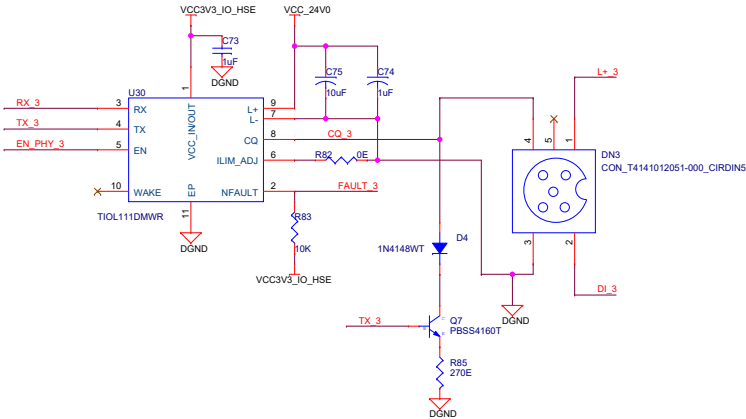
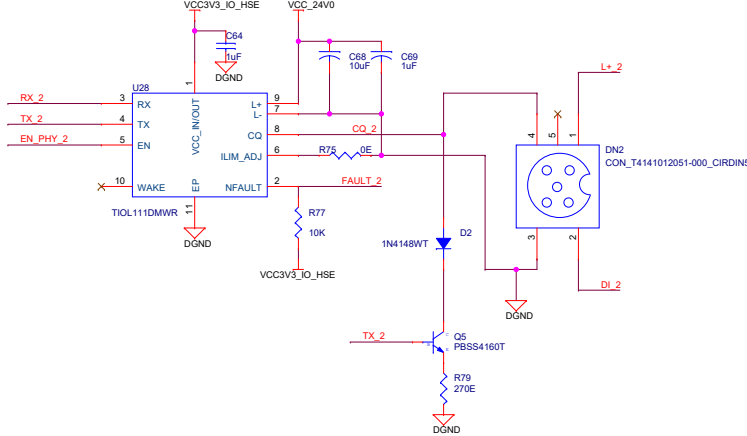
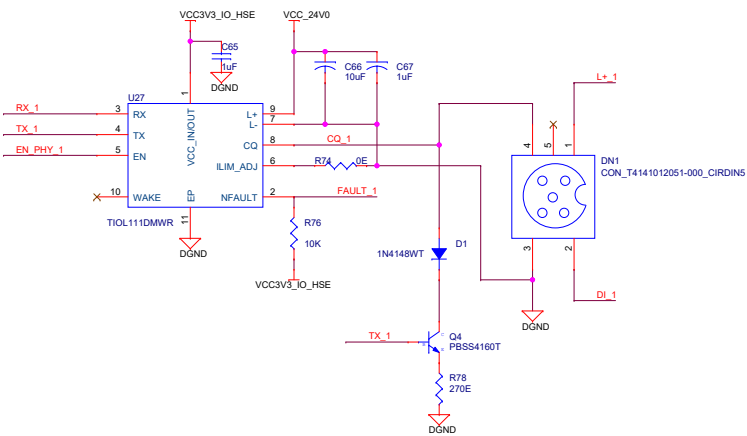


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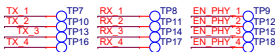


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IO LINK TRANCIEVER[1:4]



- EN_PHY_1 > EN_PHY_1
- EN_PHY_2 > EN_PHY_2
- EN_PHY_3 > EN_PHY_3
- EN_PHY_4 > EN_PHY_4
- FAULT_1 > FAULT_1
- FAULT_2 > FAULT_2
- FAULT_3 > FAULT_3
- FAULT_4 > FAULT_4
- RX_1 > RX_1
- RX_2 > RX_2
- RX_3 > RX_3
- RX_4 > RX_4
- TX_1 > TX_1
- TX_2 > TX_2
- TX_3 > TX_3
- TX_4 > TX_4
- DI_1 > DI_1
- DI_2 > DI_2
- DI_3 > DI_3
- DI_4 > DI_4
- L+3 > L+3
- L+1 > L+1
- L+2 > L+2

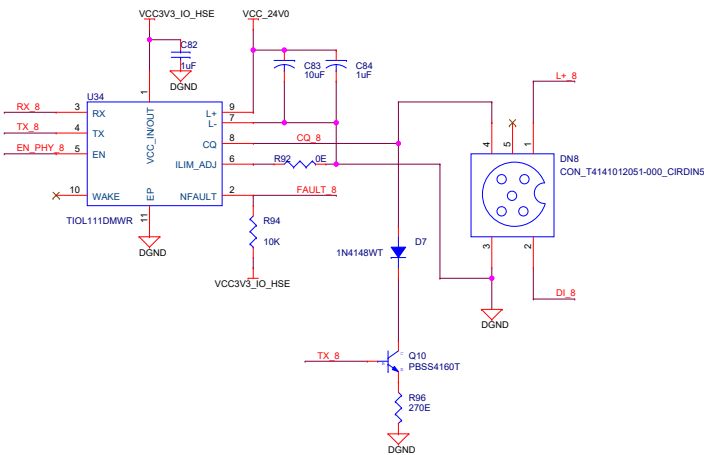
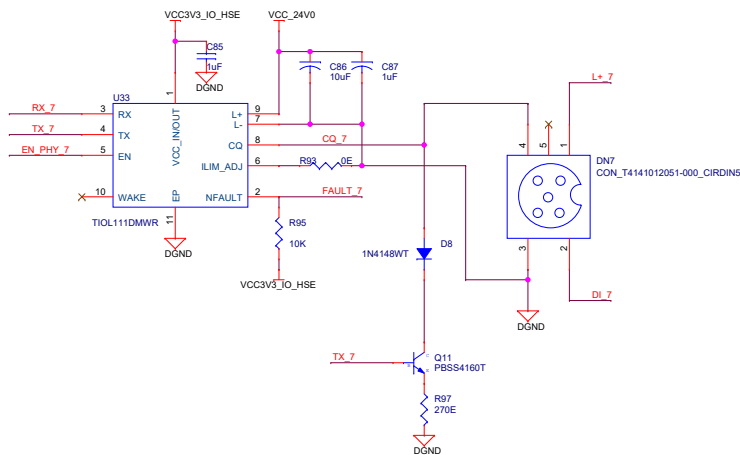
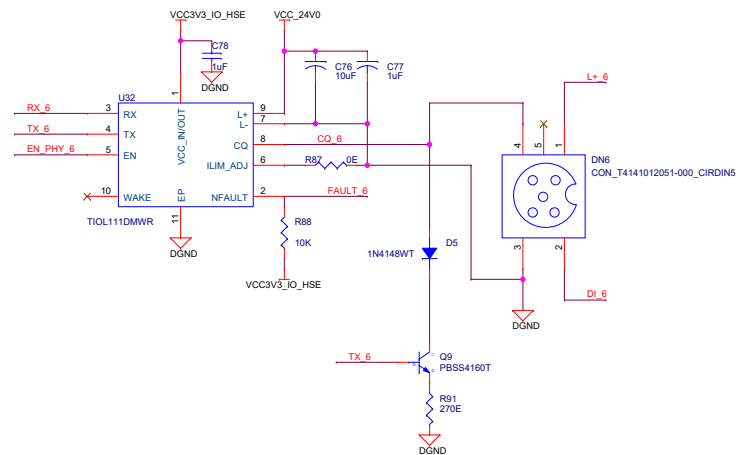
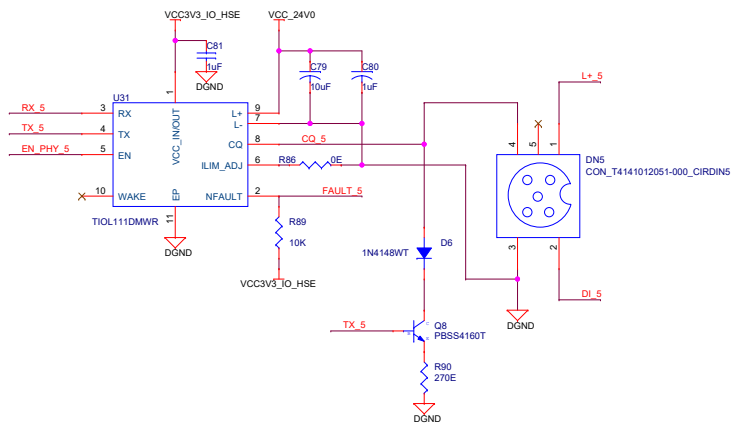


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IO LINK TRANCIEVER[5:8]



TX_5 TP19 RX_5 TP20 EN_PHY_5 TP21
TX_6 TP22 RX_6 TP23 EN_PHY_6 TP24
TX_7 TP25 RX_7 TP26 EN_PHY_7 TP27
TX_8 TP28 RX_8 TP29 EN_PHY_8 TP30

DI_5 DI_5
DI_6 DI_6
DI_7 DI_7
DI_8 DI_8
L+_5 L+_5
L+_6 L+_6
L+_7 L+_7
L+_8 L+_8

FAULT_5 FAULT_5
FAULT_6 FAULT_6
FAULT_7 FAULT_7
FAULT_8 FAULT_8
EN_PHY_5 EN_PHY_5
EN_PHY_6 EN_PHY_6
EN_PHY_7 EN_PHY_7
EN_PHY_8 EN_PHY_8
RX_5 RX_5
RX_6 RX_6
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RX_8 RX_8
TX_5 TX_5
TX_6 TX_6
TX_7 TX_7
TX_8 TX_8

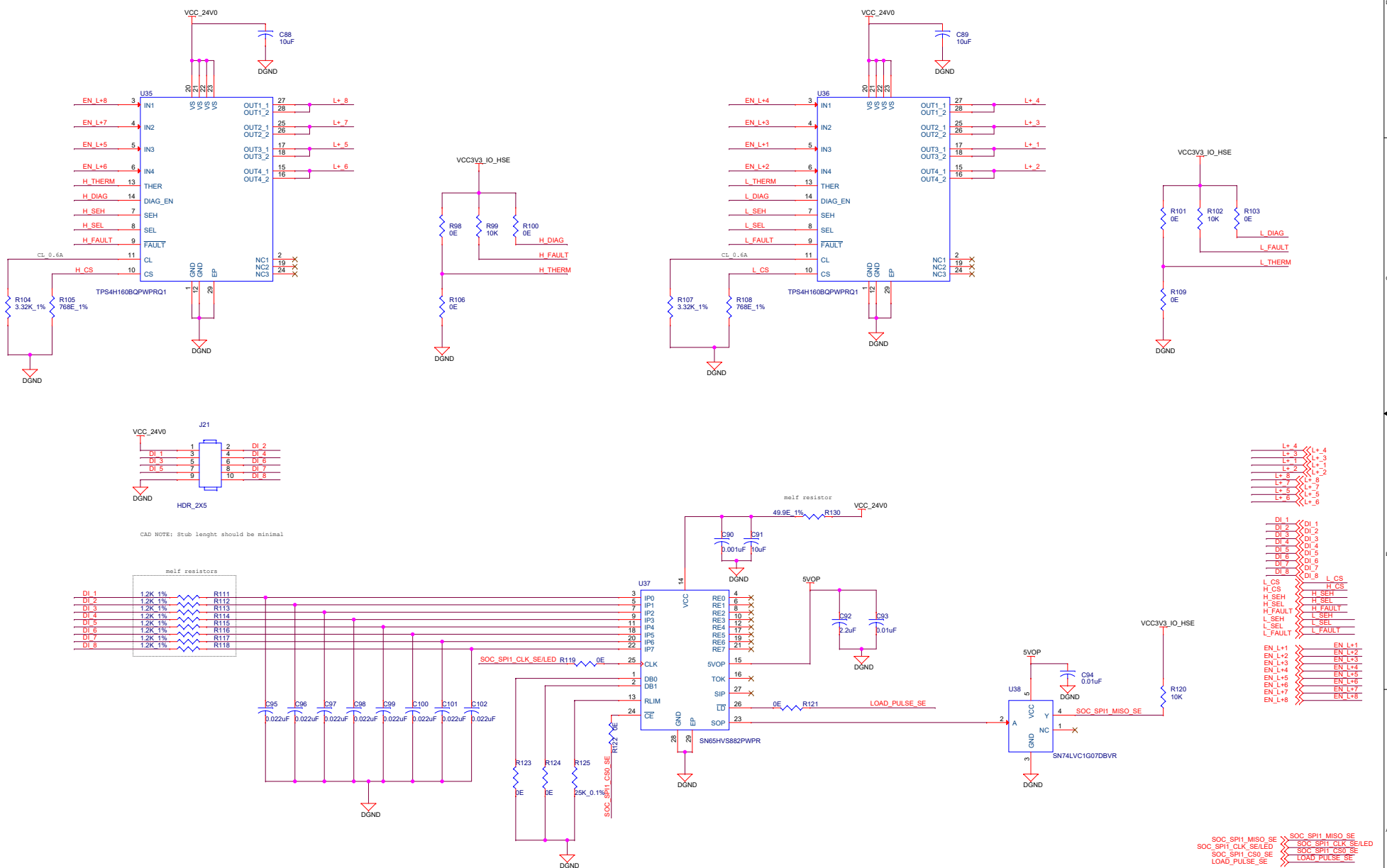
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Title IO LINK TRANCIEVER[5:8]

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SMART SWITCH



A

