IO LINK/BREAKOUT BOARD

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VER	0.4

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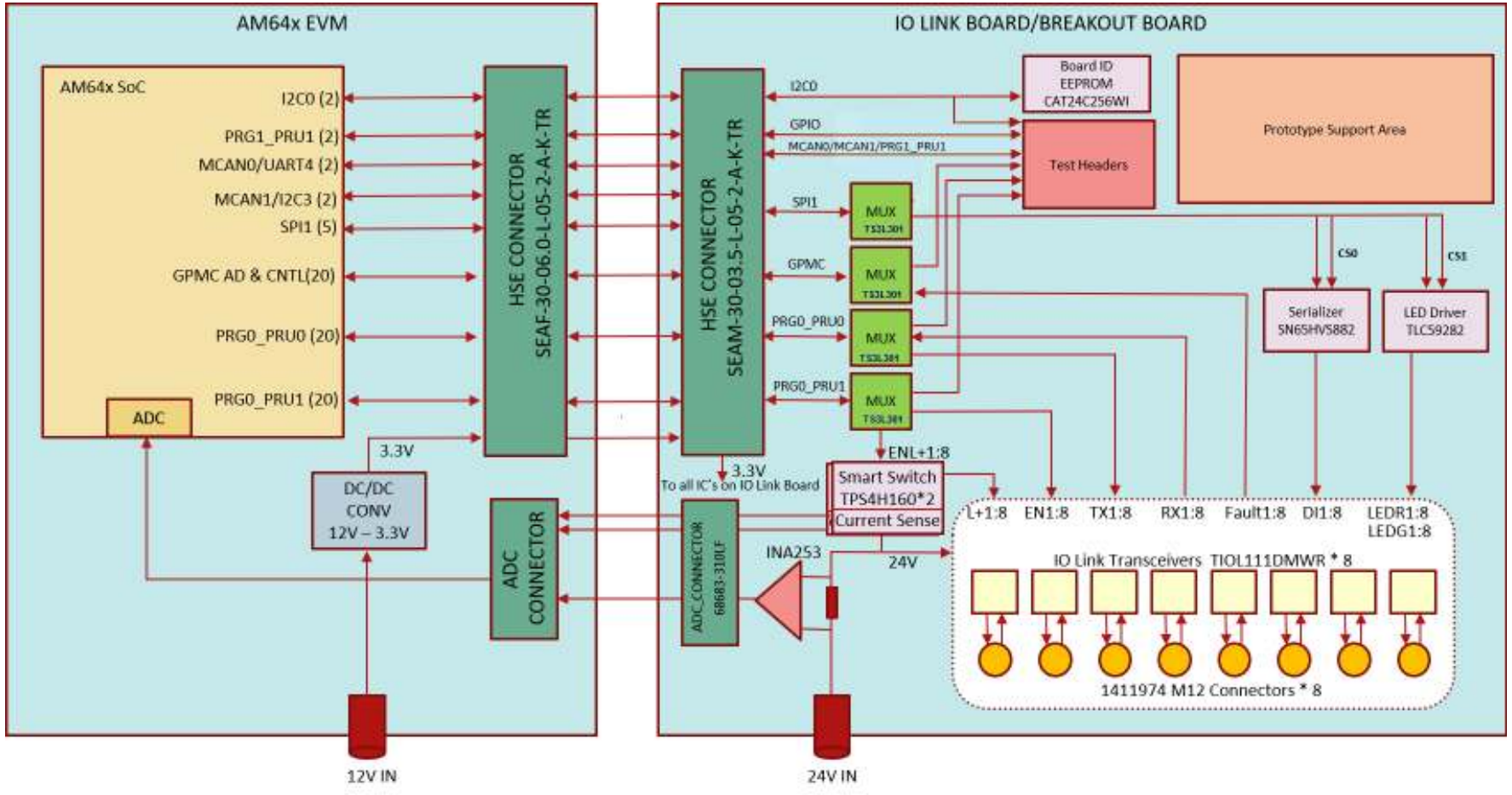
REVISION HISTORY

REV #	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.1	17-07-2020	INITIAL DRAFT	Mistral Design Team	RAKESH RAJDEV	AJIT MB
E1	0.2	03-09-2020	M12 connector parts changed, Level translators removed.	Mistral Design Team	RAKESH RAJDEV	AJIT MB
E1	0.3	15-09-2021	RELEASED FOR TI REVIEW	Mistral Design Team	RAKESH RAJDEV	AJIT MB
E1	0.4	29-09-2021	Rearranged Signals as per TI Review Comments	Mistral Design Team	RAKESH RAJDEV	AJIT MB

BLOCK DIAGRAM



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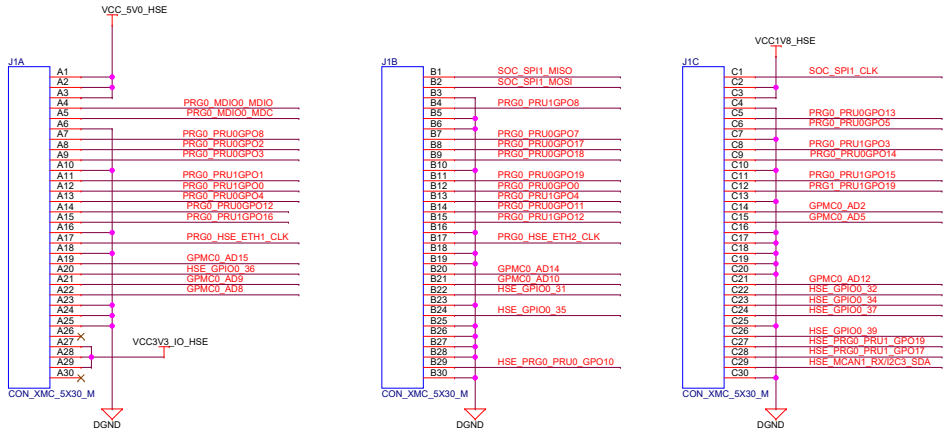
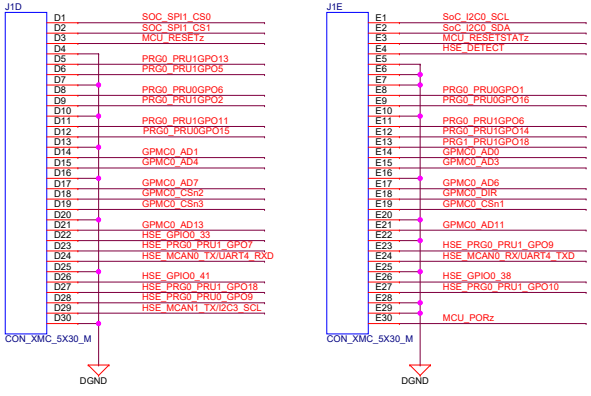
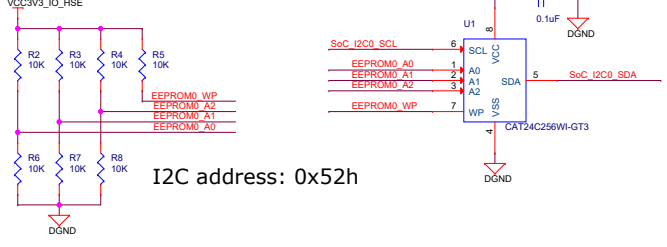
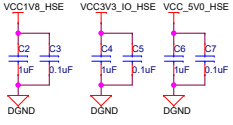
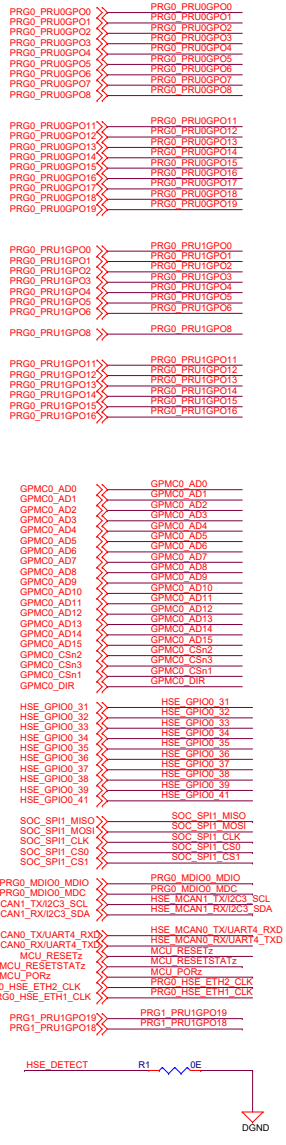
HSE CONNECTOR











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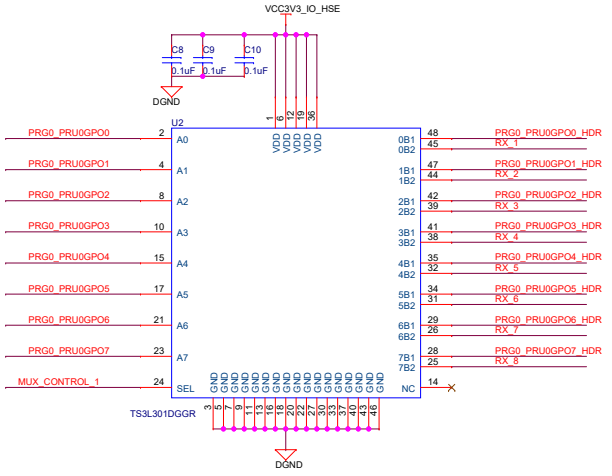
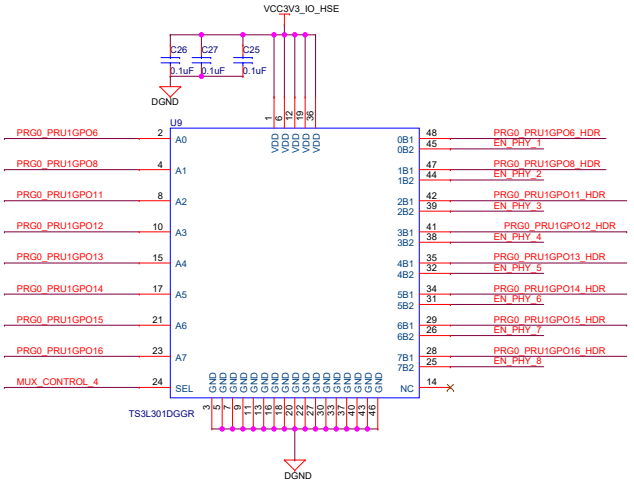
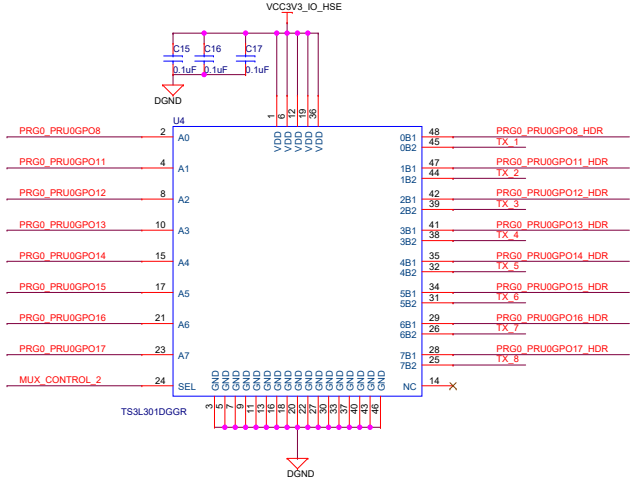
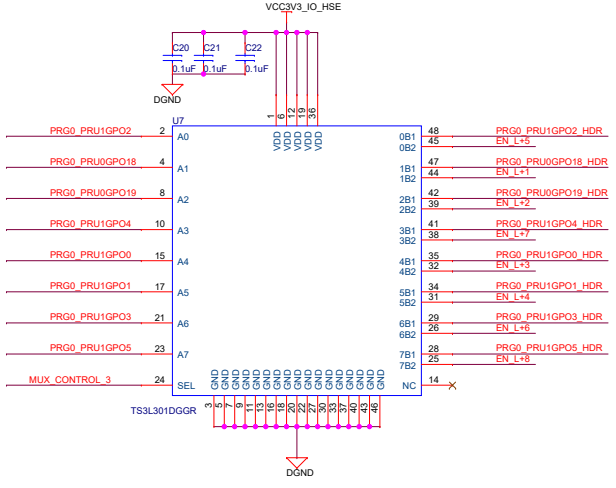
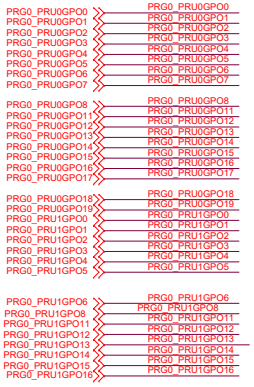
PRG SIGNALS

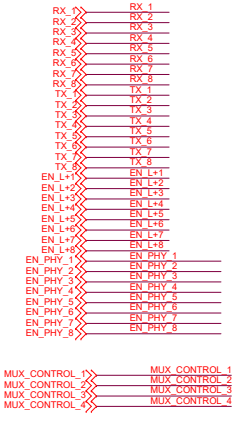


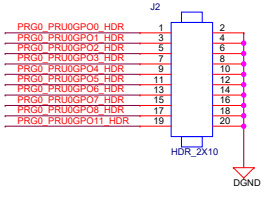


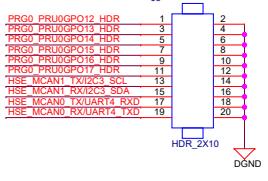


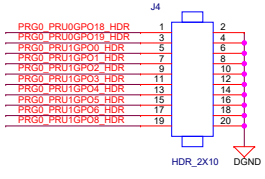


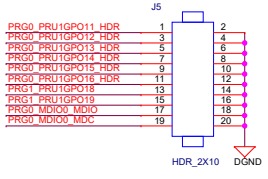












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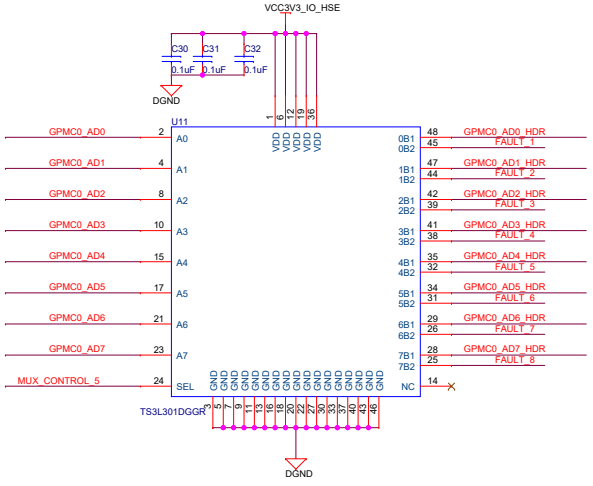
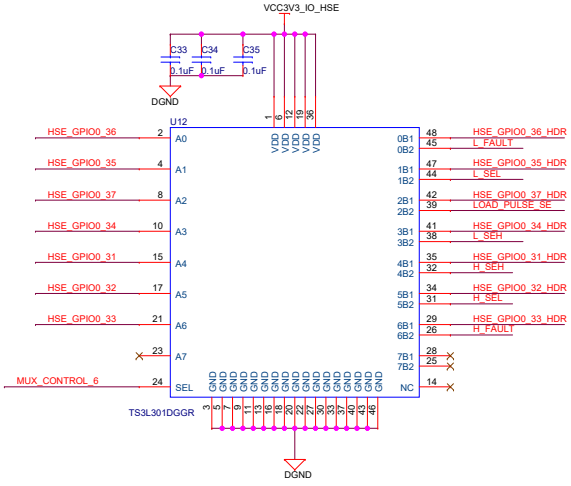
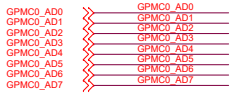
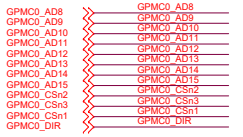
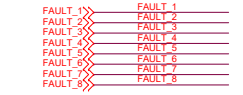
GPMC SIGNALS

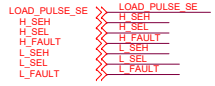


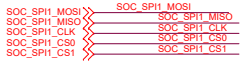




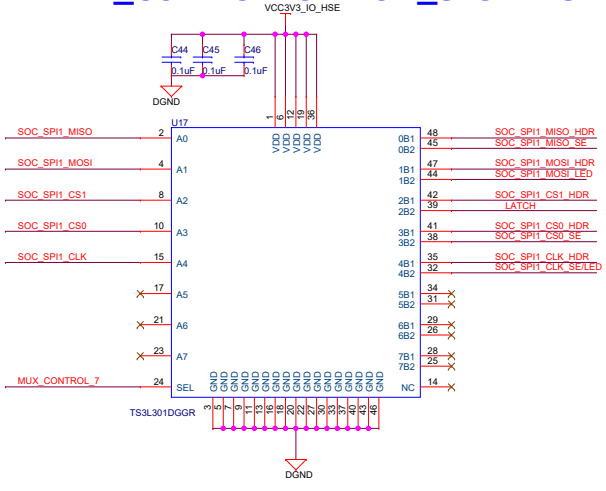


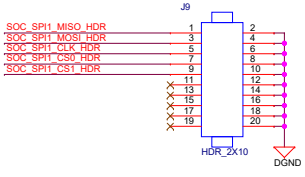


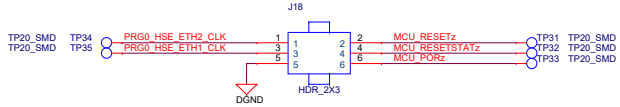


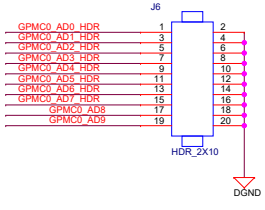


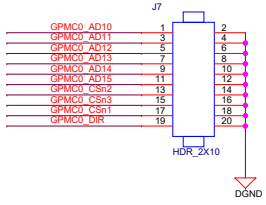
PERIPHERAL_COMMUNICATION_SIGNALS

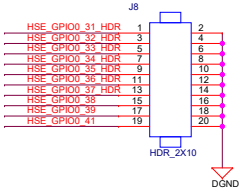












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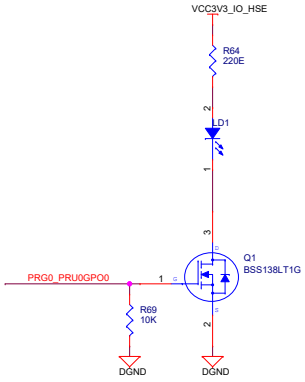
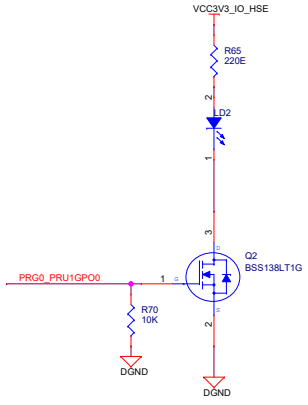
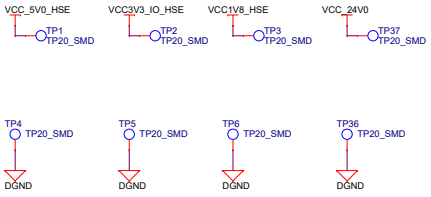
LED'S

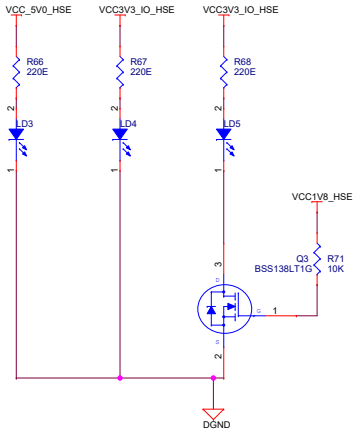
PRG0_LED

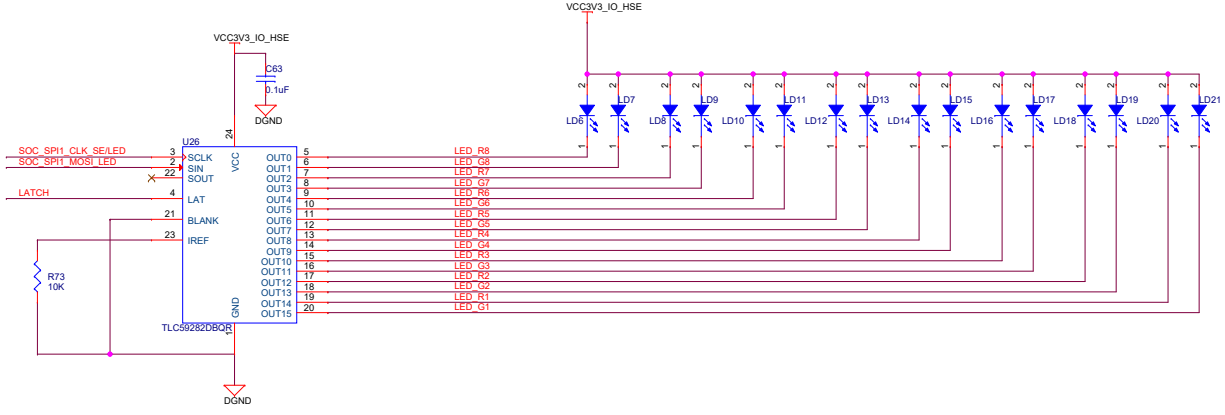


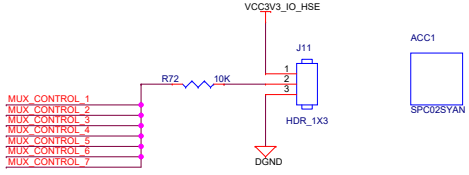


Test Points









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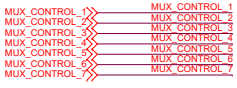
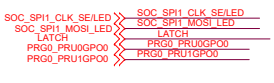
H	nB2	An=nB2

HEADER SIDE IS ACTIVATED

IO LINK IS ACTIVATED





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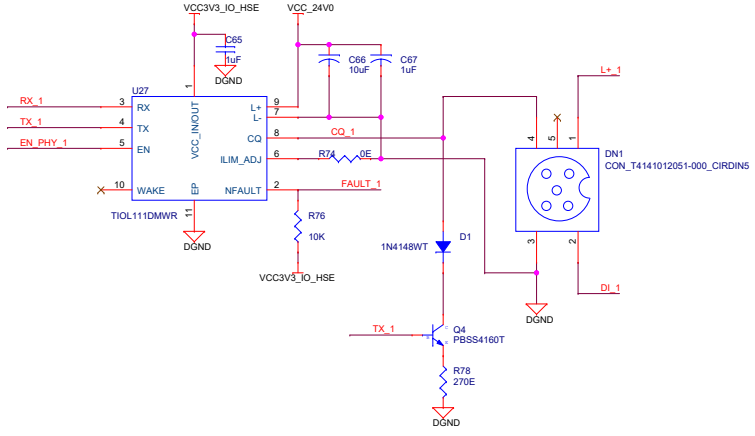
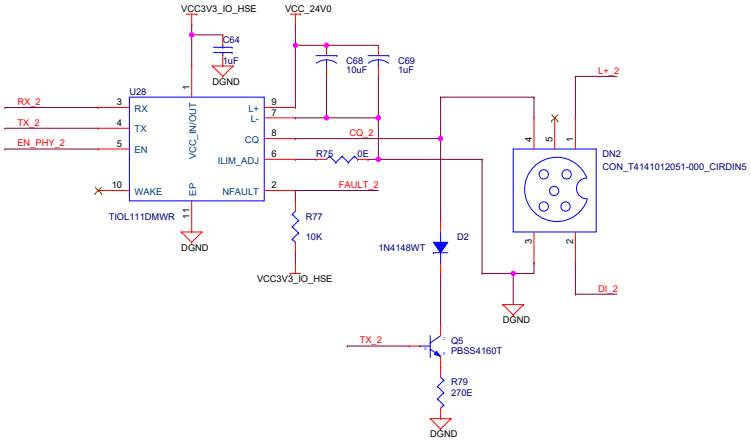
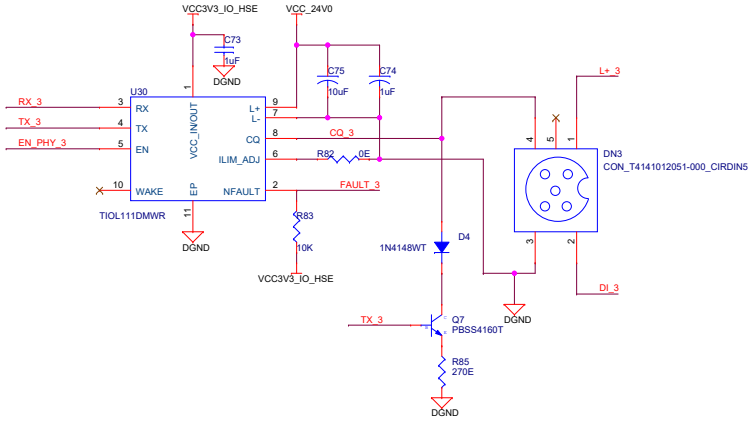
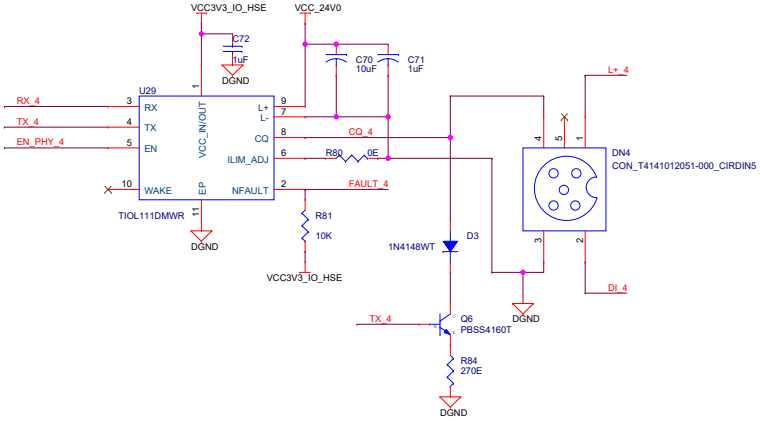
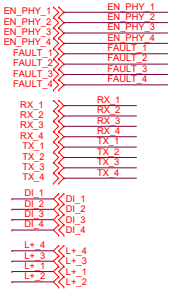
IO LINK TRANCIEVER[1:4]

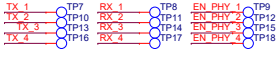












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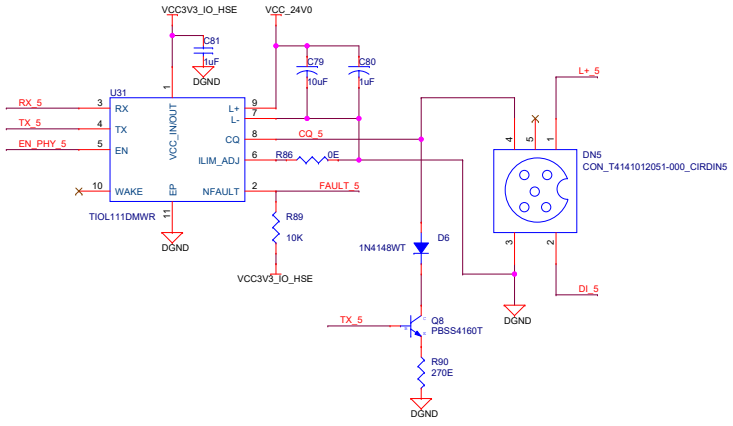

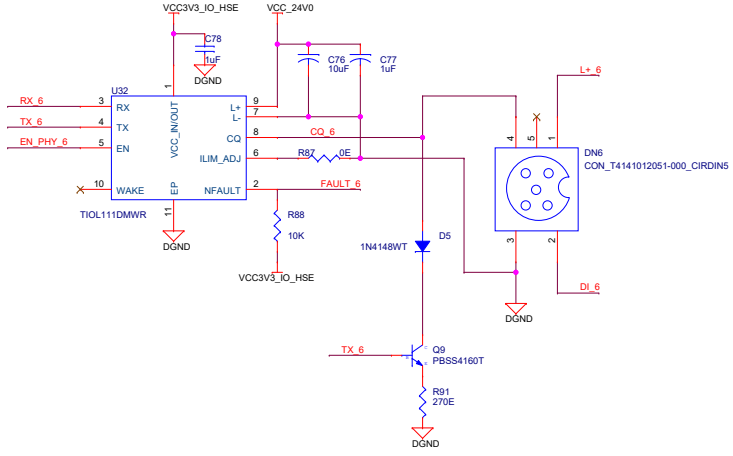

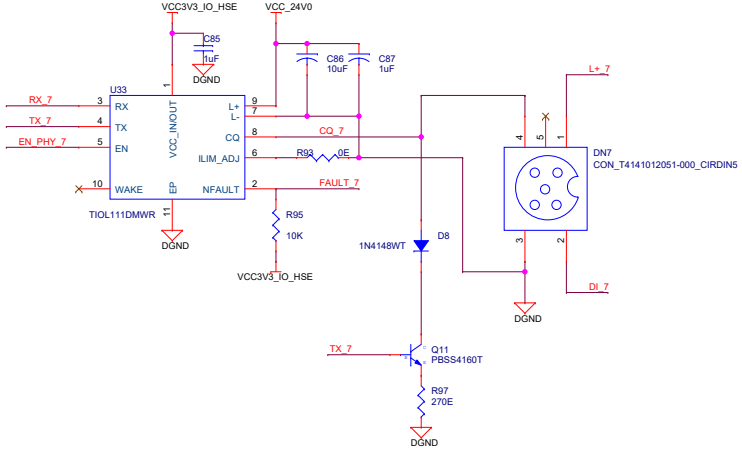

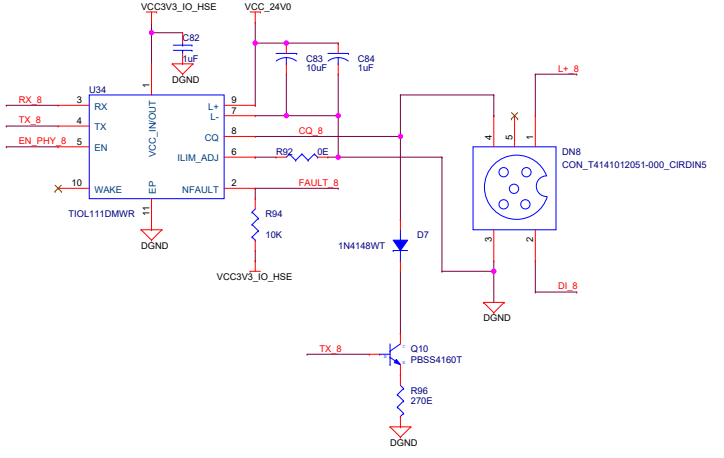

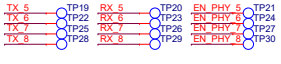

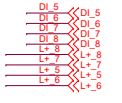

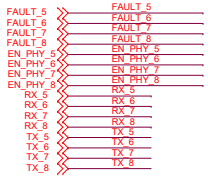

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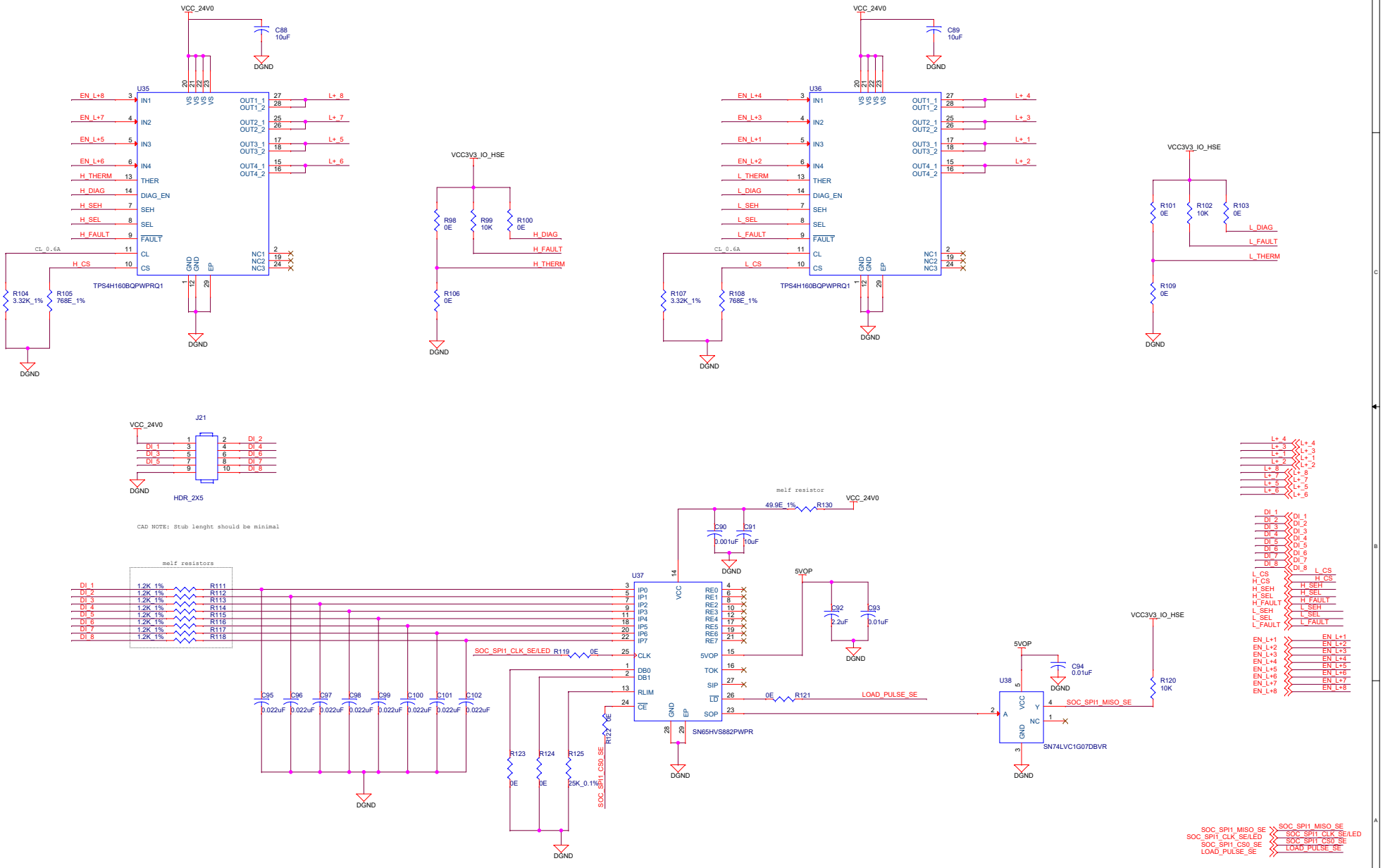
SMART SWITCH



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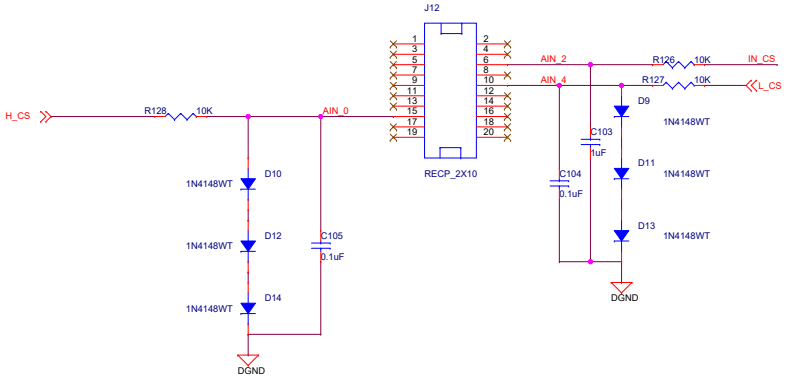
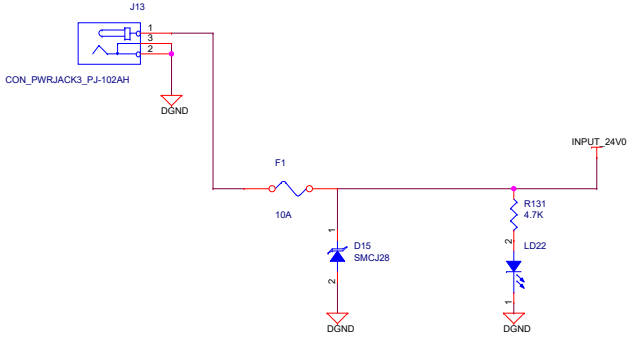
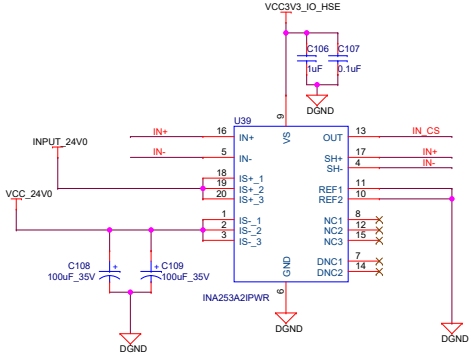
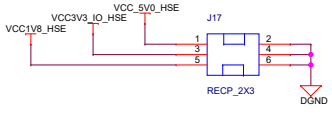
POWER AND ADC SECTION







POWER SUPPLY_HEADER



CAD NOTE: PLACE THIS HEADER NEAR PROTOTYPE SUPPORT AREA

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