

Power Supply Design Seminar

Practical EMI Considerations for Low-Power AC/DC Supplies

Reproduced from 2020 Texas Instruments Power Supply Design Seminar SEM2400

TI Literature Number: SLUP400

© 2020 Texas Instruments Incorporated

Power Seminar topics and online power training modules are available at: ti.com/psds



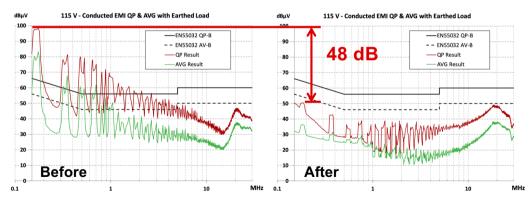
Practical EMI Considerations for Low-Power AC/DC Supplies

Bernard Keogh
Joe Leisten

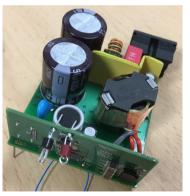


Electromagnetic interference (EMI)

- I built my 65 W adapter prototype and resolved all functional issues
- I ran first-pass EMI scan and my design failed badly! ~100 dBμV
 - How can I fix the EMI?
 - Where do I start?
- This presentation will show how to get to a result like this, without necessarily adding a big EMI filter







Agenda

- Introduction to EMI testing
- What causes EMI
- Differential-mode vs common-mode EMI
- EMI mitigation options
- Analyzing the transformer
- · Troubleshooting & debug
- 65 W USB-PD example design using active clamp flyback (ACF) topology

Conducted emissions (CE) standards

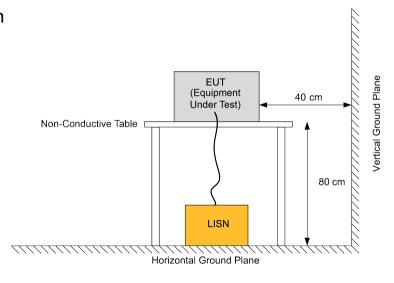
Summary of main product standards for conducted emissions

Product Sector	CISPR Standard	EN Standard	FCC Standard
Automotive	CISPR 25	EN 55025	
Multimedia	CISPR 32	EN 55032	Part 15
ISM	CISPR 11	EN 55011	Part 18
Household appliances, electric tools and similar apparatus	CISPR 14-1	EN 55014-1	
Lighting equipment	CISPR 15	EN 55015	Part 15/18

Reference:

Timothy Hegarty, "An overview of conducted EMI specifications for power supplies," http://www.ti.com/lit/wp/slyy136/slyy136.pdf

- Equipment under test (EUT) placed on non-conductive table
- · Horizontal & vertical ground planes
 - Or screened room
- EUT powered through line impedance stabilization network (LISN)
- Measure high-frequency (HF) emissions from LISN

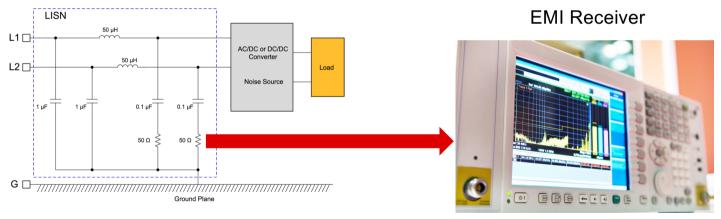


[1] EN55022, 2010, "Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement"



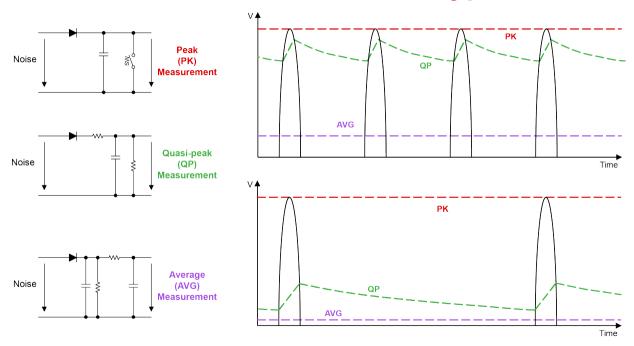
LISN – Line impedance stabilization network

- Presents stable, consistent & repeatable line source impedance
- Separation of power source noise current for measurement
 - Low frequency power current passes straight through from AC source
- "Total" noise levels measured separately on L1 (live) and L2 (neutral)



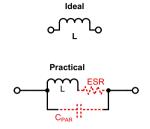
^{**} Functional equivalent circuit of a LISN, not a complete schematic **

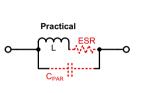
EMI receiver – Built-in detector types

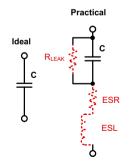


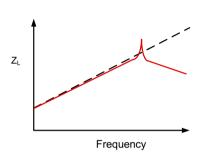
Component parasitics

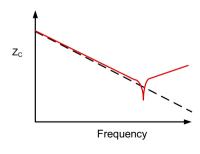
- Parasitic elements are the dominant cause of EMI issues
- EMI noise is coupled & propagated through parasitic elements:
 - Capacitive coupling
 - Inductive coupling
- EMI filter performance is **dominated** by parasitic elements at higher frequency:
 - Parasitic capacitance of inductors
 - Parasitic inductance of capacitors



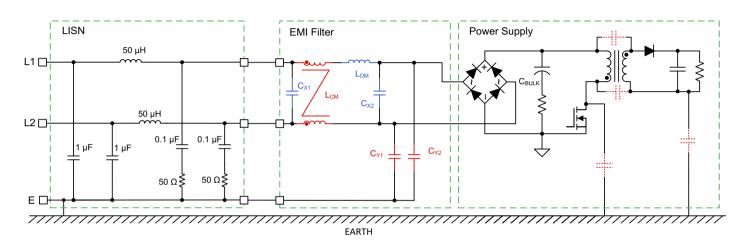








LISN + EMI filter + power supply



LISN - measures noise

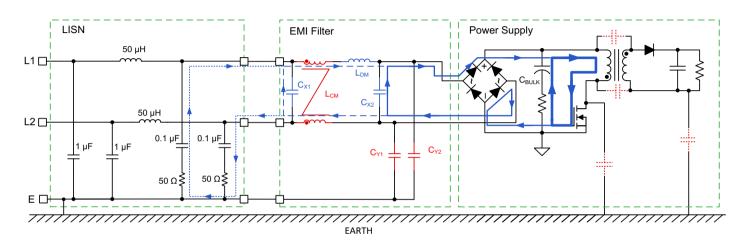
EMI filter – limits noise that gets to the LISN

(CM - red, DM - blue)

Power supply – generates the noise

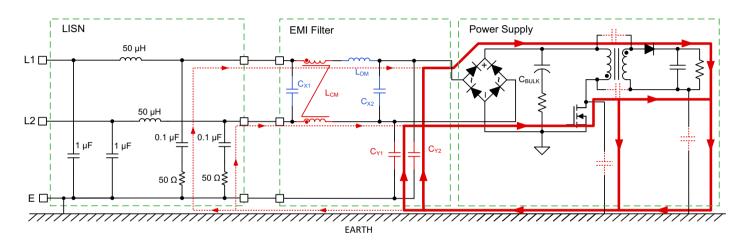
(parasitic cap – red dotted)

DM EMI filter and current path



- DM EMI filter limits DM noise that gets to the LISN
 - X-caps divert current away from LISN, keep local to power supply
 - DM choke high impedance reduces size of current flowing to LISN

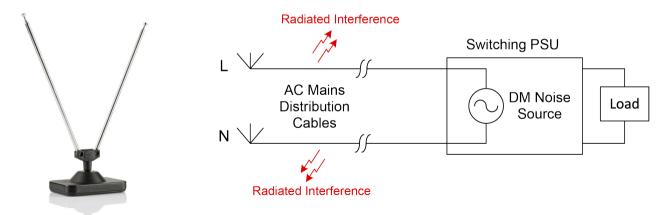
CM EMI filter and current path



- CM EMI filter limits CM noise that gets to the LISN
 - Y-caps divert current away from LISN, keep local to the power supply
 - CM choke high impedance reduces size of current flowing to LISN

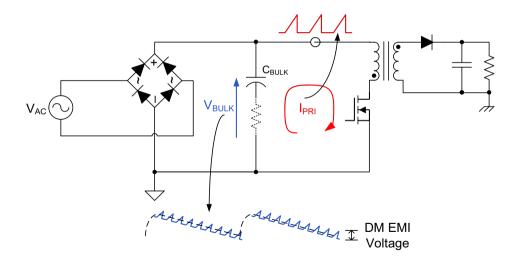
Why care about differential-mode (DM) EMI?

- DM noise conducts to the AC utility supply network
- Long AC distribution cables act as good dipole antenna
- Will inadvertently radiate switching noise and interfere with radio communications
 - (E.g., noise @ ~100 MHz will affect FM radio)



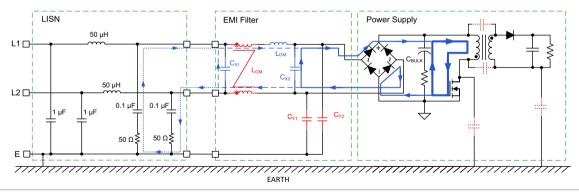
How is DM EMI generated?

- Switching ripple current produces ripple voltage across ESR (& ESL)
- Ripple voltage is the DM noise that needs to be attenuated/filtered



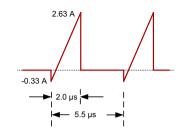
Mitigation options for DM noise

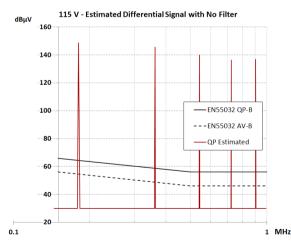
- Include EMI at the design phase
 - Make design & component choices to minimize DM EMI signal amplitude
 - Chose frequency, inductance, etc. to minimize PK-PK ripple current
 - Choose capacitors with low ESR to minimize PK-PK ripple voltage
 - Good PCB layout important to minimize EMI
- Design sufficient DM LC filter to reduce the ripple that gets onto the AC line input



DM filter design methodology

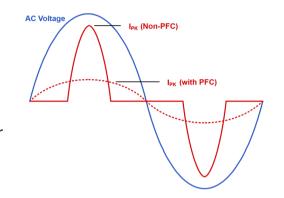
- Measure, simulate or calculate time-domain current waveform
- Fourier analysis of time-domain switching current
 - Convert waveform into harmonic components
- Establish required attenuation at each frequency
 - To get sufficient margin below the required EMI limit
- Design the DM filter to achieve required attenuation
 - Need to check all frequencies of interest
 - Typically limited by lowest frequency inside measurement band
 - Typically EMI starts at 150 kHz for AC/DC PSU to meet EN55022 or EN55032

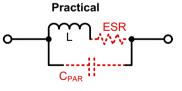




DM filter choke practical considerations

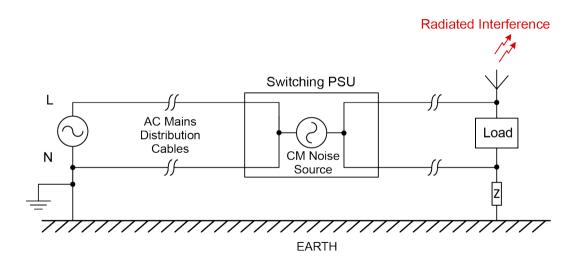
- Choke requires high attenuation over wide bandwidth:
 - Load current amplitude typically several amps
 - At 50 dB μ V, current in LISN 50 Ω resistor only ~6.3 μ A
- Beware inductance roll-off with DC-bias
 - Must not saturate to be effective needs high current rating
 - Consider the peak line current for non-PFC high crest factor
- Switching power stage has fast changing magnetic fields
 - Beware filter bypassing & noise coupling
- Parasitic capacitance across DM inductor very important
 - Reduces effectiveness, especially at high frequency
- Example: To filter 300 kHz component, typically set LC freq. ~30 kHz
 - Expect ~40 dB attenuation at 300 kHz (double-pole ⇒ 40 dB/decade)
 - With parasitic cap ⇒ more like 30 dB attenuation only even worse at higher frequency





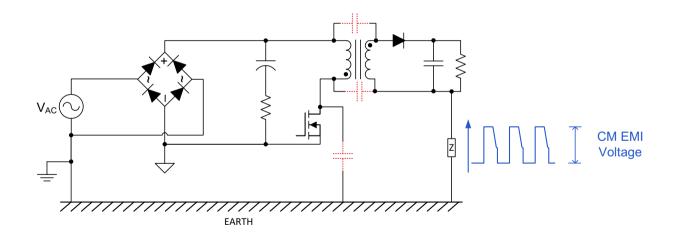
Why care about common-mode (CM) EMI?

- Again, AC distribution cables and output load cables act as good uni-polar antenna
- CM noise will radiate from the cables and interfere with radio communications



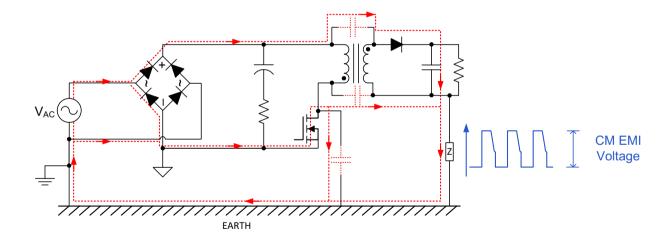
How is CM EMI generated?

Switching voltage across parasitic capacitance causes CM current flow to EARTH



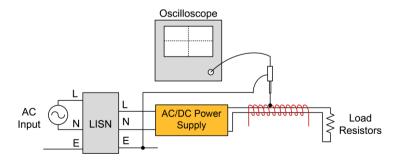
How is CM EMI generated?

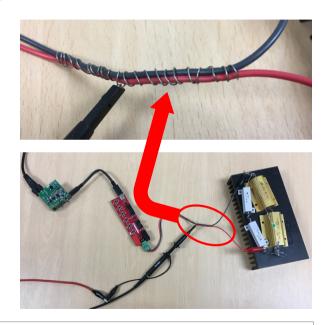
- Switching voltage across parasitic capacitance causes CM current flow to EARTH
- CM noise also radiated to other circuit nodes



Observing the time-domain CM signal at the output

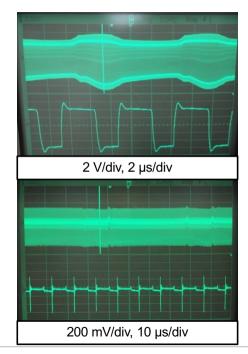
- Useful debug technique ball-park indication of CM performance
 - Remove Y-cap temporarily (maximize signal)
 - Power EUT through LISN, with resistor loads
 - Wind several turns of wire around the load cables to create capacitive sensing coil (pickup coil)
 - Connect scope EARTH lead to LISN EARTH
 - Connect scope tip to sensing coil
 - Scope plot shows how much CM is coupled to output





Interpretation of time-domain CM signal

- Will see "switch-node" shaped waveform coupled to output
- Large PK-PK amplitude ⇒ bad CM noise
 - Will require significant CM filtering to suppress
 - Result from ACF example with 100 dBμV EMI
- Small PK-PK amplitude ⇒ good CM noise
 - "Balanced" structure giving low CM
 - Will require much smaller CM filter
- Residual HF "spikes" ⇒ should only need small HF CM choke



Mitigation options for CM noise

Shielding:

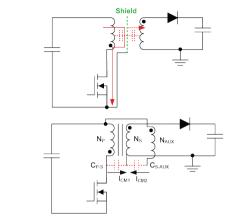
Reduce flow of HF current to EARTH

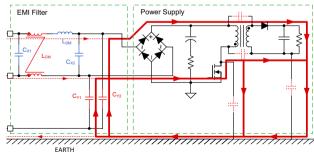
2. Cancellation:

 Arrange transformer and power stage for balanced CM

3. Filtering:

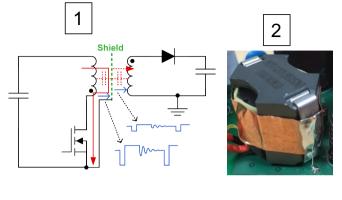
- Increase impedance of the EARTH return path
- Provide alternative routes for the HF current

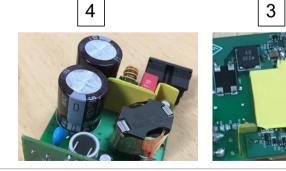




1. CM mitigation by shielding

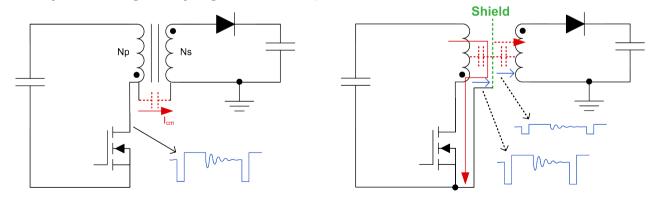
- 1. Shielding inside the transformer
 - Internal shields between pri & sec
- Shielding outside the transformer
 - GNDed flux-band
- 3. Shielding of noisy circuit nodes
 - GNDed heatsinks over/around high-voltage switching nodes
- Shielding of EMI filter from switching cct.
 - GNDed shields/enclosures around filter





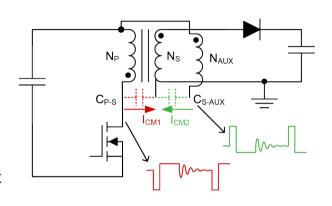
Transformer internal shielding

- Shield added to keep most of CM current local to primary
- Shield is 1-turn winding ⇒ lower induced voltage, less voltage across parasitic capacitance between shield & sec ⇒ less CM current flows
- Shield must be thin (< 50 μm) ⇒ minimize induced eddy current loss
 - Eddy currents get very significant as F_{SW} increases



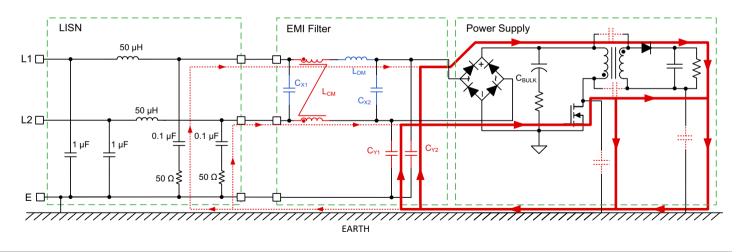
2. CM mitigation by cancellation/balance

- Single-ended topologies can add explicit additional cancellation elements
 - Add auxiliary (AUX) transformer winding
 - AUX voltage proportional to CM waveform
 - Arrange AUX polarity for opposite phase
 - Capacitor to inject cancelling current, I_{CM2}, to balance CM current from primary, I_{CM1}
 - Injection capacitor explicit physical component added to design
 - Or can use parasitic capacitance, e.g., C_{S-AUX}, part of transformer structure



3. CM mitigation by filtering

- CM filter uses high-impedance CM chokes and low-impedance Y-capacitors
- CM choke limits the flow of CM current from EARTH through the LISN
- Y-cap provides low impedance to keep CM current local to primary GND and away from LISN



CM filter choke practical considerations

Frequency response of core material

- High-µ cores ⇒ high L value @ low freq, but roll off fast at higher freq
- High-freq cores ⇒ low-μ, smaller L value @ low freq, better vs freq
- Sometimes need to use 2 CM chokes, 1 for LF & 1 for HF

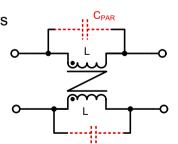
Split-wound vs bifilar-wound toroid

- Split-wound popular, lower cost, "free" DM choke from leakage field
- Bifilar ⇒ 1-side insulated wire, higher cost, but better noise immunity

Parasitic input-output cap – multi-layer windings

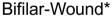
Parasitic cap depends on number of turns & layers

- High C_{PAR} input-output cap ⇒ worse @ HF
- Less layers \Rightarrow lower L, but also lower C_{PAR}
- Sectional bobbins used to reduce C_{PAR}











Multi-Section



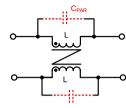
^{*}CM choke 3-D images reproduced with permission of Wurth Elektronic

CM filter choke – Impact of C_{PAR}



Split-Wound 2L

- Split-wound 2-layer:
 - 25T, 5.1 mH
 - Excess pass margin @ LF
 - Low pass margin @ 20 MHz





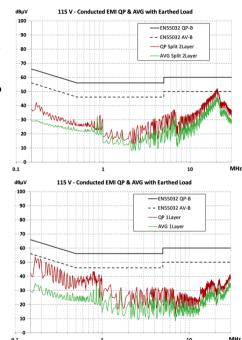
Bifilar-Wound 1L

- Bifilar-wound 1-layer:
 - 14T, 1.1 mH
 - Low input-output C_{PAR}
 - Lower L at LF, but better at HF
 - Better balance across frequency span



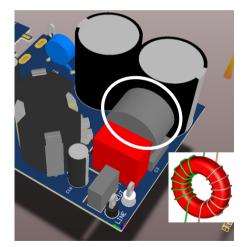
Split-Wound 1L

- Split-wound 1-layer:
 - 14T, 1.4 mH
 - Similar low input-output C_{PAR}
 - Similar result as bifilar-wound



CM choke example

- Initial split-wound choke had issues due to asymmetric noise coupling from transformer
 - Shows up as big difference in EMI on L vs N



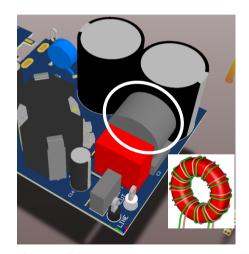


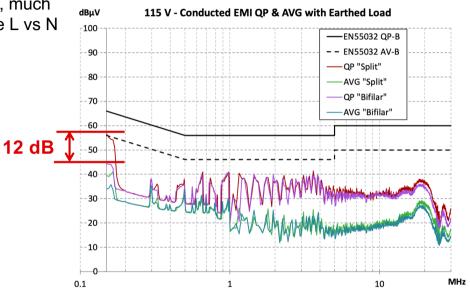
*CM choke 3-D image reproduced with permission of Wurth Elektronic

CM choke example

 Changed to bifilar-wound choke, much better EMI result; less difference L vs N

Much better noise immunity

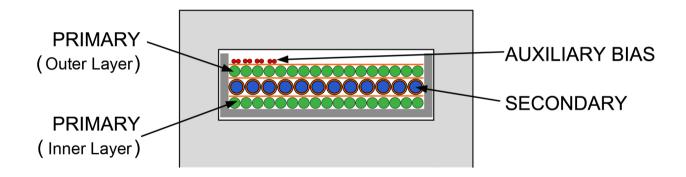




^{*}CM choke 3-D image reproduced with permission of Wurth Elektronic

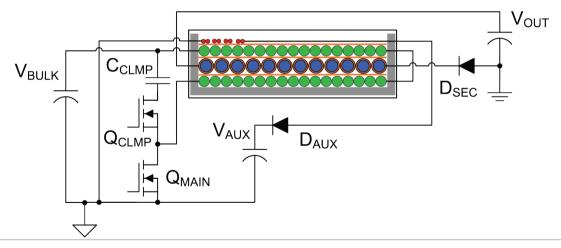
Transformer CM noise analysis – PMP21479 ACF

- Initial design interleaved flyback transformer construction, no internal shielding
- Same transformer used for initial test with poor 100 dbµV EMI result



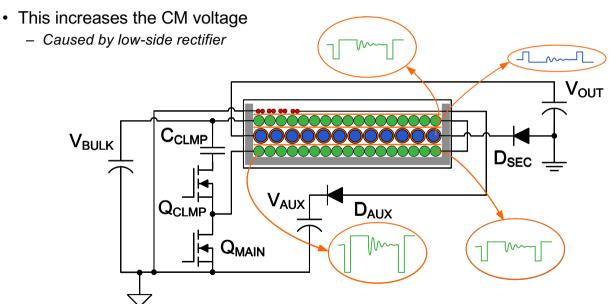
Transformer CM noise analysis – PMP21479 ACF

- Circuit connections to the ACF power stage
- Note the secondary low-side rectifier causes inverted secondary winding polarity



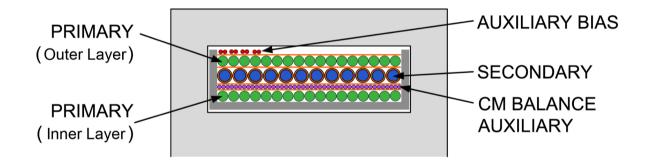
Transformer CM noise analysis – PMP21479 ACF

Note that primary and secondary waveforms are inverse of each other



Transformer CM balance – PMP21479 ACF

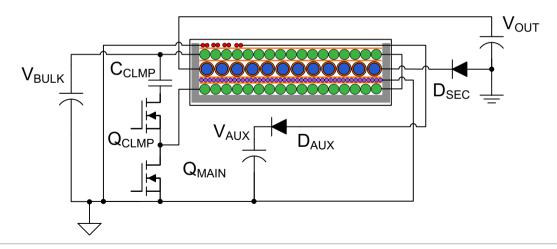
- Add CM balance auxiliary layer (purple) in-between inner PRI (noisier) to SEC interface:
 - Fill layer completely acts as shield between PRI & SEC
 - Add turns to create CM balance, inject current to balance other PRI-SEC interface



- NOTE: this example shows one way to add CM balance
- But there are many different ways to achieve the same CM result

Transformer CM balance – PMP21479 ACF

- PRI, SEC & AUX bias connections same as before
- CM auxiliary layer starts at PRI GND, and winds in SAME direction as SEC

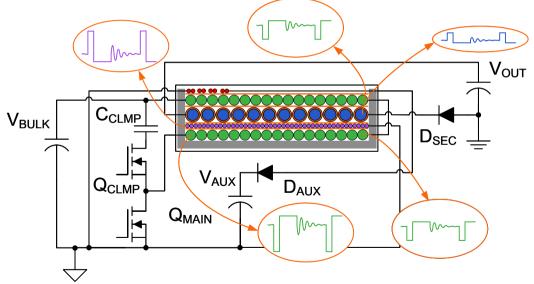


Transformer CM balance – PMP21479 ACF

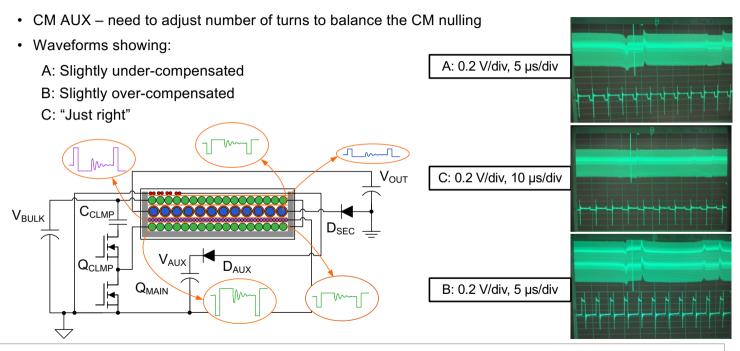
Waveforms – PRI & SEC same as before

CM AUX – same phase as secondary – but amplitude increased to compensate for outer

PRI

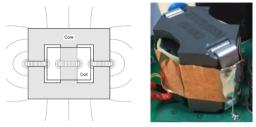


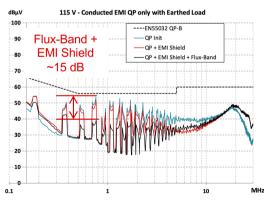
Transformer CM balance – PMP21479 ACF



Transformer "housekeeping" best practices

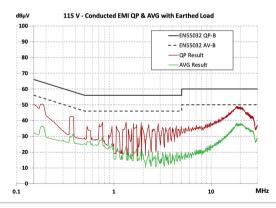
- Center-leg air-gaps only outer legs will radiate
- "Noisier" windings on inside of layer structure
- Tie ferrite core to local primary GND
- Flux-band to minimize stray coupling
 - GNDing & flux-banding can give >10 dB improvement!
- Interleaving trade-offs
 - Lower leakage inductance
 - Higher pri-sec parasitic capacitance, higher CM
- Be aware of internal construction
 - Average CM voltage across the pri-sec capacitance
 - Arrange winding layers to minimize voltage difference
 - Minimizes CM current

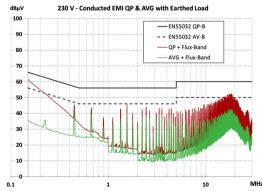




PMP21479 65 W ACF USB-PD – Final result

- Improve transformer structure, add CM balance/shield winding layer
- · Add transformer grounding & flux-banding + EMI shield
- Improve CM choke to bifilar-wound type
- Improve output capacitor location, improve PCB orientation
 - Largely "low-cost" improvements
 - Small efficiency penalty (eddy loss in cancellation layer)









Summary & conclusions

- Consider EMI right from the start inherent part of the power supply design
- Minimize DM & CM EMI noise at source
- DM filter can be designed/calculated/simulated more easily than CM
- CM balance is important as much as practically possible
- Debug to establish if EMI issue is CM or DM or both
- Assess CM performance in time-domain compare different transformers
- For isolated PSU, transformer is most important component
 - Internal construction details, CM balance, shielding, parasitic capacitance, housekeeping
- EMI filter components be aware of parasitics and HF effects
- PCB layout and component placement be aware of stray coupling paths

References

- "Understanding and Optimizing Electromagnetic Compatibility in Switchmode Power Supplies,"
 Bob Mammano & Bruce Carsten, 2002 TI Power Supply Design Seminar.
 - http://www.ti.com/lit/slup202
- "Flyback transformer design considerations for efficiency and EMI," Isaac Cohen & Bernard Keogh, 2016/7 TI Power Supply Design Seminar.
 - http://www.ti.com/lit/slup338
- "Input EMI Filter Design for Offline Phase-Dimmable LED Power Supplies," James Patterson & Montu Doshi, 2012/3 TI Power Supply Design Seminar.
 - http://www.ti.com/lit/slup298
- "Designing low-EMI power converters for industrial & automotive systems," Perry Tsao, David Baba & JP Fung, 2016/7 TI Power Supply Design Seminar.
 - http://www.ti.com/lit/slup362
- "Understanding Noise-Spreading Techniques and Their Effects in Switch-Mode Power Applications,"
 John Rice, Dirk Gerhke & Mike Segal, 2008/9 TI Power Supply Design Seminar.
 - http://www.ti.com/lit/slup269
- "65W Active clamp flyback with Si FETs reference design for a high power density 5-20V AC/DC adapter," PMP21479, Brian King, 2019.
 - http://www.ti.com/tool/PMP21479

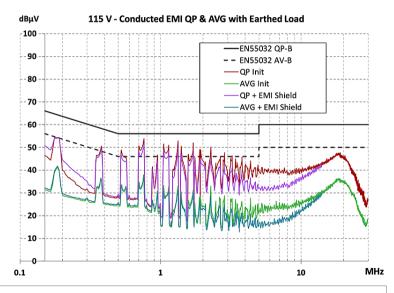
APPENDIX – BACK-UP SLIDES

Transformer flux-band detailed results – 115 V

- EMI shield only (over switch-node and between EMI filter and transformer)
- · NO flux-band, ferrite core floating
- Biggest improvement ~5-8 MHz





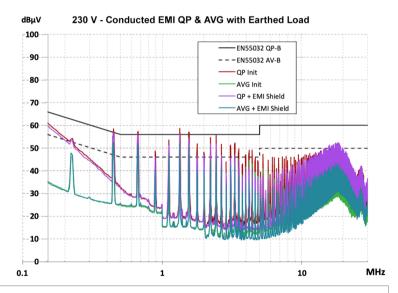


Transformer EMI shield detailed results – 230 V

- EMI shield only (over switch-node and between EMI filter and transformer)
- · NO flux-band, ferrite core floating
- Biggest improvement ~3-8 MHz



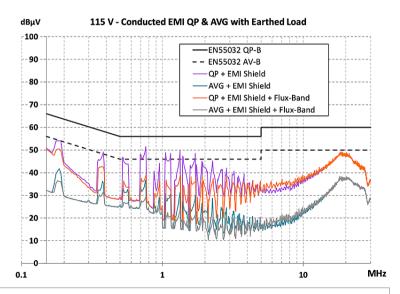




Transformer flux-band detailed results – 115 V

- EMI shield only (over switch-node and between EMI filter and transformer)
- Add flux-band, connected to local primary GND
- Much more significant reduction from 150 kHz to ~4 MHz



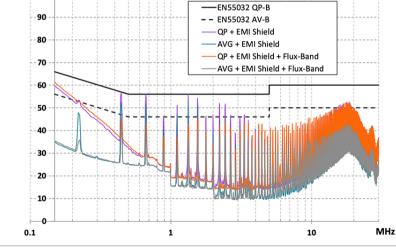


Transformer flux-band detailed results – 230 V

dBμV

- EMI shield only (over switch-node and between EMI filter and transformer)
- Add flux-band, connected to local primary GND
- Much more significant reduction from 150 kHz to ~4 MHz

 Especially for AVERAGE, which is much tougher at 230 V



230 V - Conducted EMI OP & AVG with Earthed Load

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Tl's products are provided subject to Tl's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such Tl products. Tl's provision of these resources does not expand or otherwise alter Tl's applicable warranties or warranty disclaimers for Tl products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2020, Texas Instruments Incorporated