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On Package Characterization using Various Thermal Metrics

Package Technology Group

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Li Zhang, National Semiconductor Corp.

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Package Thermal Characterization: Why So Important?

- **The die temperature needs to be maintained below its design limit (125 C to 150C) in order to guarantee the proper functioning of the circuit**

- **Device long-term reliability is inversely proportional to the operating temperature of the silicon device (by Arrhenius equation)**

- **By creating thermal mismatch at interfaces, high temperature is the main cause of stress/fatigue-related failures**

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Goal of the Thermal Characterization

- **To predict the die temperature by providing thermal resistance between the die and a reference location, where the temperature can be easily measured.**

$$\theta_{J-X} = \frac{T_J - T_X}{P}$$

T_J : Junction or die temperature (^oC)
T_X : Temperature at location "X" (^oC)
P : Power exchange between junction and location X (W)

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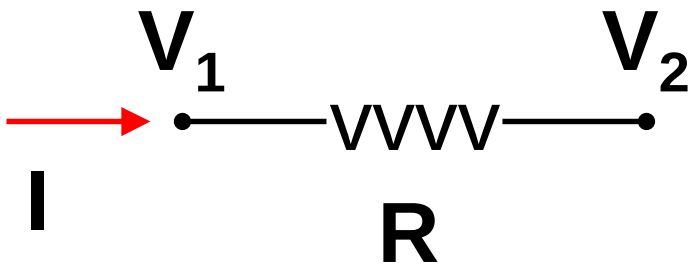
Analogy between thermal and electrical resistance

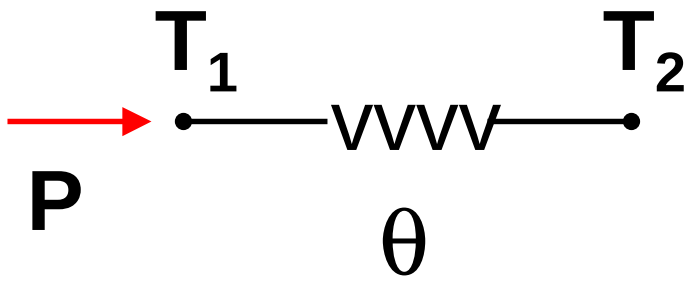
Electrical Resistor



$$R = (V_1 - V_2) / I$$

$$I \times t = Q$$

Thermal Resistor



$$\theta = (T_1 - T_2) / P$$

$$P \times t = Q$$

Temperature -> “Thermal potential”
Power -> “Thermal current”
Heat -> “Electrical charge”

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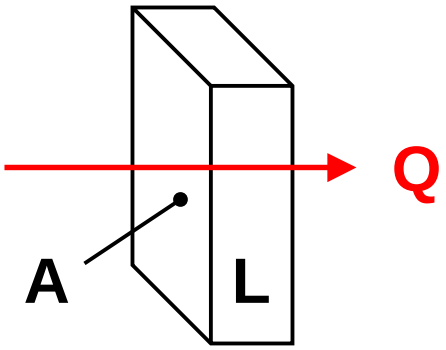
Thermal resistance for simple geometry

Conduction

$$Q = kA\frac{\Delta T}{L}t$$

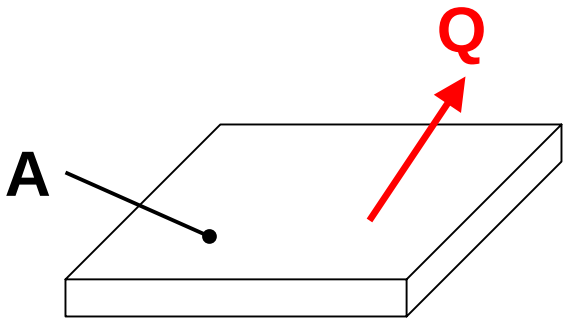


$\theta = L/kA$

k: thermal conductivity: material properties

Convection

$$Q = hAt\Delta T$$

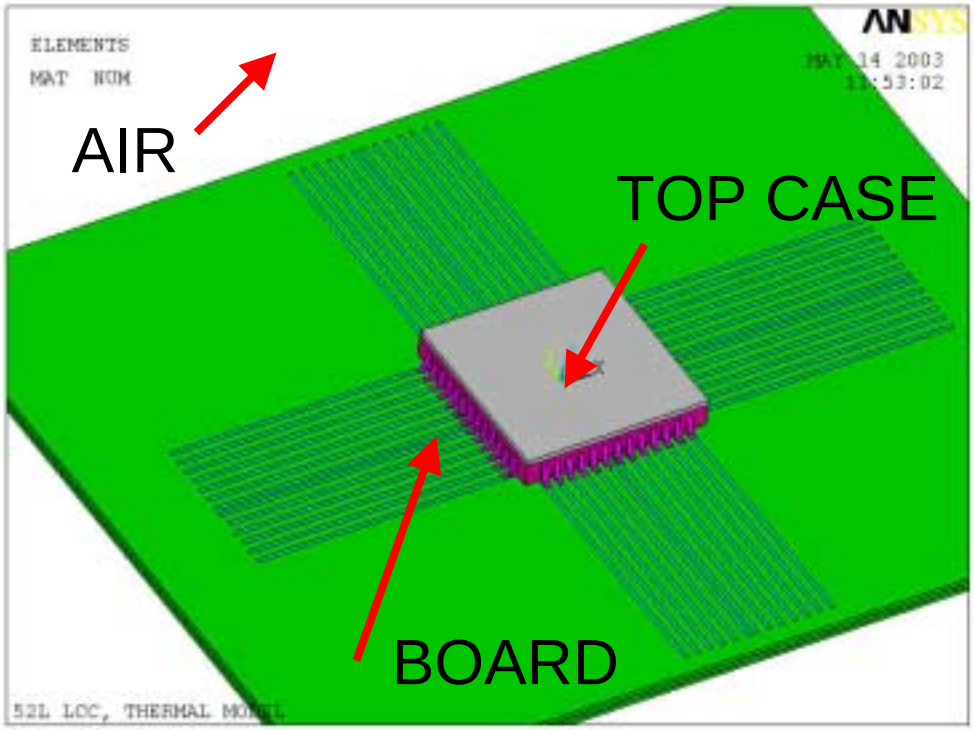


$\theta = 1/hA$

h: heat transfer coefficient

Partial differential equations need to be solved for complex geometry

Thermal Resistance by Reference Locations



Ambient Air	Package Case	Board
θ_{JA}	θ_{JC} ψ_{JT}	θ_{JB} ψ_{JB}

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Difference between Θ type vs. ψ type parameter?

$$\theta_{JX} = \frac{T_J - T_X}{P} \qquad \psi_{JX} = \frac{T_J - T_X}{P}$$

Θ type

- **All heat flows from junction to location X *(which remains isothermal)***
- **Location X serves as external heat sink to the package**

Ψ type

- **Only a fraction of heat flows from junction to location X *(non-isothermal)***
- **Temperature gradient exists in location X *(different points have different temperature readings)***

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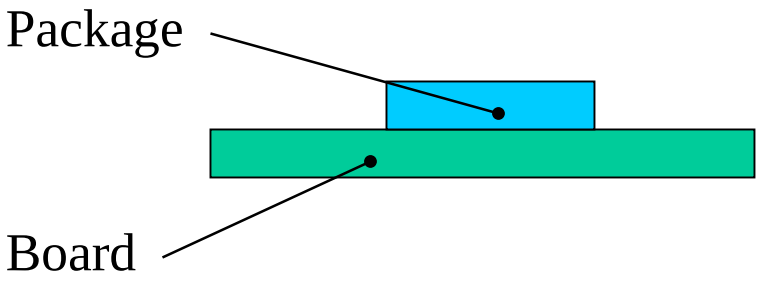
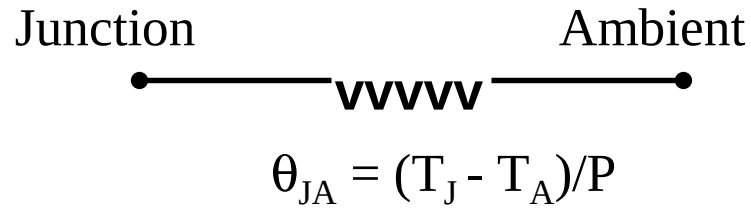
Explanation of Θ_{JA}

- **Mount package on a *standard* board (defined in JESD51-3,-7 -9)**
- **Use a *standard* test environment (wind tunnel or JEDEC cube)**
- **Apply known amount of power to the package**
- **Measure junction temperature and surrounding air temperature**
- **The lower, the better!**
- **Value is *strongly* board-dependent**





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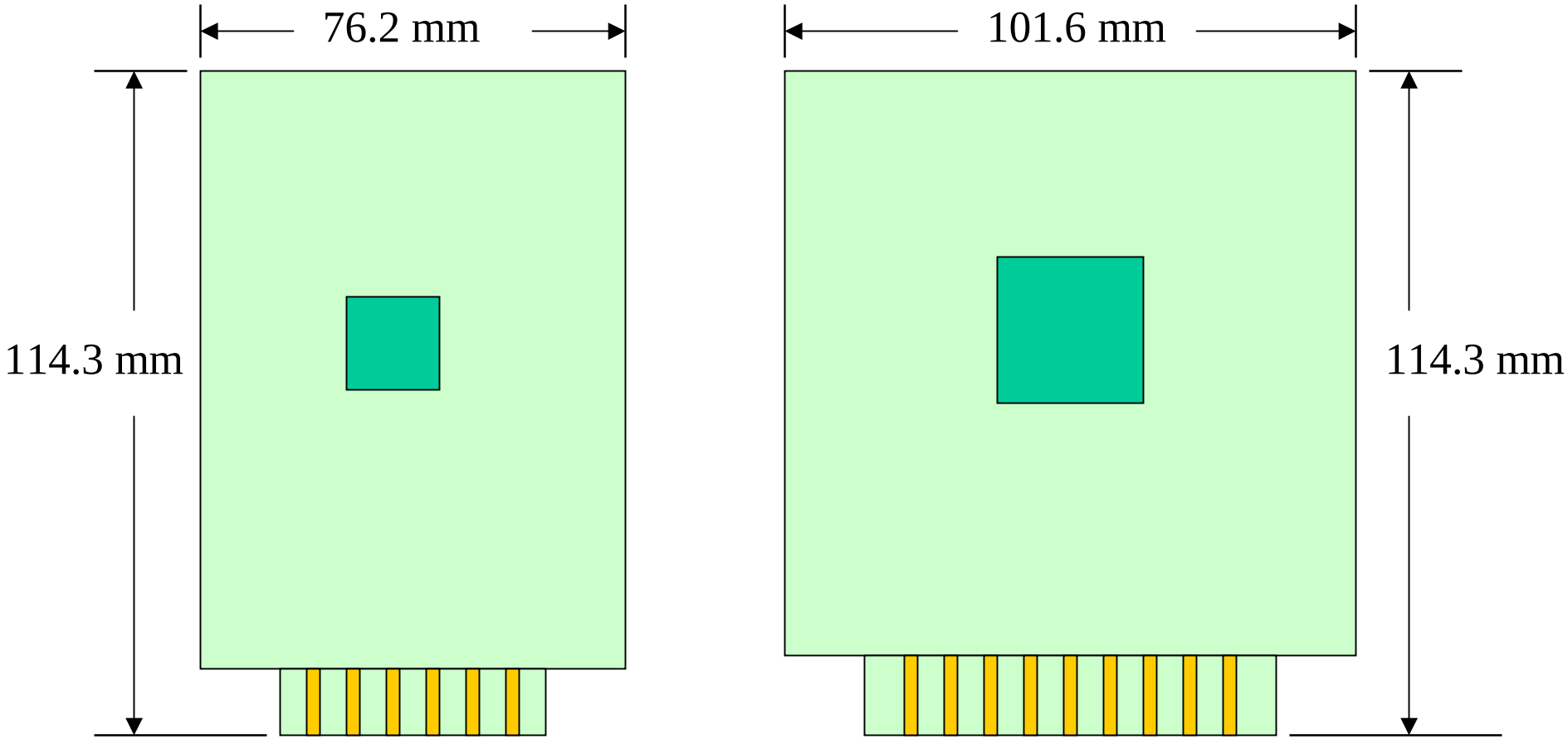
Applications of Θ_{JA}

- **Used to rate different packages in terms of their thermal performance**

- **Occasionally, may be used to predict junction temperature if application environment is similar to test environment (Not recommended and use with great caution! May yield wrong answer due to difference in two environments)**

$$T_j = \Theta_{JA} x POWER + T_{AIR}$$

Recommended boards for JA test

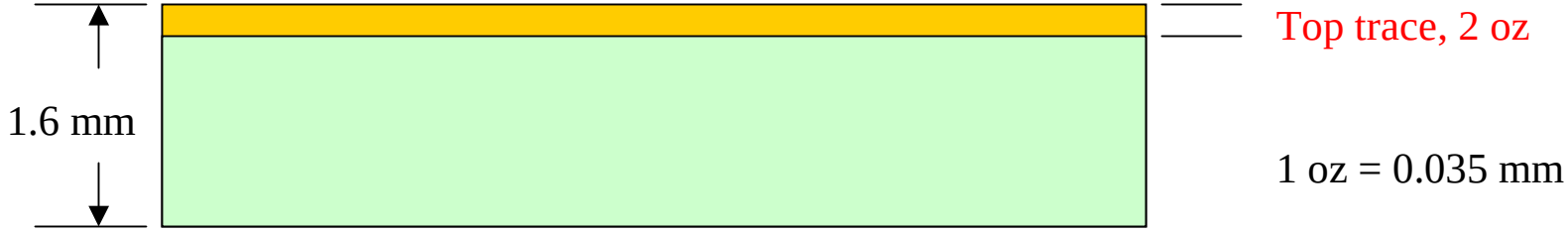


Packages < 27 mm x 27 mm

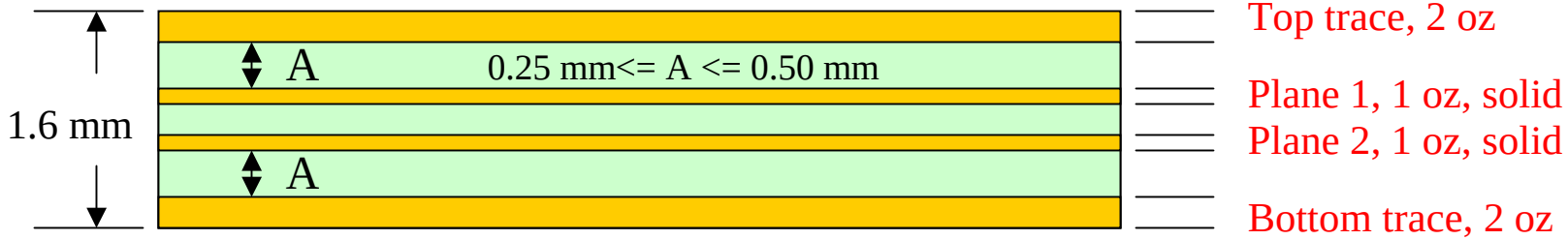
Packages > 27 mm x 27 mm

Recommended boards for JA test (cont.)

Low effective thermal conductivity test board (JESD51-3)



High effective thermal conductivity test board (JESD51-7)



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Explanation of Θ_{Jc}

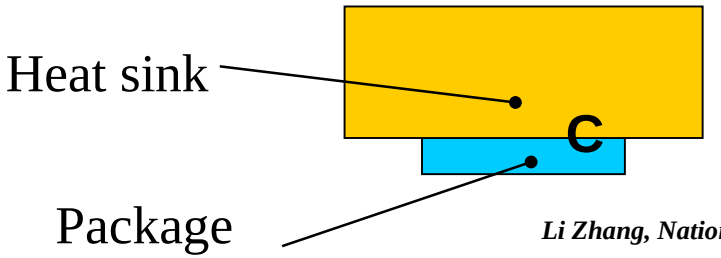
- **Does not need a board in most cases (stand-alone package)**

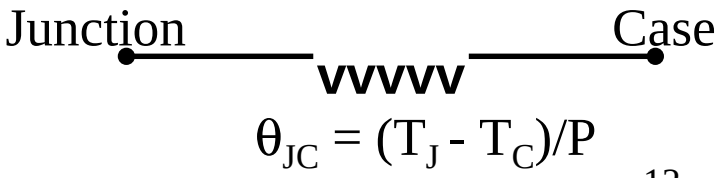
- **Contact the package outer case (top or bottom depending on package structure) on a external heat sink**

  - **Thermally Insulate packages on all other sides**
  - **Force all heat to flow from junction to outer case**

- **Apply known amount of power**

- **Measure junction temperature and case temperature (ideally should be equal to heat sink temperature)**





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Applications of Θ_{JC}

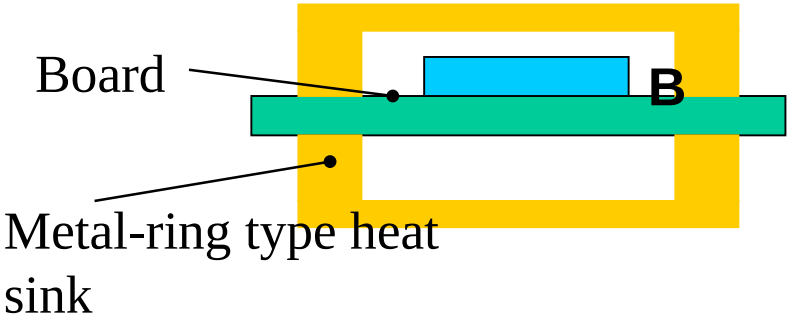
1. **Applicable only to situations where all or nearly all of the heat is flowing through top or bottom of the package (to an external heat sink)**

2. **May be used to predict junction temperature by measuring top/bottom case temperature (Not recommended and use with great caution! May yield wrong answer if #1 condition is not satisfied)**

$$T_j = \Theta_{Jc} x POWER + T_{case}$$

Explanation of Θ_{JB}

- **Mount the package on a standard board**
- **Use a metal-ring type heat sink to clamp the board by sides**
- **Put a thermocouple on board at edge of package**
- **Force all heat to flow from junction to board**
- **Measure junction temperature and board temperature**
- **Value is board-independent**



$\theta_{JB} = (T_J - T_B)/P$

* P : Total power dissipation

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Applications of Θ_{JB}

- **Measures how well heat flows from the junction to the board**

- **May be used to predict junction temperature (may not be as accurate as Ψ_{JT})**

- **PTG currently does not have test-setup for Θ_{JB}**

$$T_j = \Theta_{JB} x POWER + T_{Board}$$

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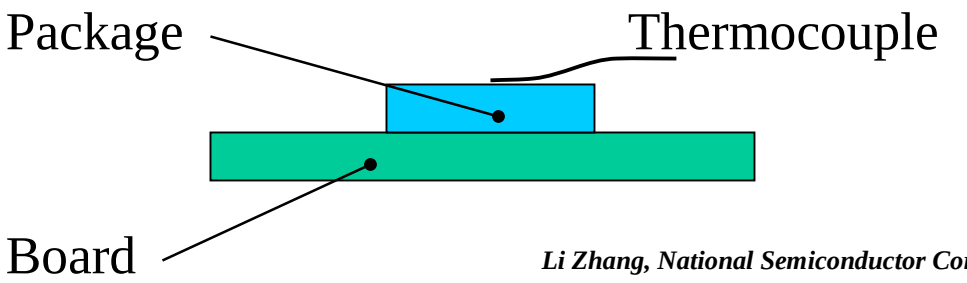
Explanation of Ψ_{JT}

- **Follow exactly the same procedure for Θ_{JA} except:**

- **Measure the top case temperature instead of ambient air temperature**

- **Perform calculation: $\Psi_{JT}=(T_j-T_t)$/TOTAL POWER**

- **Value is *somewhat* board-dependent**



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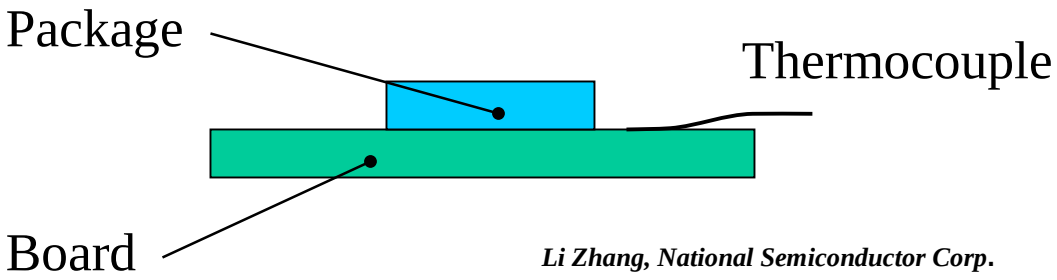
Explanation of Ψ_{JB}

- Follow exactly the same procedure for Θ_{JA} except:
- Measure the board temperature instead of ambient air temperature
- Board temperature measured at a trace connecting the middle lead on the longer side of the package
- Perform calculation: $\Psi_{JB}=(T_j-T_B)/\text{TOTAL POWER}$
- Value is ***somewhat*** board-dependent



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Applications of Ψ_{JT}/ Ψ_{JB}

- **Are not true thermal resistances**
- **Total power is used because it is what is known**
- **Usually, only part of total power flows from junction to top case or board**
- **Used to estimate junction temperature by measuring top-center case temperature or board temperature**

$$T_j = \Psi_{JT} x POWER + T_{case}$$

$$T_j = \Psi_{JB} x POWER + T_{Board}$$

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How to get thermal resistance values

- Check out our thermal webpage first! (http://ptg.nsc.com/thp)
- Thermal measurement at thermal lab (Noella Jeeves)
- Computer simulation using finite element analysis (Li Zhang)
- Equivalent thermal resistor network model (Li Zhang)

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Thermal resistances through measurement

Theta JA wind tunnel in the thermal lab

- **Located in South Portland, Maine**
- **Actual package attached to a thermal test board required**
- **Currently can test Θ_{JA} / Θ_{JC} only**
- **Working on establishing procedure for Ψ_{JT}/ Ψ_{JB}**

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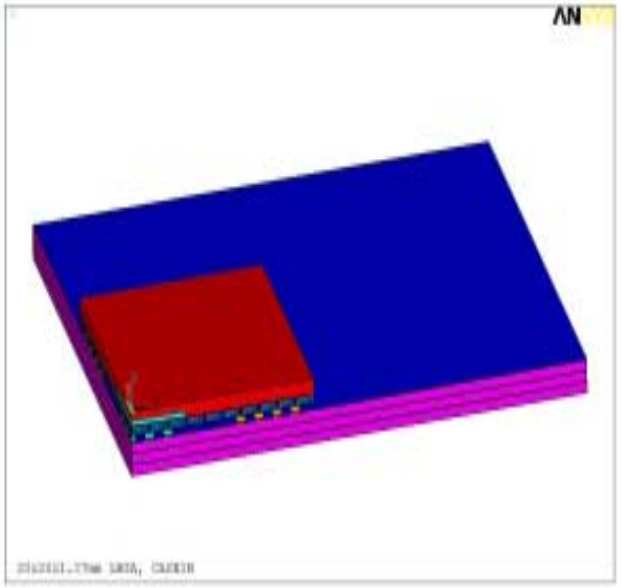
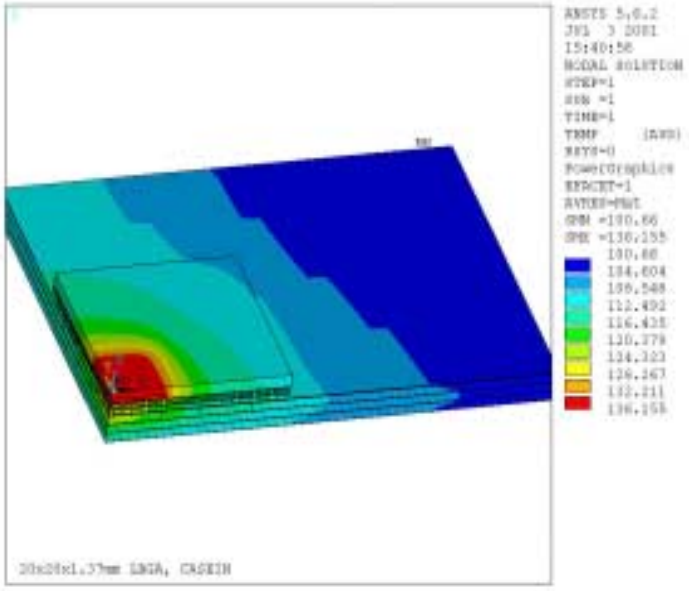
Thermal resistances through simulation



Finite Element Model of a LBGA Package



Calculated temperature profile of the same package

- **Finite element model created for package and the board**
- **Capable of providing all thermal resistances (Θ type or Ψ type)**
- **Error band is +/-15% compared with measurement**
- **Once correlated, valuable tool in the all stages of package development with tremendous saving in cost and time**

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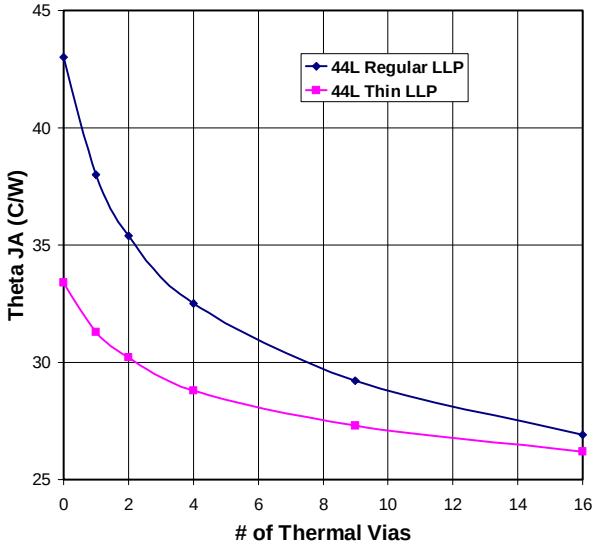
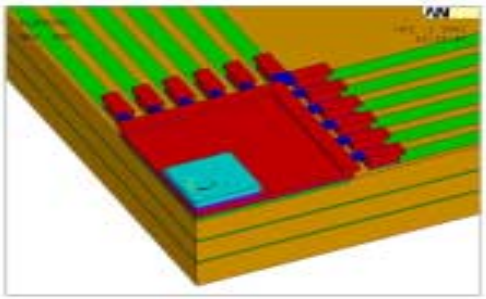
Simulation Examples

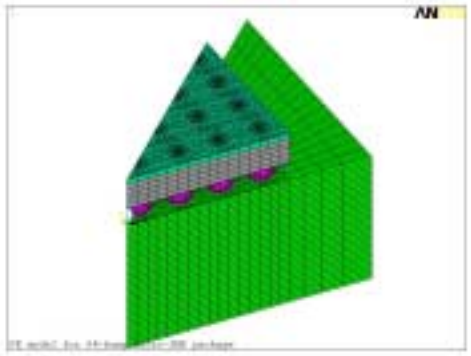
Impact of # of vias on Theta JA for a LLP package

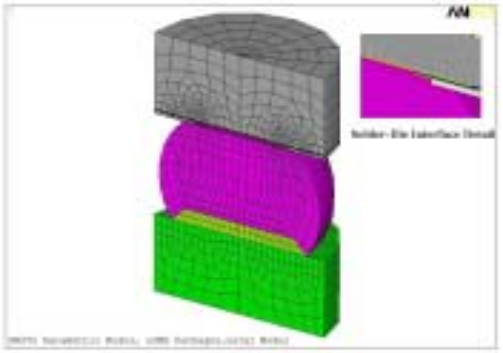




44L LLP

Study on solder fatigue life improvement under temperature cycling condition by increasing the passivation layer opening for a micro SMD package





Bump Count	Package	Fatigue Life	Local/Global Model	Percentage Error
8L	gular Passivati	540	480	11.1
8L	rge Passivatio	930	893	3.9

Cost of testing: 15000$/6 weeks
Cost of simulation: 0$/1 week

Cost of testing: >35 days
Cost of simulation: 6 hours (Does not include model development)

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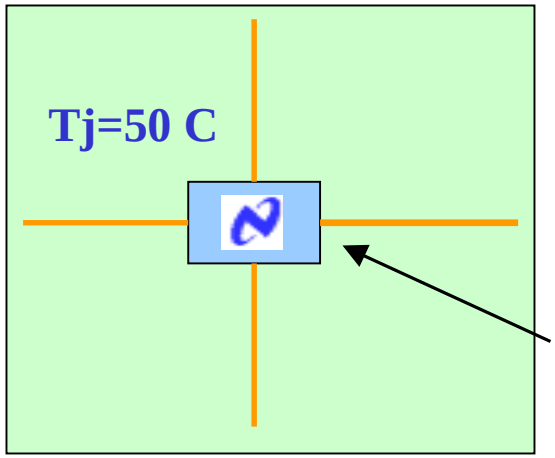
Packaging options that affect the thermal performance

- Die size: the larger, the better
- Package body size: the larger, the better
- Lead/ball count: the more, the better
- Material selection: the higher the thermal conductivity, the better
- The better the package-board thermal connection, the lower the Θ_{JA}
- The more number of layer of the board, the better

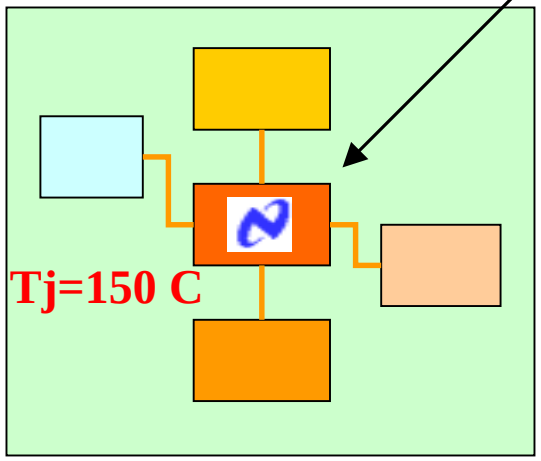
Thermal Analysis: Package Level vs. System Level



Package Level

- Single package (heating component) on board
- Heat removed by convection by surrounding air only
- Finite Element Analysis

Same package, different temperature, what is wrong?!!



System Level

- Multiple packages on board
- Complicated boundary conditions
- Computational Fluid Mechanics (CFD)
- Responsibility of those who build the system
- As package supplier, NSC provides package-level resistance ONLY

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Thermal Exercises

- **Package A has ΘJA of 40 C/W, Package B has ΘJA of 60 C/W. Which one has better performance?**
  - **Answer: incomplete information, need to know board condition/environmental condition**
- **Customer measured the top case temperature of a package to be 50C, ΘJC, ΨJT and ΨJB for the package are 30 C/W,5 C/W and 20 C/W,respectively. It is also known that package dissipates 1.5W. What is the best estimate for junction temperature?**
  - **Answer: 57.5 C**
- **2 different silicon dies can fit into the same package, it is known that both dies dissipates the same amount of power but die A is much larger than die B, which one is likely to have lower ΘJA?**
  - **Answer: die A**

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Summary

- The goal of the package thermal characterization is to provide appropriate thermal resistances between junction and a reference location

- The reference location can be ambient air, top case or board

- The most commonly used thermal resistance include ΘJA, ΨJT and ΨJB

- ΘJA is used to compare thermal performance between different packages. It is strongly board dependent

- ΨJT and ΨJB are often used to predict the junction temperature in end user environment

- Check PTG's thermal page at http://ptg/thp first if you have questions