Testing with Picoscope 4-channel

Notebook:	Automatic Hen Door Opener		
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Testing with Picoscope 4-channel
Ch A **Blue**: FAULTn 1.2K ohm pull-up to Vcc
Ch B **Red**: Isense across 0.56 ohm R13 (reduced to prevent motor forward/backward tripping)
Ch C **Green**: IN2 - ignore Y-values, as the display is offset
Ch D "**Yellow**": IN1 - ignore Y-values, as the display is offset

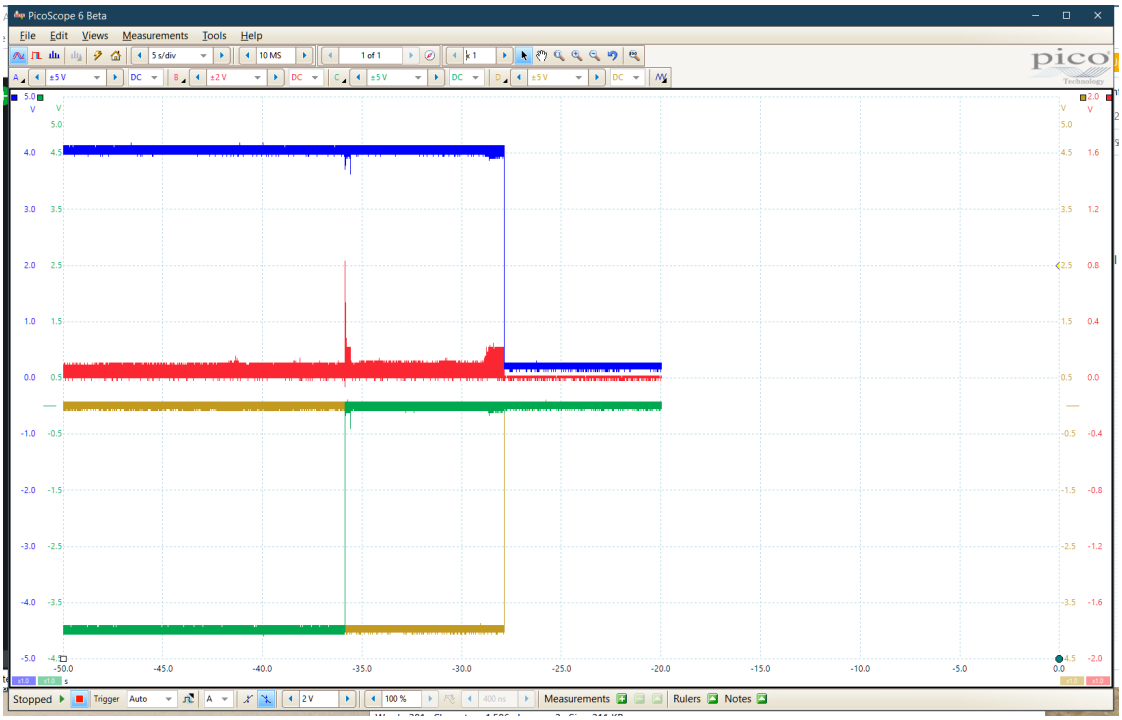
Problem: After a STALL then FAULTn does not de-assert itself as expected, so is this an OCP derived fault?

Vcc on the board is approx 4 Volt. Current PCB design cannot completely isolate Vcc to the DRV8832 as it seems to be held at about 50% Vcc by logic gates HIGH output into IN1 and IN2.

- Next iteration of the PCB would need 3-state gates with EN (when FAULTn is negated HIGH).

Normal use as a door opener is maybe three or four times per day, door movement operation completes in about 10 seconds.
A manual override Push-Button can independently operate the door forward and reverse (so IN1 and IN2 are toggled simultaneously).

TEST JIG:
Motor is loaded with a test jig and Magnetic Slip Clutch to simulate normal load conditions.
Then continually put into FORWARD then REVERSE (as Push-Button above) to monitor Isense when IN1 and IN2 alternate.



Resulting display above is Fig 1. which gives an overview of the overall result

Zooming in on the details (see Fig 2. below) as follows reveals:

1. An average of 120mV across Rsense (0.56 ohm)
2. Spikes in Isense seen as 900mV peak across Rsense when motor is reversed.
3. No OCP or other fault condition generated.

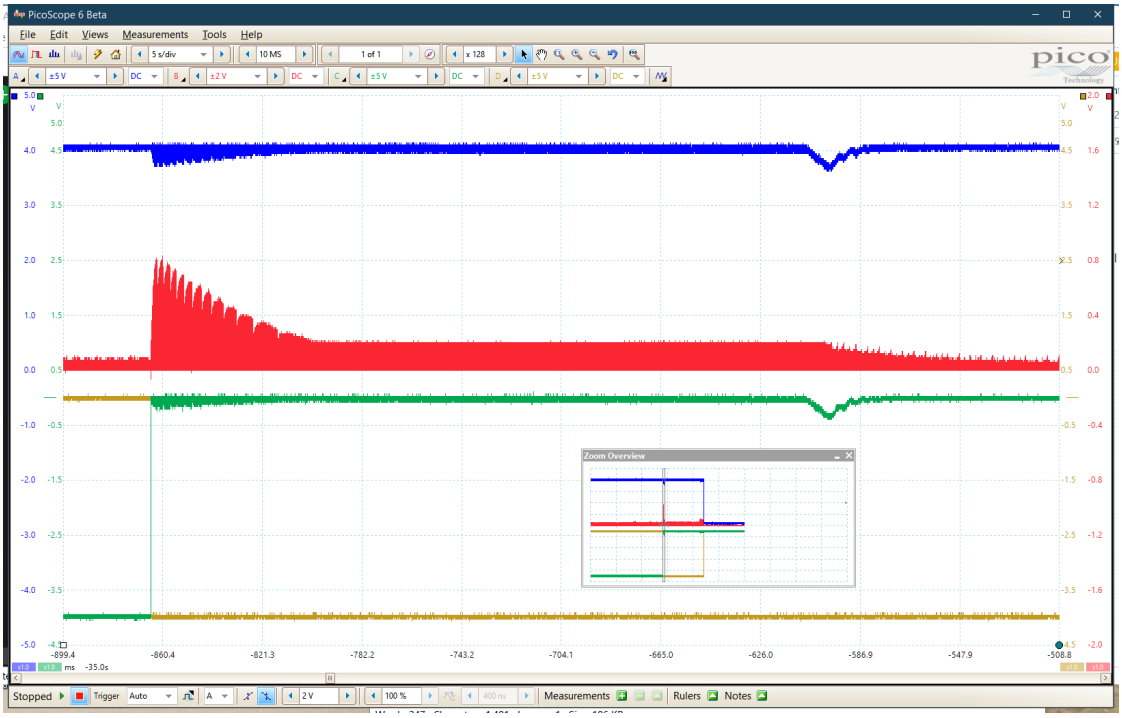


Fig 2. above: Zoom into the details of Fig 1.to see motor reversal "current" spikes

The motor is then stalled to see the FAULTn generation and Isense current, see Fig 3 below.

1. Voltage across Rsense rises to 200mV peak (as per datasheet V_{ILIM} 200mV typ.)
2. FAULTn is asserted
3. Logic gates put IN1 and IN2 both HIGH for a BRAKE condition
4. No spikes prior to FAULTn assertion
5. FAULTn is not released after the BRAKE halts the motor

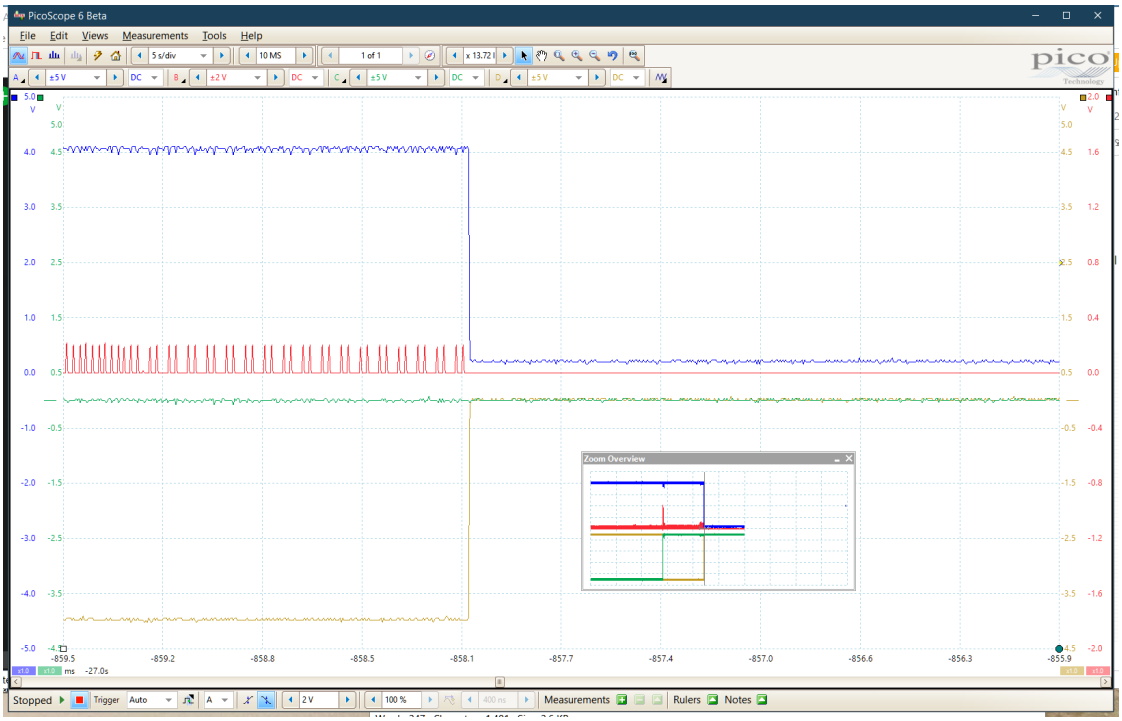


Fig 3. above is a zoom of the Fig 1 at the FAULTn assertion.

Conclusions so far:

1. This motor definitely needs a lower value of Rsense, from 0.91 ohm to 0.56 ohm. But any lower then the motor torque at stall would be too great, trying to protect a living body.
2. The motor reversal generates high currents but these seem to be controlled by the DRV8832 PWM(?) and stay within any OCP trip levels, so no FAULTn assertion.
3. A real stall does not generate any current spikes just an average current increase which causes a rise in V_{ILIM} to 200mV then FAULTn is asserted as expected.
4. When the motor is put into BRAKE mode due to the STALL then the FAULTn does **not** reset as expected.

A curious phenomenon (see Fig 4. below), FAULTn occasionally (sometimes consecutively) asserts itself before a motor operation, the logic gates then put IN1 and IN2 HIGH to BRAKE, but FAULTn immediately de-asserts itself and the motor operation starts normally.

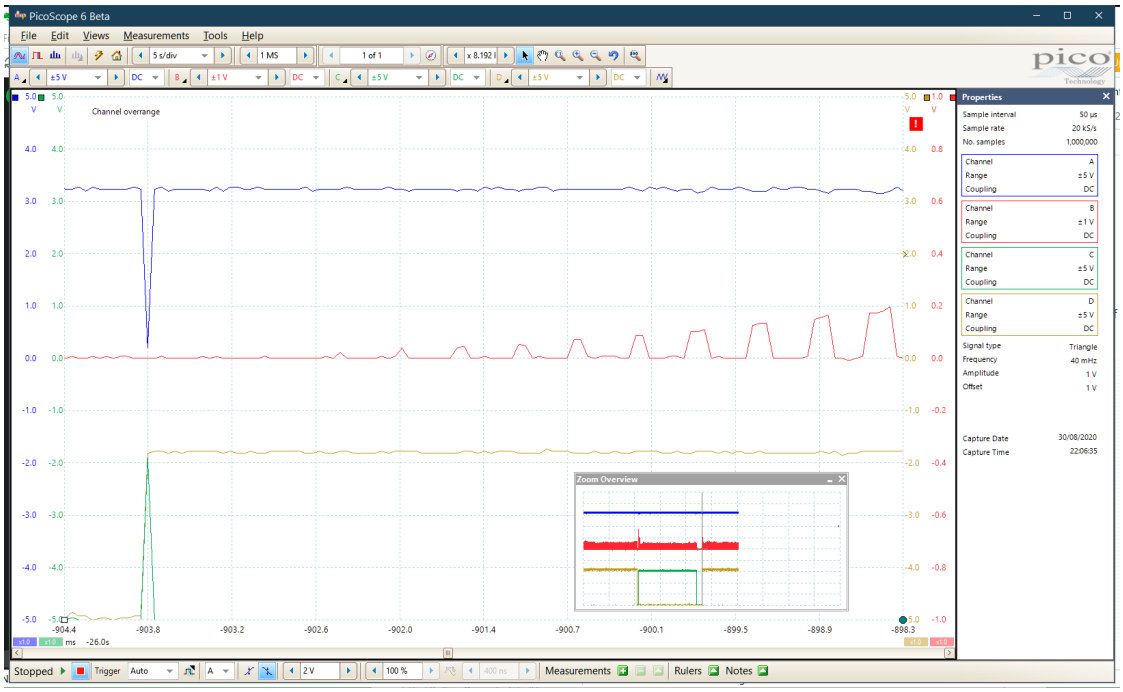


Fig 4. Spurious FAULTn assertion. This one at Vcc = 3.2V.