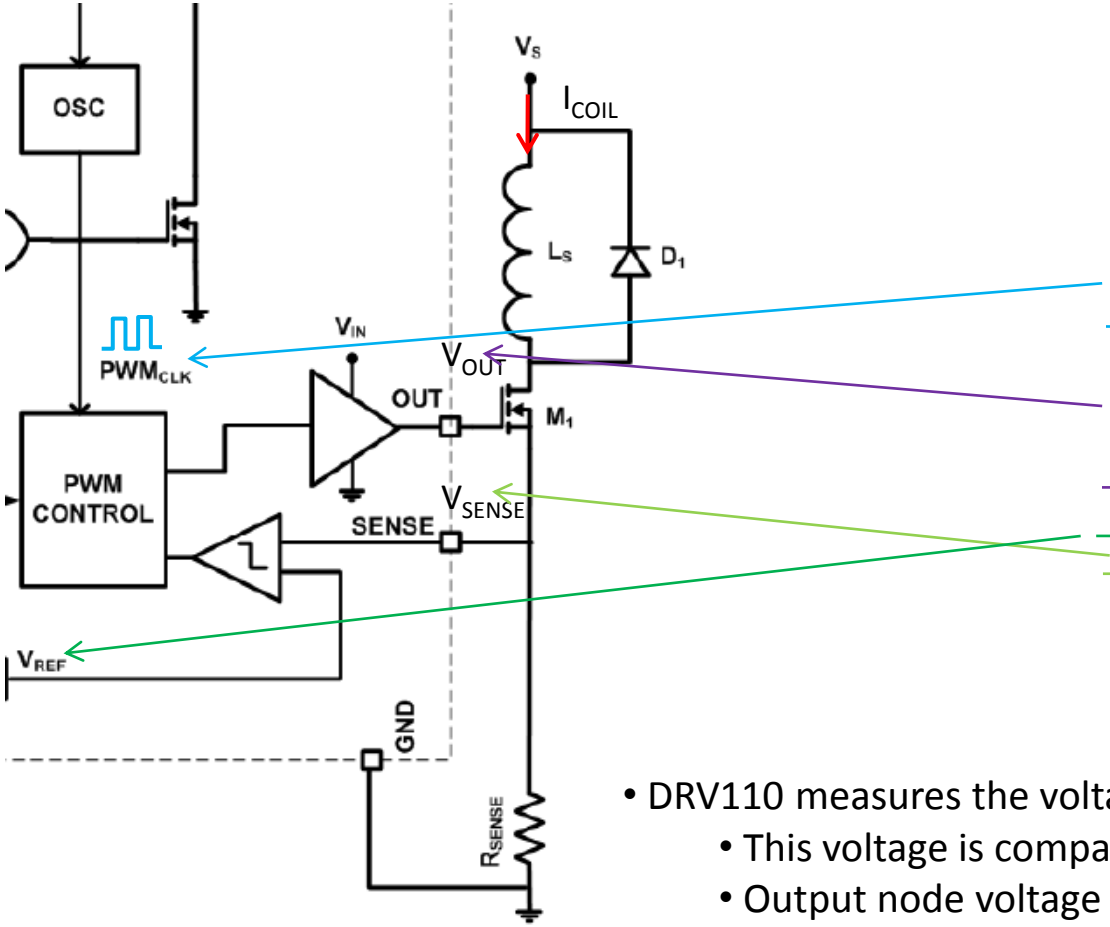
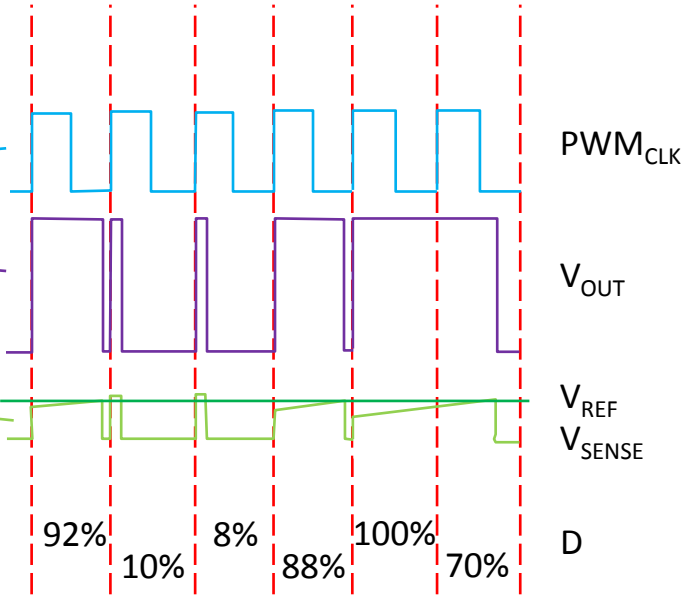
DRV110 Non-Uniform PWM Explanation

Current Control of DRV110

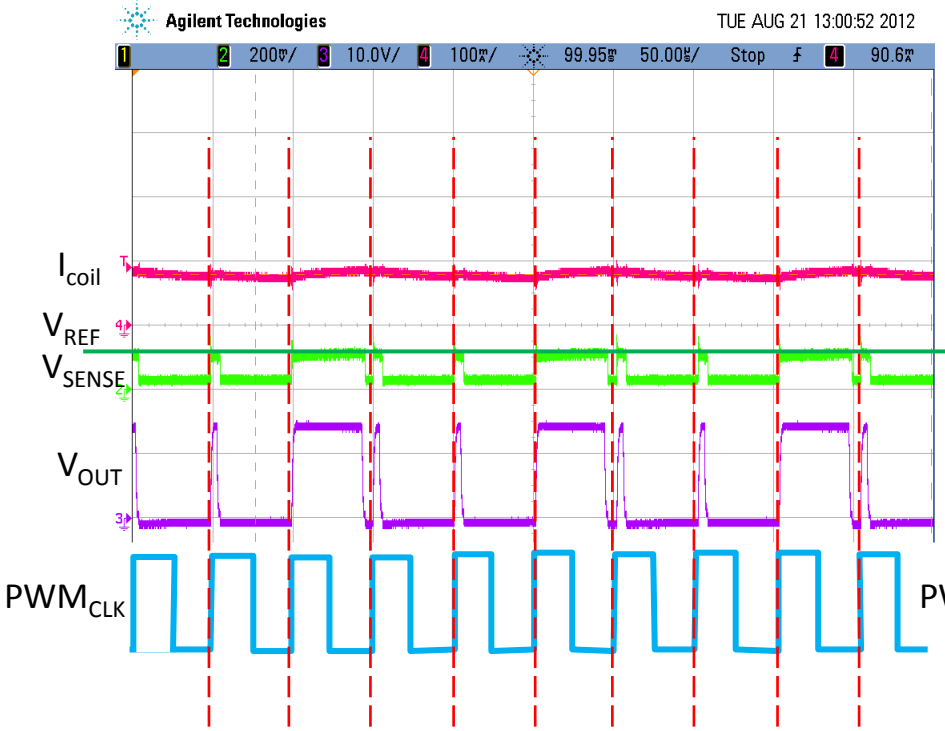




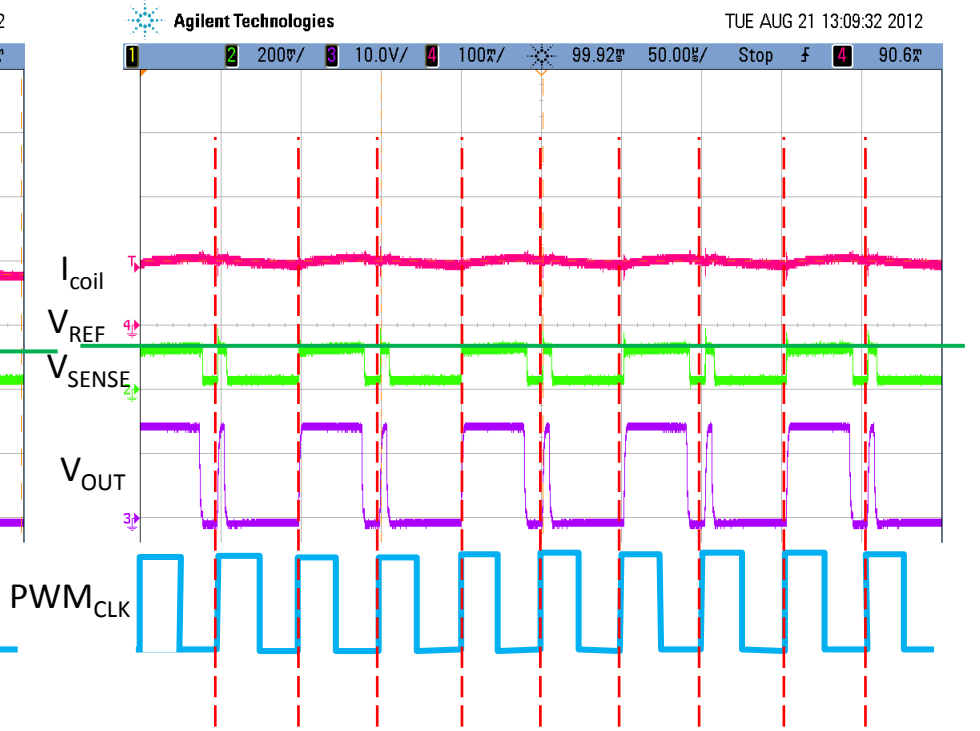
- DRV110 measures the voltage V_{SENSE} at SENSE node
  - This voltage is compared against V_{REF} every clock cycle
  - Output node voltage V_{OUT} will go low when $V_{SENSE} \geq V_{REF}$
  - Duty cycle D of V_{OUT} will vary between 8% and 100%
- Summary: V_{SENSE} is sampled after every rising edge of PWM_{CLK} and will go low only after $V_{SENSE} \geq V_{REF}$
  - Minimum D=8%

Measurement Plots Explained – Medium I_{HOLD} Settings

I_{HOLD} = 76.9mA



I_{HOLD} = 90.9mA



- PWM_{CLK} is internal PWM clock signal, not visible outside
- Decision made by current control during <u>every</u> clk cycle (50us interval for PWM 20kHz frequency)
  - At least ~8% (duty cycle) pulse given out every clock cycle
  - Duty cycle can go up to 100%, even for several consecutive clk cycles
    → <u>V_{out} signal does not always show the PWM frequency, especially with high I_{HOLD} settings</u>
  - Note that the sensing comparator has also tens of mV hysteresis

Measurement Plots Explained – High I_{HOLD} Setting

- Duty cycle explained for each PWM cycle of the I_{HOLD} =142.8mA setting
  - Measured value 151mA
    - Accuracy ~6%
    - In line with data sheet
  - As seen from the individual duty cycle values, duty cycle can for each pulse
    - Due to cycle-by-cycle control of V_{SENSE} against V_{REF}
    - Duty cycle depends on the inductance and on-resistance of the coil
    - This control helps to reduce EMI issues
- Internal PWM clock PWM_{CLK} is fixed frequency, but this signal not visible outside of IC
- If you want to verify the f_{PWM} setting, need to use so small I_{HOLD} setting that you always have duty cycle <100%

I_{HOLD} = 142.8mA