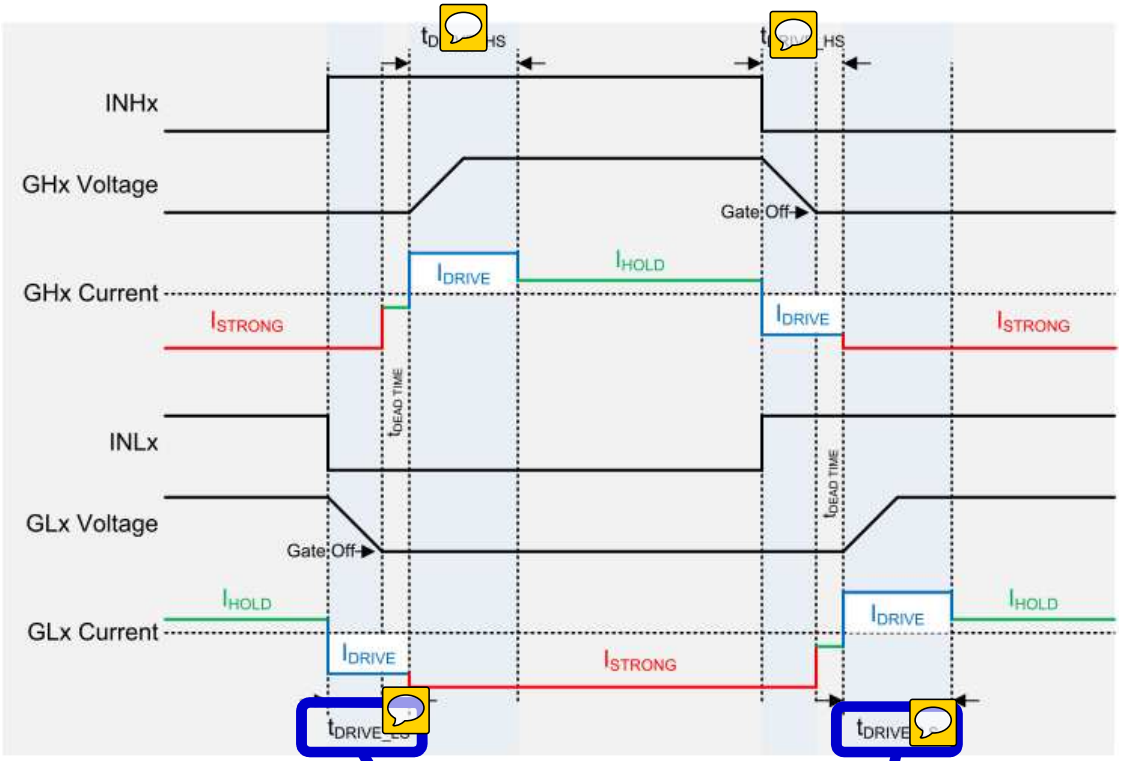

Figure 11. TDRIVE Gate Drive State Machine

7.6.2.1 HS Gate Drive Control (Address = 0x5)

Table 14. HS Gate Driver Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R/W	RSVD	0x0	-
9:8	R/W	TDRIVEN	0x3	High-side gate driver peak source time b'00 - 220 ns b'01 - 440 ns b'10 - 880 ns **b'11 - 1780 ns**
7:4	R/W	IDRIVEN_HS	0x4	High-side gate driver peak sink current b'0000 - 20 mA / b'0001 - 30 mA / b'0010 - 40 mA / b'0011 - 50 mA **b'0100 - 60 mA** / b'0101 - 70 mA / b'0110 - 80 mA / b'0111 - 0.25 A b'1000 - 0.50 A / b'1001 - 0.75 A / b'1010 - 1.00 A / b'1011 - 1.25 A b'1100 - 60 mA / b'1101 - 60 mA / b'1110 - 60 mA / b'1111 - 60 mA
3:0	R/W	IDRIVEP_HS	0x4	High-side gate driver peak source current b'0000 - 10 mA / b'0001 - 20 mA / b'0010 - 30 mA / b'0011 - 40 mA **b'0100 - 50 mA** / b'0101 - 60 mA / b'0110 - 70 mA / b'0111 - 0.125 A b'1000 - 0.25 A / b'1001 - 0.50 A / b'1010 - 0.75 A / b'1011 - 1.00 A b'1100 - 50 mA / b'1101 - 50 mA / b'1110 - 50 mA / b'1111 - 50 mA

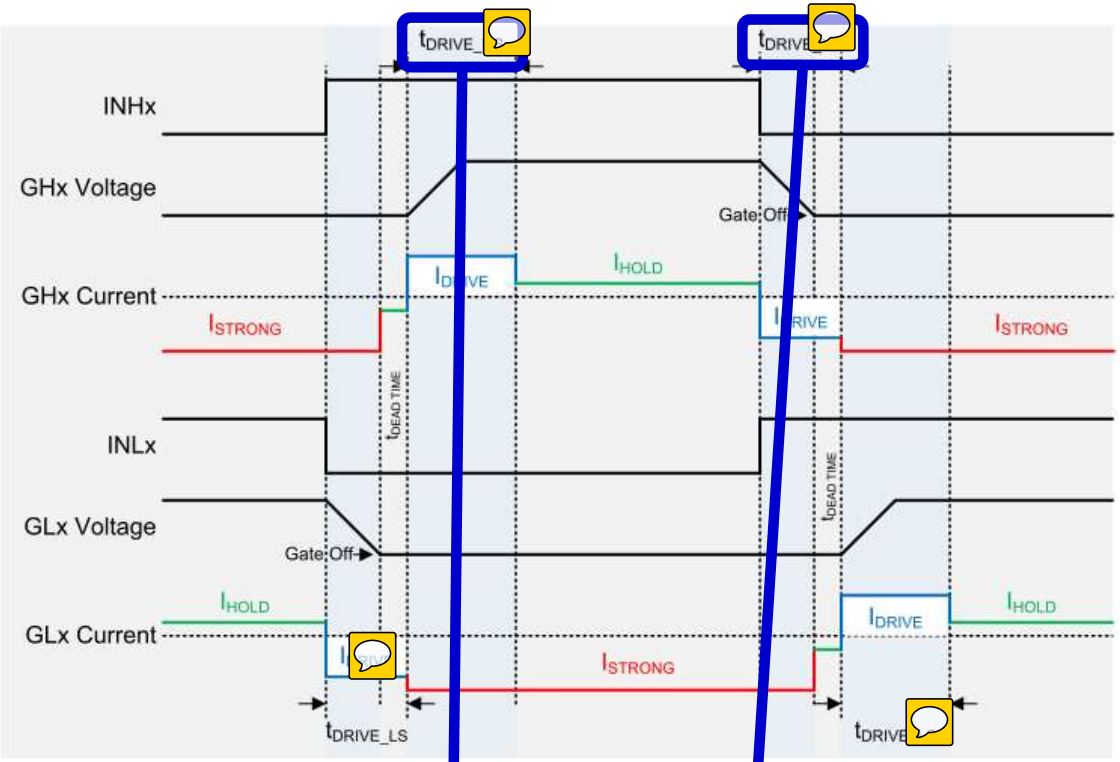

Figure 11. TDRIVE Gate Drive State Machine

7.6.2.2 LS Gate Drive Control (Address = 0x6)

Table 15. LS Gate Driver Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION			
10	R/W	RSVD	0x0	-			
9:8	R/W	TDRIVEP	0x3	Low-side gate driver peak source time b'00 - 220 ns b'01 - 440 ns b'10 - 880 ns **b'11 - 1780 ns**			
7:4	R/W	IDRIVEN_LS	0x4	Low-side gate driver peak sink current			
				b'0000 - 20 mA **b'0100 - 60 mA** b'1000 - 0.50 A b'1100 - 60 mA	b'0001 - 30 mA b'0101 - 70 mA b'1001 - 0.75 A b'1101 - 60 mA	b'0010 - 40 mA b'0110 - 80 mA b'1010 - 1.00 A b'1110 - 60 mA	b'0011 - 50 mA b'0111 - 0.25 A b'1011 - 1.25 A b'1111 - 60 mA
3:0	R/W	IDRIVEP_LS	0x4	Low-side gate driver peak source current			
				b'0000 - 10 mA **b'0100 - 50 mA** b'1000 - 0.25 A b'1100 - 50 mA	b'0001 - 20 mA b'0101 - 60 mA b'1001 - 0.50 A b'1101 - 50 mA	b'0010 - 30 mA b'0110 - 70 mA b'1010 - 0.75 A b'1110 - 50 mA	b'0011 - 40 mA b'0111 - 0.125 A b'1011 - 1.00 A b'1111 - 50 mA