Vin is isolated from VM and VDRAIN because the buck is on a separate die that is integrated into the device. It is the same buck as the LM5008A device.

To understand how VM and VDRAIN interact with the driver it is helpful to look at the below diagram:

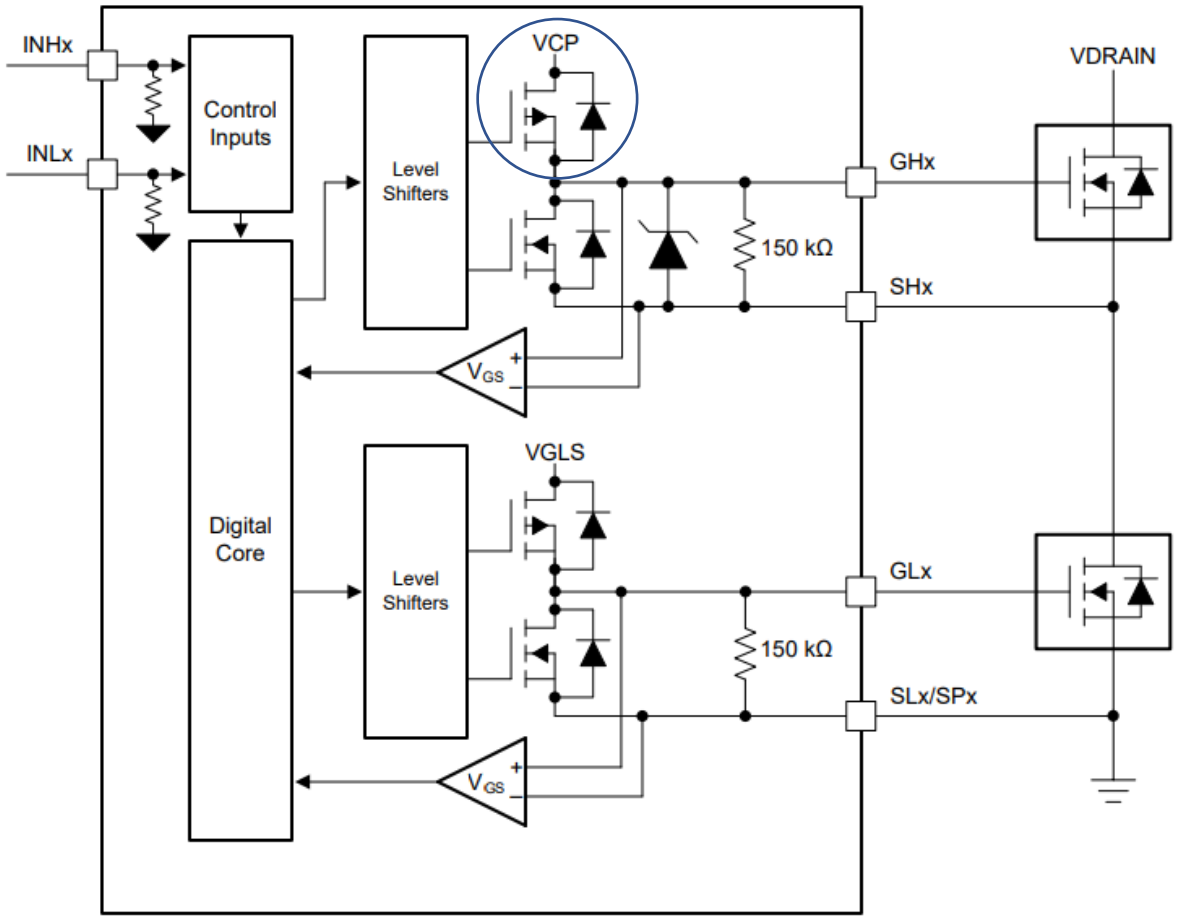

Figure 32. Gate Driver Block Diagram

When an INHx signal comes in to indicate that the high side MOSFET needs to be turned on, the driver turns on the internal high side P-MOS (circled in blue) to supply the VCP voltage to the Gate of the High side MOSFET.

The VCP voltage is generated from VDRAIN using a charge pump architecture as shown below to generate a voltage that is 10.5V above VDRAIN.

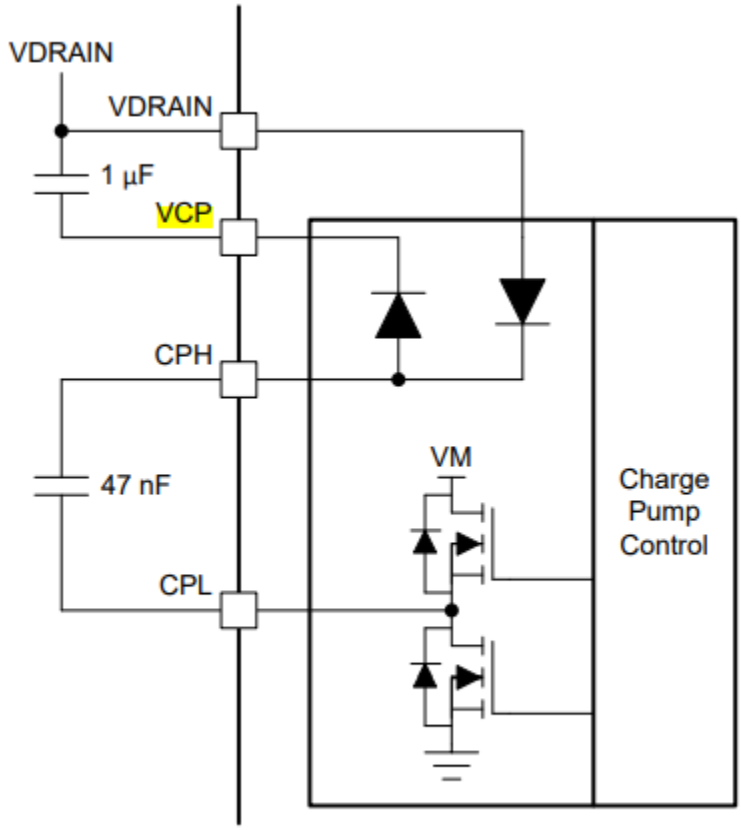

Figure 29. Charge Pump Architecture

This is done by the charge pump control alternately turning on and off the internal high and low side charge pump MOSFETs to supply a PWM of VM to the CPL pin which allows the VCP voltage to shift 10.5V above VDRAIN. **For the charge pump architecture, VM is isolated from VDRAIN by a MOSFET, a capacitor, and a diode.**

VM is also used to generate the 5V DVDD linear regulator as shown in the simplified diagram below. DVDD is used to power much of the internal digital logic of the device. VM is also used to generate the 11V VGLS linear regulator voltage that is used to turn on and off the low side external MOSFET.

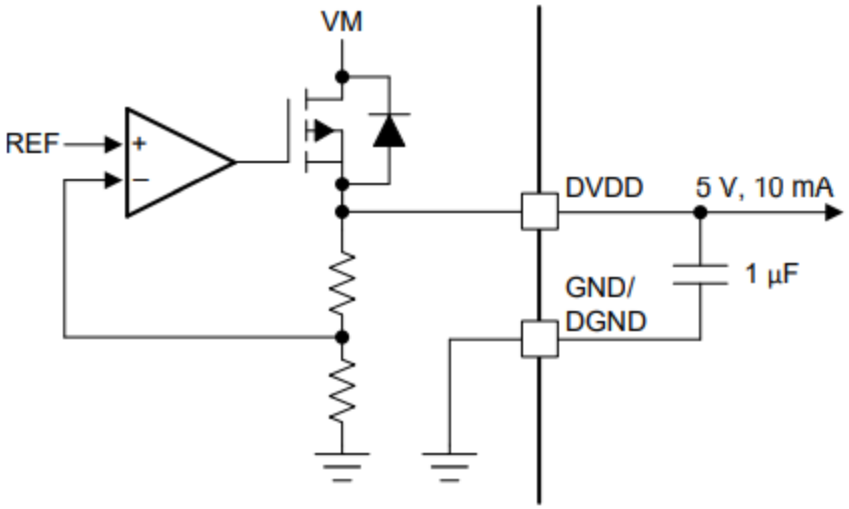

Figure 36. DVDD Linear Regulator Block Diagram

Finally, as shown below and circled in blue, the VDRAIN pin is connected to an internal comparator to monitor the drain to source voltage of the high side MOSFET.

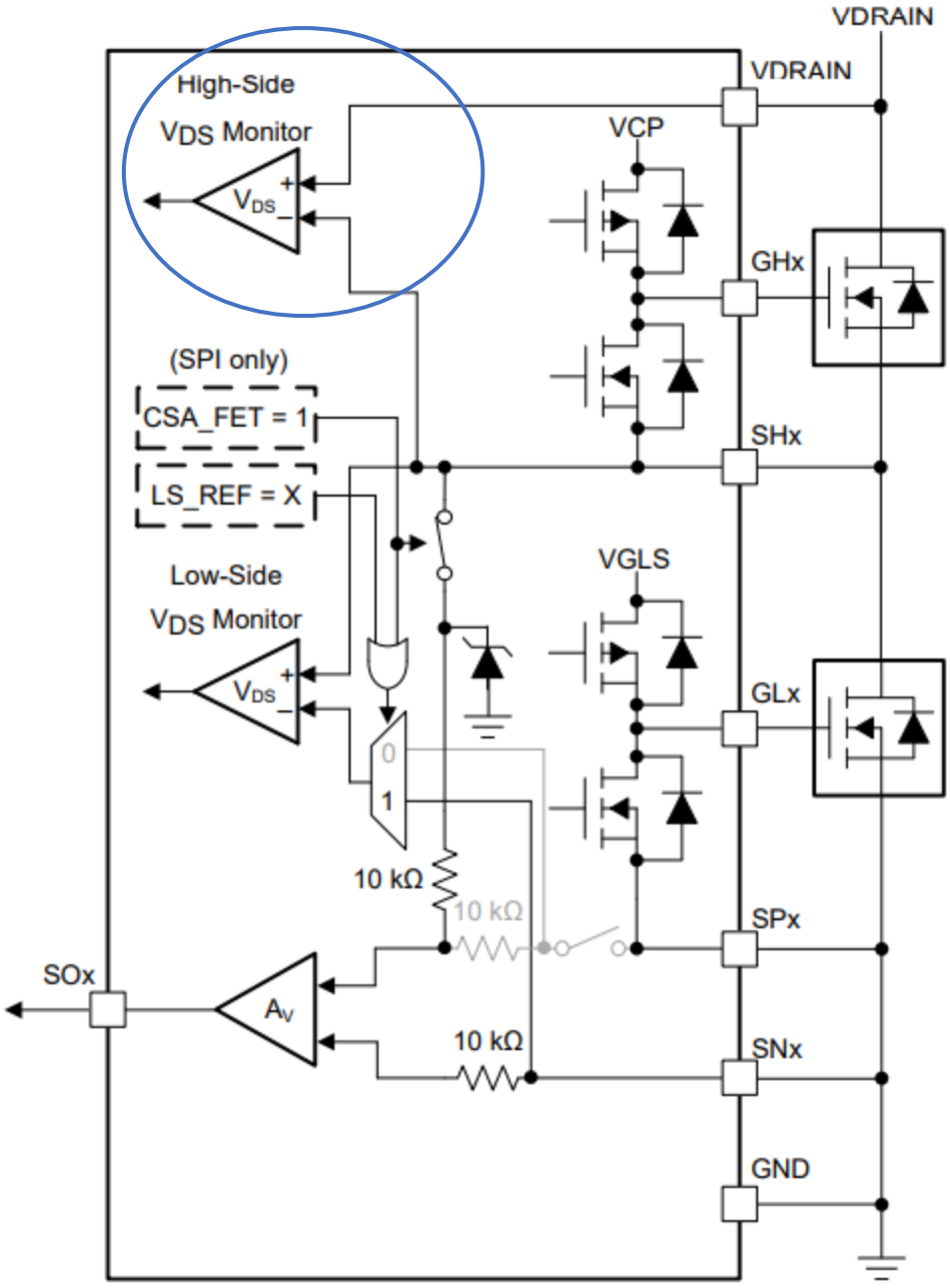

Figure 49. V_{DS} Sense Configuration