A screenshot of a computer

Description automatically generatedGraphical user interface, application

Description automatically generatedGraphical user interface, application

Description automatically generatedtSCLK minimum period = 100 ns. The measured value is 500 ns. OK

tSCLKH minimum high time = 50 ns. The measured value is 244 ns. OK

tSCLKL minimum low time = 50 ns. The measured value is 136 ns. OK

Graphical user interface, application

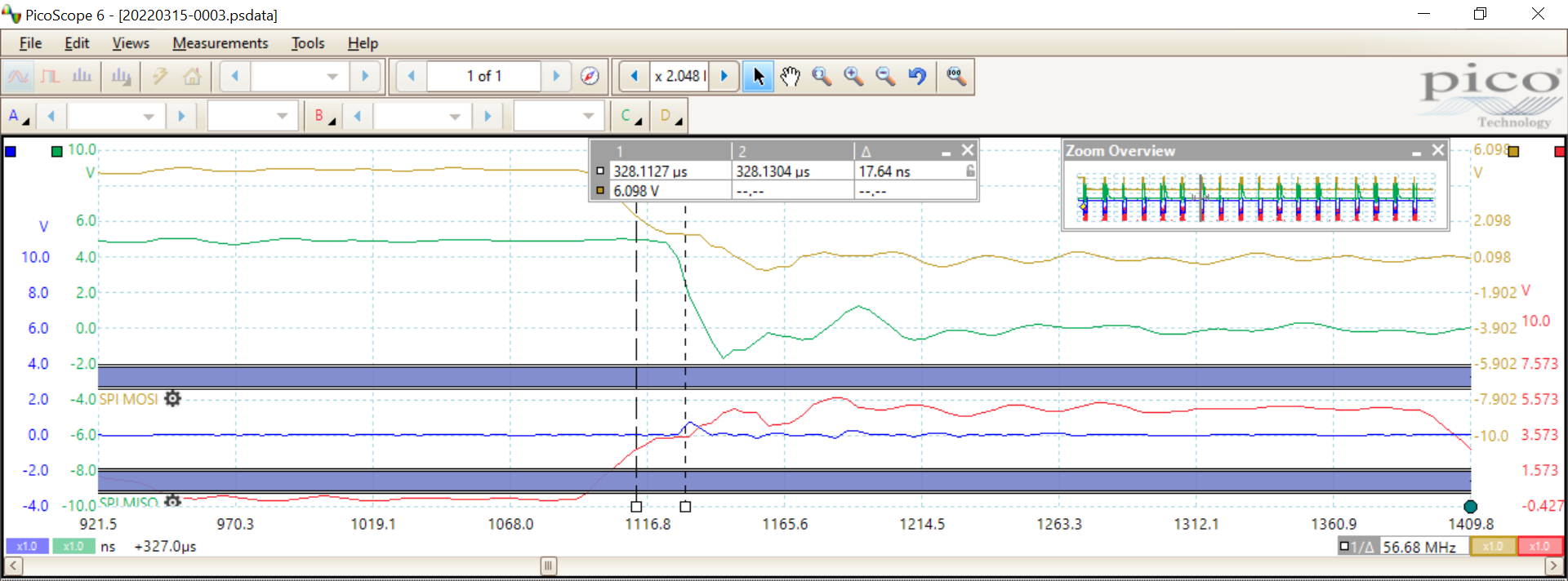
Description automatically generated

tH\_SDI Minimum, SDI input data hold time = 25 ns. The signal’s logic level is retained for more than 25 ns. OK

A screenshot of a computer

Description automatically generated

tSU\_SDI Minimum SDI input data setup time = 25 ns. The signal’s logic level is retained for more than 25 ns. OK



tD\_SDO Maximum SDO output data delay time = 30 ns. The measured value is 18 ns. OK

A screenshot of a computer

Description automatically generated

tH\_nSCS Minimum nSCS input hold time = 25 ns. The measured value is 1100 ns. OK

A screenshot of a computer

Description automatically generated

tSU\_nSCS Minimum nSCS input setup time = 25 ns. The measured value is 1300 ns. OK

A screenshot of a computer

Description automatically generated

tHI\_nSCS Minimum nSCS high time = 450 ns. The measured nSCS high time is more than 450 ns. OK

Graphical user interface, application

Description automatically generated

tEN\_nSCS Maximum enable delay time = 50 ns. The measured value is 15 ns. OK

Graphical user interface, text, application

Description automatically generated

tDIS\_nSCS Maximum enable delay time = 50 ns. SDO remains active for more than 50 ns. TBD if this is an issue

A screenshot of a computer

Description automatically generated

tDIS\_nSCS The measured disable delay is 2000 ns. TBD if this is an issue