7.3.2 Bridge Control

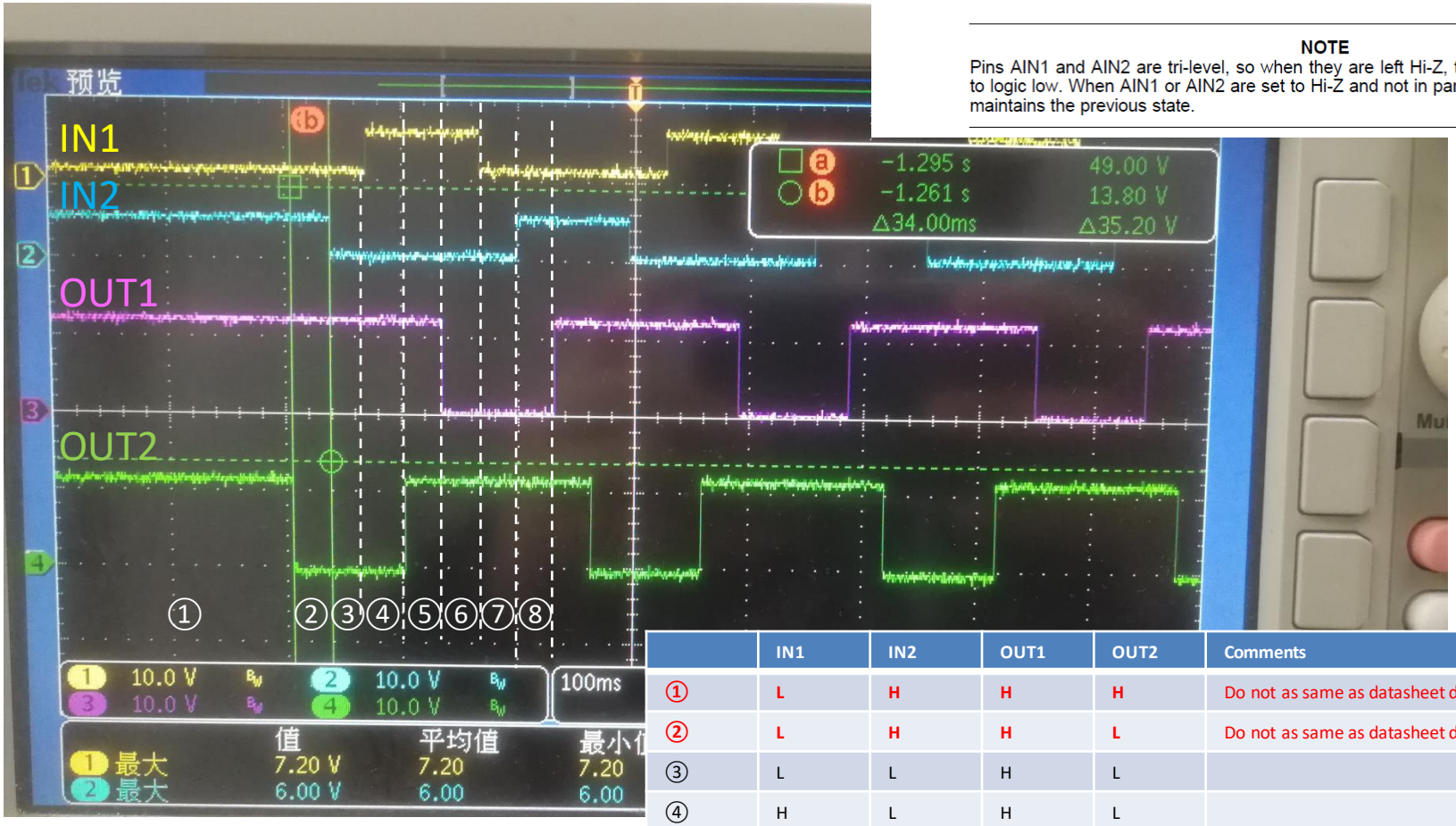
Table 1 shows the logic for the inputs xIN1 and xIN2.

Table 1. Bridge Control

xIN1	xIN2	xOUT1	xOUT2	Function (DC Motor)
0	0	Z	Z	Coast (fast decay)
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake (slow decay)

NOTE

Pins AIN1 and AIN2 are tri-level, so when they are left Hi-Z, they are not internally pulled to logic low. When AIN1 or AIN2 are set to Hi-Z and not in parallel mode, the output driver maintains the previous state.



	IN1	IN2	OUT1	OUT2	Comments
①	L	H	H	H	Do not as same as datasheet description
②	L	H	H	L	Do not as same as datasheet description
③	L	L	H	L	
④	H	L	H	L	
⑤	H	L	H	H	Do not as same as datasheet description
⑥	H	L	L	H	Do not as same as datasheet description
⑦	L	L	L	H	
⑧	L	H	L	H	