Table 8-3. Half-Bridge SPI Register Control (HBx_CTRL)

HBx_CTRL (1-8)	Gate Driver State	GHx (1-8)	GLx (1-8)	SHx (1-8)
00b	High Impedance (Hi-Z)	L	L	Hi-Z
01b	Drive Low-Side (L)	L	H	L
10b	Drive High-Side (H)	H	L	H
11b	Drive PWM (PWM)	Table 8-5	Table 8-5	Table 8-5

At NSLEEP = LOW

GHx / GLx are 0V and both DS terminals of the FET are OPEN.

DS bot ends are Open.

0V
GHx to GND

At NSLEEP = HIGH, HBx_CTRL = 00b

GLx is normal at 0V, GHx is required to be 12V (GHx to GND), and the two DS terminals of the FET are required to be 0.8kΩ.

DS bot ends are about 0.8kΩ.

In conclusion, 12V is applied to the SHx terminal.

12V
GHx to GND