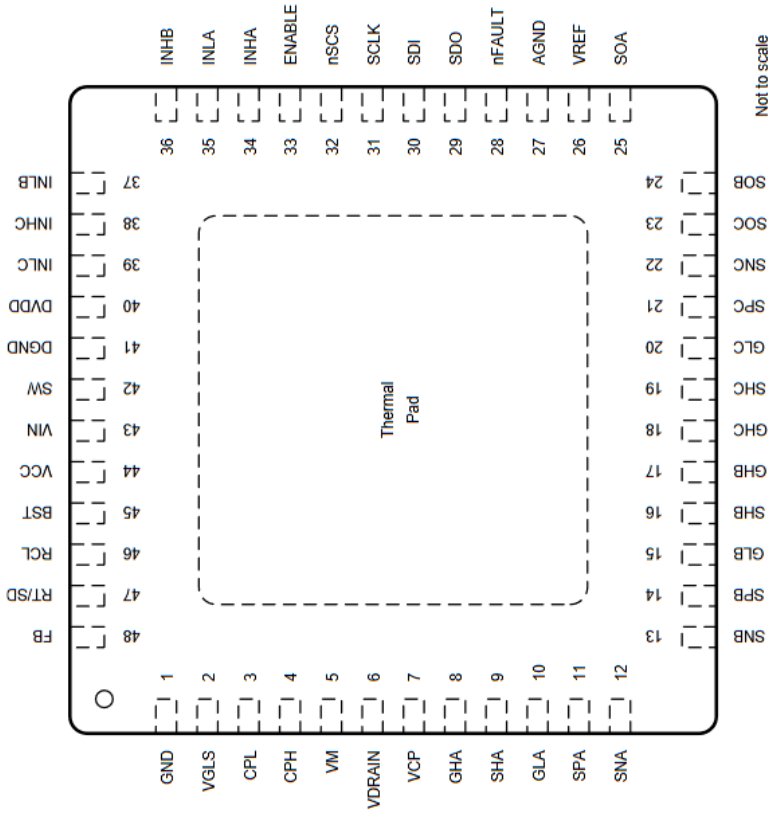
Device info

Table 21. DRV835x Gate-Driver External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	X5R or X7R, 0.1-µF, VM-rated capacitor
C_{VM2}	VM	GND	≥ 10 µF, VM-rated capacitor
C_{VCP}	VCP	VM	X5R or X7R, 1-µF, 16-V capacitor
C_{VGLS}	VGLS	GND	X5R or X7R, 1-µF, 16-V capacitor
C_{SW}	CPH	CPL	X5R or X7R, 47-nF, VDRAIN-rated capacitor
C_{DVDD}	DVDD	DGND	X5R or X7R, 1-µF, 6.3-V capacitor
R_{nFAULT}	VCC(1)	nFAULT	Pullup resistor
R_{SDO}	VCC(1)	SDO	Pullup resistor
R_{IDRIVE}	IDRIVE	GND or DVDD	DRV835x hardware interface
R_{VDS}	VDS	GND or DVDD	DRV835x hardware interface
R_{MODE}	MODE	GND or DVDD	DRV835x hardware interface
R_{GAIN}	GAIN	GND or DVDD	DRV835x hardware interface
C_{VREF}	VREF	GND or DGND	Optional capacitor rated for VREF
R_{ASENSE}	SPA	SNA and GND	Sense shunt resistor
R_{BSENSE}	SPB	SNB and GND	Sense shunt resistor
R_{CSENSE}	SPC	SNC and GND	Sense shunt resistor

(1) VCC is not a pin on the DRV835x family of devices, but a VCC supply voltage pullup is required for the open-drain output nFAULT and SDO. These pins can also be pulled up to DVDD.



General Info (Copied and pasted):

Highest priority to lowest priority routing:

Voltage Rails

- VM, VCP, CPH, CPL, VGLS. Analog rails requiring output or decoupling caps
    - C_SW, C_VCP, C_DVDD, C_VGLS,
        - Low ESR, close to pins as possible
    - C_VM1 closest, C_VM2 next, then to via (if applicable)
        - Place capacitors as close to the VM pin as possible with a thick trace or ground plane connected to the GND pin

Important signal path signals

- GND, the reference voltage for the DRVx, as well as the FETs
    - All ground should be tied together at some point
    - Don't use thermal Relief connects, do it directly
    - Trace path from negative return path,
- GHx and SHx, GLx and SPx or SLx, SPx and SNx, which are used for functional, protection, and sensing signals should treated "like" differential pairs where lengths, widths, and loop shape should be similar or the same size for the pairs (not necessarily every A, B, C half bridge needs the same specs).
    - Only the SPx and SNx are recommended to be held to actual differential routing rules, the rest should be "treated as" but not "strictly treated as" differential
        - This means, the GLx and SPx pairs should be given lower priority compared to SPx and SNx traces
    - Do not connect the SLx pins (and SNx) directly to GND. Instead, use dedicated traces to connect these pins to the sources of the low-side external MOSFETs. If using less than 3 shunt, use a common point of GND and then branch to 3 separate traces to each low side FET (like VDRAIN)
    - If a set of half bridge signals are longer than the other, try to use wider traces to counter-act the higher parasitic inductance introduce in the path
    - Do not overlap any of these traces with each other or other high current paths as crosstalk should be prevented
    - Traces >10mil thickness but preferred the size of the pin at least
    - Try to avoid vias in path if possible
    - Try to make short as possible, more length means more inductance
- VDRAIN, SLx. For protection or sensing
    - For VDRAIN, Use a dedicated trace to connect to the common point of the drains of the high-side external MOSFETs. This means, VDRAIN will eventually consolidate into one trace. The 3 traces should come from the HS drains of the FETs and be of similar lengths before hitting the common point that consolidates the traces together.

Digital signals

- INLx, INHx, SDI, SDO, SCLK. Digital Signals that switch frequently
    - At this point, we're dealing with digital signals and they matter a lot less. Assuming the switching frequency isn't nearing close to MHz (if so, then follow high speed guidelines)
    - Give priority to other signals but make sure these are crossing over any of the signals above or to each other so there's no cross-talk. SPx, SNx, SLx, and VDRAIN are specifically prone to cross talk
    - Vias or longer routing is definitely an option, weigh all other layout criteria before these and below
- nFAULT, nSCS, . Digital signals that switch sometimes
    - Throw these signals through vias, other layers, make them long
    - Put the pull far away from the device, these signals just don't matter compared to the others
- MODE, IDRIVE, VDS. Digital signals that never switch
    - These only really "switch" during power up phase. Make sure their criteria is met during power up requirements. Besides that, give all other signals higher priority
        - But in general, parasitics shouldn't be enough unless grounding is really bad
    - Throw these signals through vias, other layers, make them long
    - Put the pull far away from the device, these signals just don't matter compared to the others

Other info from motor drive layout app note I linked to you previously https://www.ti.com/lit/an/slva959a/slva959a.pdf :

- Your traces don't look like 20 mils on your gate driver and FET paths

  Follow these general routing techniques when doing a motor driver PCB design:

  - Make gate drive traces wide and as short in length as possible. Start with a trace width of 20 mils for at least a 1 oz copper, more if required by high currents.

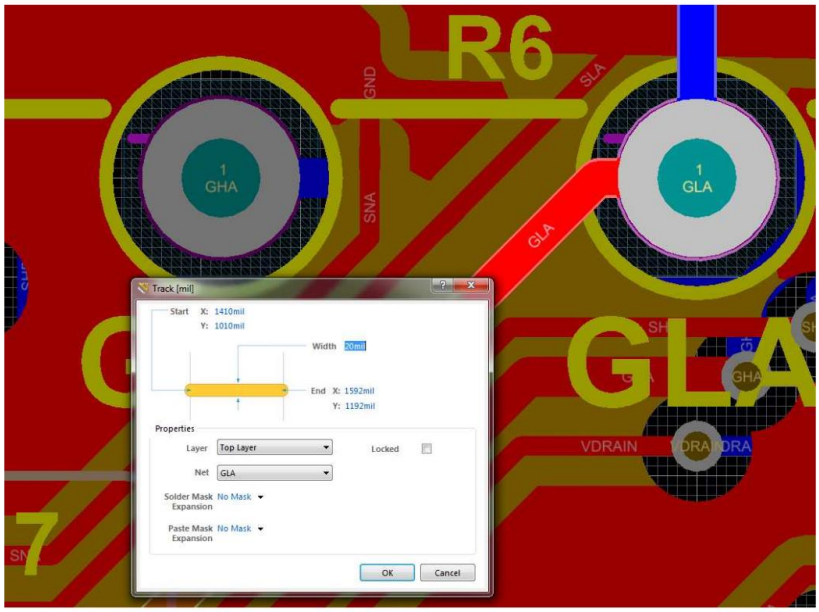


Figure 16. DRV8323xEVM Gate Signal

- See some points you did do this

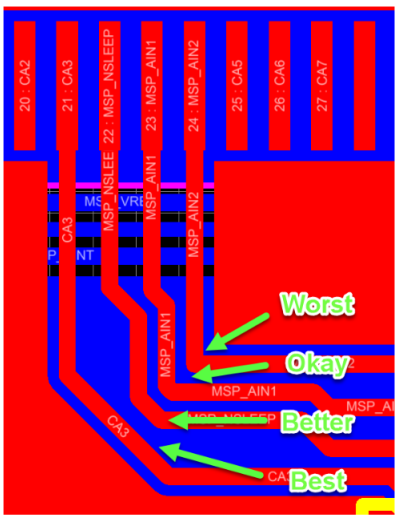


Figure 18. Right Angle Trace

High power design mitigation

Note, it only looks like you have localized decoupling, and your layout isn't ideal and will create parasitics. This section is to expose you to some other high power mitigation techniques.

Intro into our high power design philosophy:

First, it's inevitable that your high power design (48V, >500W) will have some sort of voltage or current spiking. There's parasitic inductance and capacitance all over the board. We can't avoid it, only suppress it or mitigate it.

This is the same exact mindset we share with EMI. Should I put a ferrite bead there; should I put a gate resistor there? Where are my GND loops on my signal chain decoupling caps, where are my GND loops on my gate drive current path? Should I use shielded components; should I use a higher voltage rating components? Hopefully this makes sense.

Simply put, the difference between 5A and 50A means magnetic fields are 10x stronger and the voltage generated by di/dt are 10x larger. It is even worse if the ringing lines up with some self-resonant frequency of all the Ls and Cs on the board.

Gate Current and Gate resistors

Simply put, introducing more current at the gate of the FET means the channel will open up more quickly and the equivalent voltage on the Gate and VDS will rise more quickly. Faster the slew rate on signals, the more high frequency content they contain which means they will ring at higher amplitude (as a result of higher di/dt). Flipping the logic, less gate current means less voltage spiking will occur. This is a tactic you've seen us use a lot of E2E to see if these kinds of problems can be mitigated.

In the case of the competitors, it's adding a gate resistor (3-15 ohms) and for smart gate drive technology, it's changing the source and sink current (IDRIVE), or both.

I agree that it makes a lot of stuff worse: thermals, EMI (in some cases), effective applied PWM duty cycle, etc. Without other options, most customers will have to make the tradeoff to get their existing system to work (as fixing the problems mentioned in the first section require board redesigns).

Blue wiring in some these other suggested components are just bandaids that prove that they will help in the long run as it is difficult to go to production with handwiring components to every product (especially when they add more parasitics which could make it worse).

Small mention to C_GD caps, they essentially make the equivalent Q_GD larger (caps in parallel add) so it takes more charge to turn on the FETs and get through the FETs.

RC Snubbers

This TI Design: https://www.ti.com/tool/TIDA-010056 has RC snubbers on the lowside and high side FETs. Specifically, R1 & C13, C16 & R14, R2 & C14, C17 &15, R3 & C15, and C18 & R16 are the RC snubbers. That's 12 components. The design guide also talks about the wattage rating of components (namely, 1/3*C*V^2*f_sw = P) and the blog below shows you how to calculate the components.

https://e2e.ti.com/blogs_/b/powerhouse/posts/calculate-an-r-c-snubber-in-seven-steps

The "too long, didn't read" summary for the blog shows that finding the optimal RC values require the board to be built, as they depend on parasitics of the board. Then the board is tested by swapping out the R and C and an equation is used to get the optimal value.

Also note, RC snubbers do a really good job suppressing after the initial spike, as the energy needs some time store into the capacitor. This means, its good for "settling time" but not the initial "overshoot".

Decoupling Capacitors, and Bulk caps

Other engineers have said quite a bit about this one, so you can find more info elsewhere.

Decoupling capacitors have the primary purpose to provide charge into a system so the main power supply doesn't have to. We know that small valued capacitors can be emptied and filled with charge relatively quickly, where larger valued capacitors can store a lot of energy, but not react as quickly. This is why you see 10uF in combination with 100nF capacitors placed on power supplies. Because the cap values can provide some charge quickly and a lot of charge over time, it helps with ringing and the initial spikes for the design. There's some more nuance as the smaller caps can be made out of different material and construction geometry to allow less parasitics in the path of charge, but I'll skip over the details.

Now, the caps are supposed to supply current (charge over time or C*V/t) which must travel through traces to the drain of the high side FETs, assuming the bulk capacitors are connected from the HS Drain to GND (bottom of sense resistors). This this case, we want the path between the caps and the HS Drain to be short and thick, and we want a lot of GND stitching vias to carry more current (as opposite charge needs to build up on the anode of the cap) near the GND connection of the cap.

You'll notice this is nebulous advice. I'm not giving equations or data. This is why engineers still talk about decoupling capacitors. Most notably, this is because it's much easier to put footprints, test system in reality, and if the performance isn't good enough, then we add in more caps, or change the existing cap values to higher values. Like the RC snubbers, this makes it experimental.

HS DRAIN to LS SOURCE caps

This has a very similar job to the decoupling because it provides charge to nodes or components that need the charge. One of the factors I forgot to mention in the previous section is that charge can only be provided from those caps if the reference is stable (e.g. GND is not bouncing) as the high impedance nature of the capacitors decreases as frequency increases, so current is rerouted through the cap, instead of to the component.

In the case where the node between the LS source and sense resistor is also needs charge, we know the sense resistor has some impedance, both intended and parasitic, in its connection to

GND. So, the bulk caps have to travel to through the sense resistor to provide charge to the node between the LS source an sense resistor. If GND is ringing and current is flowing through the sense resistor, charge has to fight against the flow.

The HS drain to low side source cap prevents this because it is connected to VDRAIN, which is assumed to be stable, and can dump charge directly onto the node, instead of through the path of a sense resistor. If you've ever heard the concept of an AC GND, this is the same idea. VDRAIN becomes our AC GND instead of just GND.

A lot of engineers underestimate the power of this fix. If GND or the sense resistor is ringing negative, or below GND, the HS Drain to LS source cap will provide charge in a low impedance and parasitic path. This is why waveforms are helpful for this. Keeping them around 1uF and as close to FET paths as possible, will help.

Diodes

I'm going to briefly acknowledge TVS diodes as I'm not an expert. Simply put, they'll clamp a node to a voltage so no absolute maximum ratings are violated for the device. Current rating, clamping voltage, max reverse voltage, and response time are all at play here.

A populate location is to connect the cathode to the GLx node, near the FET, and the anode to GND to help with negative transient spikes. From what I understand, these aren't recommended as a replacement to the other methods as the simply reroute energy as opposed to suppress by filtering or decoupling.

Layout techniques:

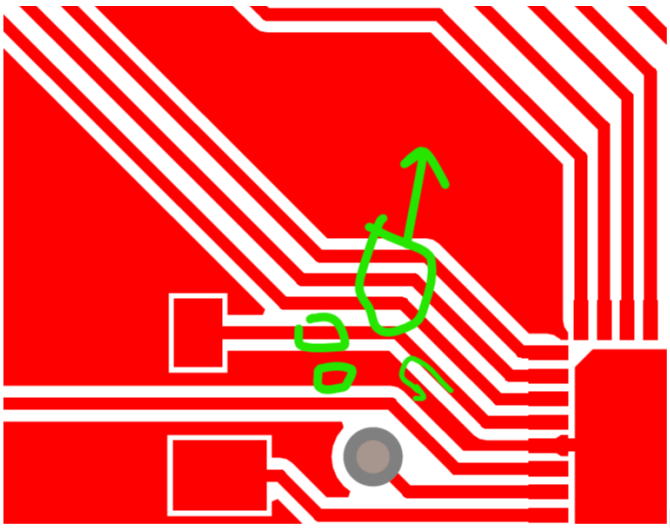
Components can only take you so far, but layout is equally important. Here's a bunch of quick wisdom.

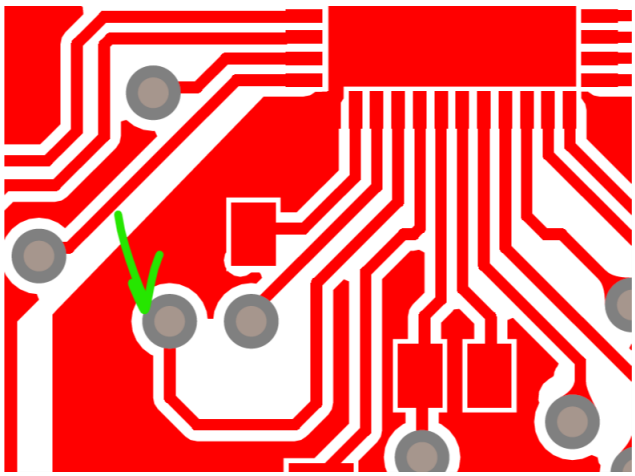
- The real PCBA has parasitic components that get added to the schematic, so to speak.
- Long traces add capacitance and resistance.
- Thin traces also add resistance and inductance.
- 10mil/Amp is a rule of thumb for the minimum trace width but it also applies to vias (angular ring area).
- Making traces thinner and smaller add impedance mismatch.
- More current means higher voltage spiking. Component footprints add parasitics.
- Vias in the path add parasitics.
- The return path must be understand: DC current will spread out on the GND planes as far it can reach where high frequency current gravitate underneath the trace. This is why common GND is always better unless current will flow near the trace
- Common ground is always better than split GND. Split GND is only ever used to divert large current or high frequency content away from sensitive components. That means the signal needs to be traveling towards those components to warrant a split GND.

- Be the current, draw the loop from the source of the pin or component to the GND pin or external connector. Make it as small as possible. This means adding lots of vias or rearranging components
- Order of importance or signals on an IC are voltage regulators (like VCP or VGLS), input regulators (like VM), signal path and higher current paths (like GHx and GLx), digital signals that switch often (like SPI), and digital signals that don't switch often (like nFAULT) which means

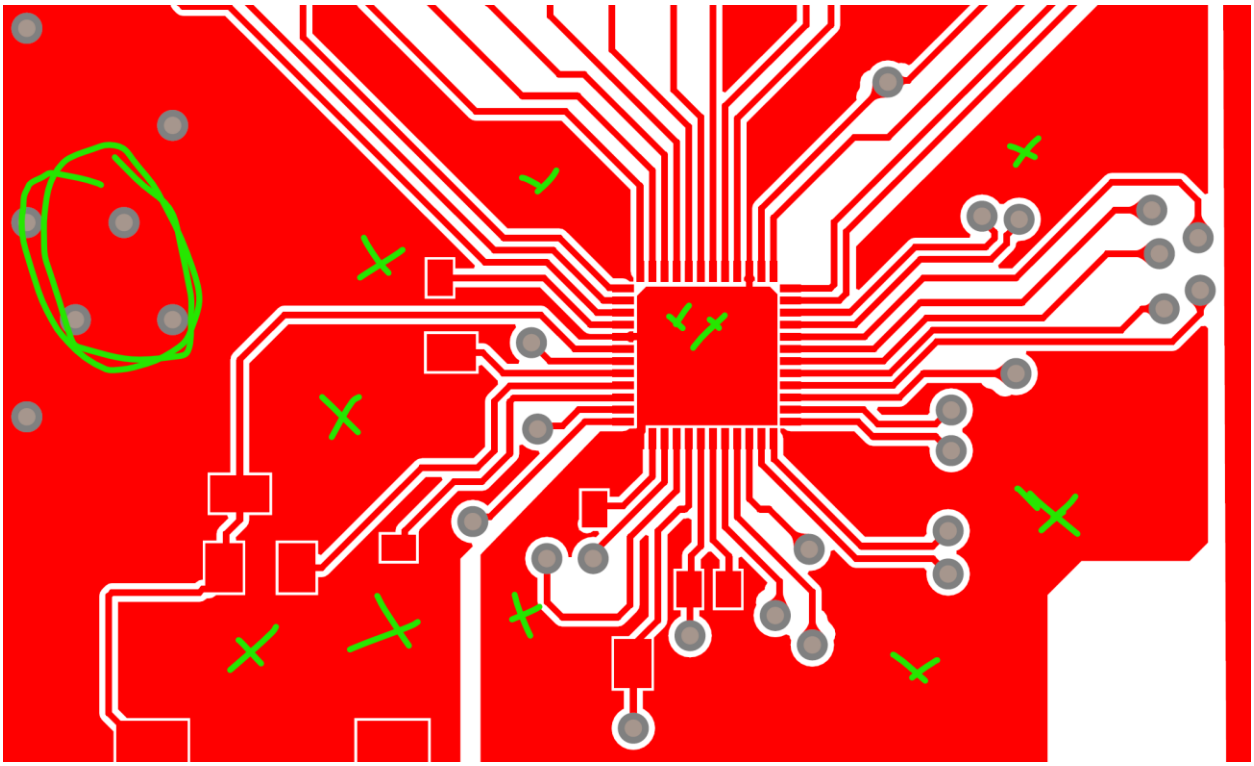
There's plenty more in this app note: https://www.ti.com/lit/an/slva959a/slva959a.pdf

Specific info:

-  In context of info above, it looks like INx signals were given priority to other signals
    - For example, DVDD, the decoupling caps, and the GND return path to the GND pin could have been make more optimal if INx thrown into vias or routed more directly to the connector
    - Recheck every cap to make sure its optimal and prioritized



- In context of above, CPL and CPH were not given priority and routed through vias



- I might have the wrong layers here but it looks like the circle is contained with vias which means there's no GND stitching vias close to the device (or even under the power pad).

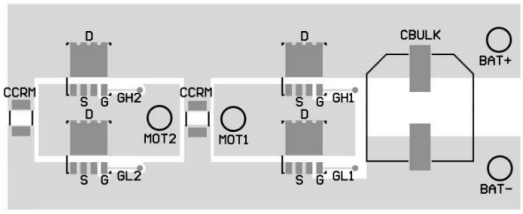
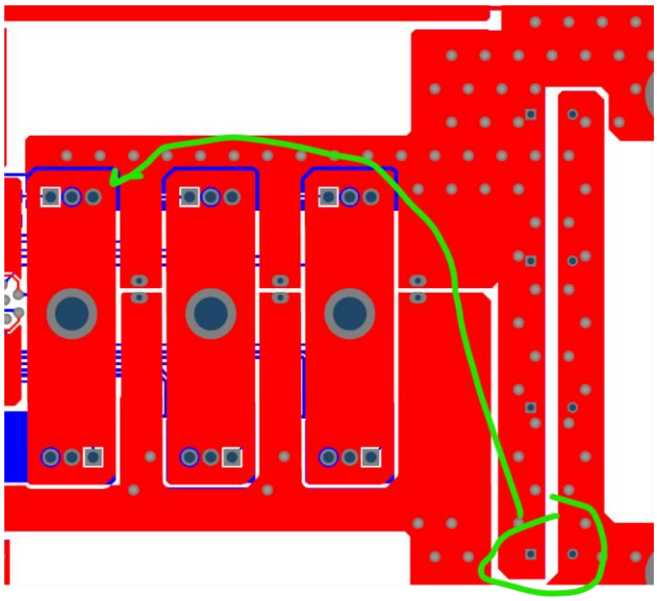


Figure 29. Bypass Capacitor Layout Example



- Look at difference between recommend bulk caps compared to yours

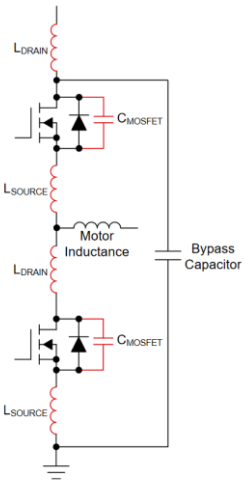
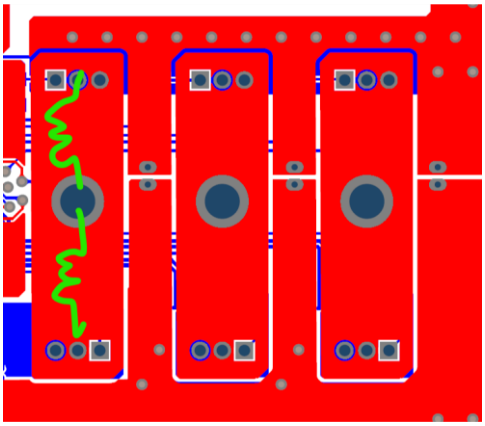


Figure 40. Half-Bridge Parasitics



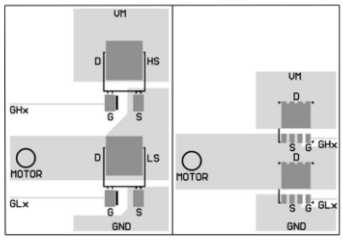


Figure 37. Half-Bridge Stack Configuration

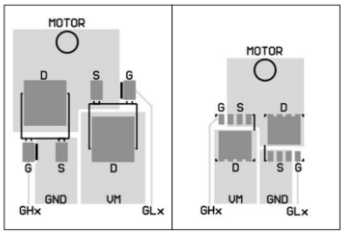


Figure 38. Half-Bridge Side-by-Side Configuration

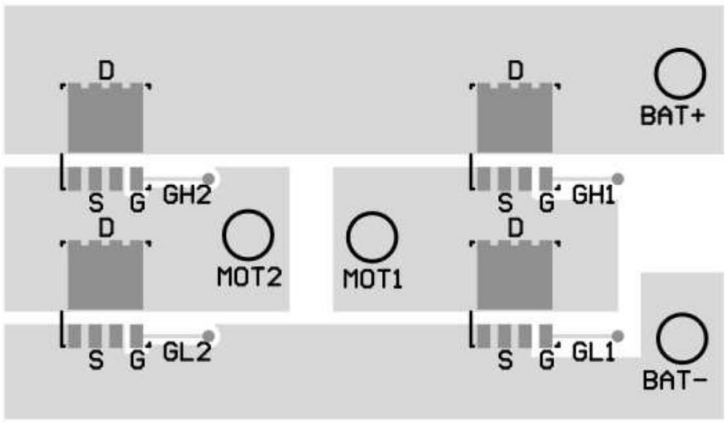
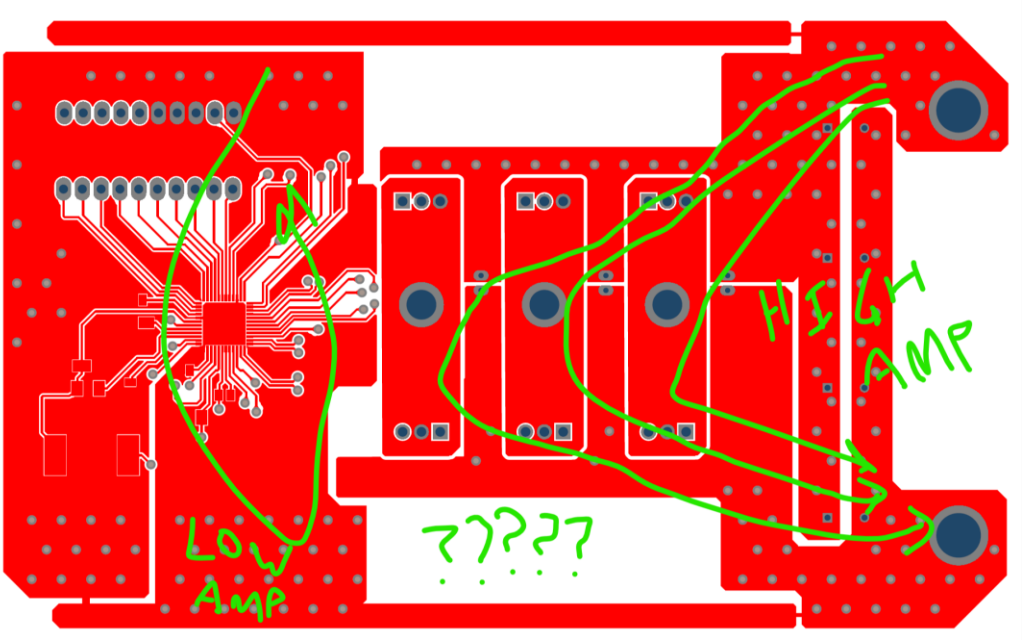
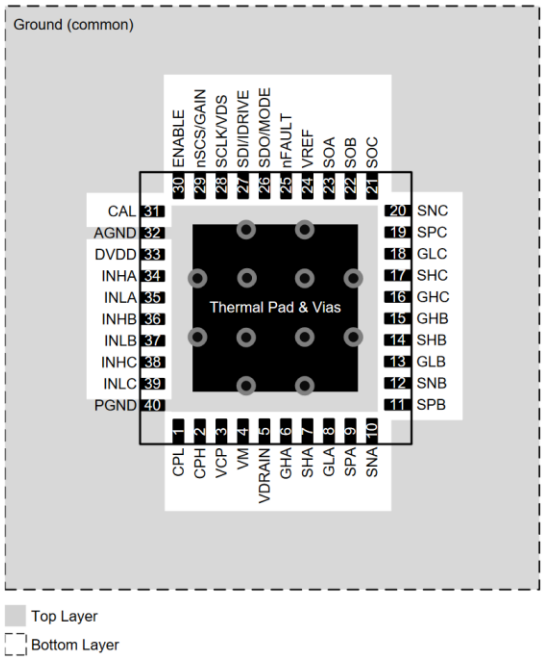


Figure 43. High-Current Loop Path Layout Example

- Doing this layout makes Lsource and Ldrain pretty large. See how recommended layout does not put the phase in the switching path?
    - The TI Design I liked does do this, but the FETs are much closer together. You might want to consider tightening up the FETs





- Common Ground is always the better layout technique. Split GND is only needed when high current is expected to flow near the DRV. If high current will never travel near, then the inductance created the objectively worse layout compared to the split GND provides no benefits.
    - Also, fill in GND in the empty spaces on both layers. There's no reason not to.

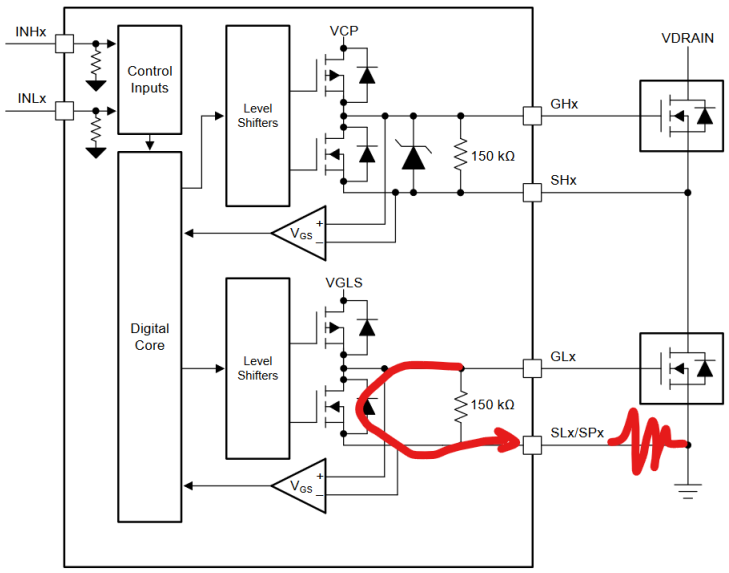


Figure 32. Gate Driver Block Diagram

- I think you have resistors in the sense path? Maybe? I don't have a schematic to tell. But if there are resistors in the SPx path you'll add inductance in the path so its not recommended to do filtering on the input of the CSA but do it on the output instead.