Motor driver layout best practices

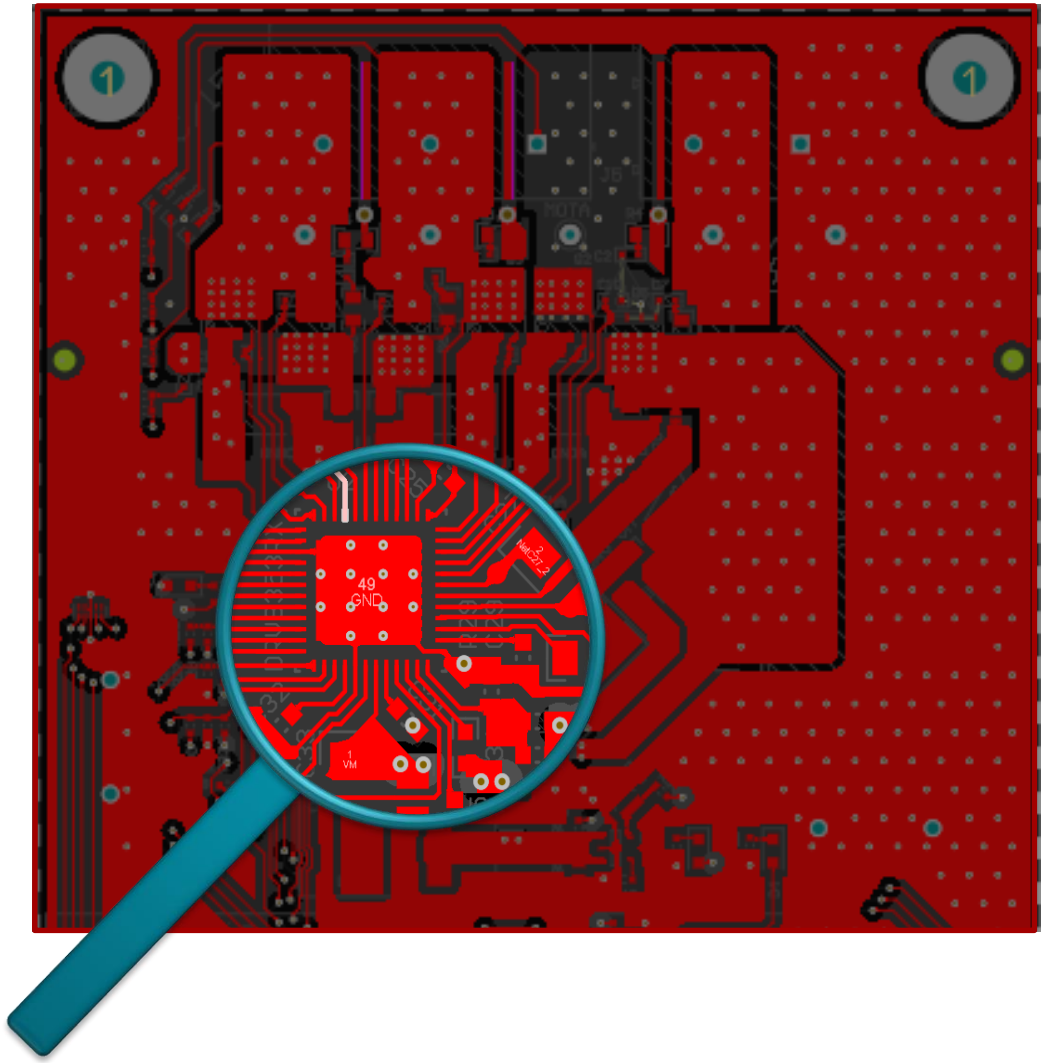
Anthony Lodi

Agenda

- Why is layout so important?
- Planning out a motor driver layout.
- Important layout considerations for BLDC motor driver layouts.
  - DRV related best practices.
  - Power stage related best practices.
  - Ground and power related best practices.
  - Analog and digital related best practices.
- Conclusion.

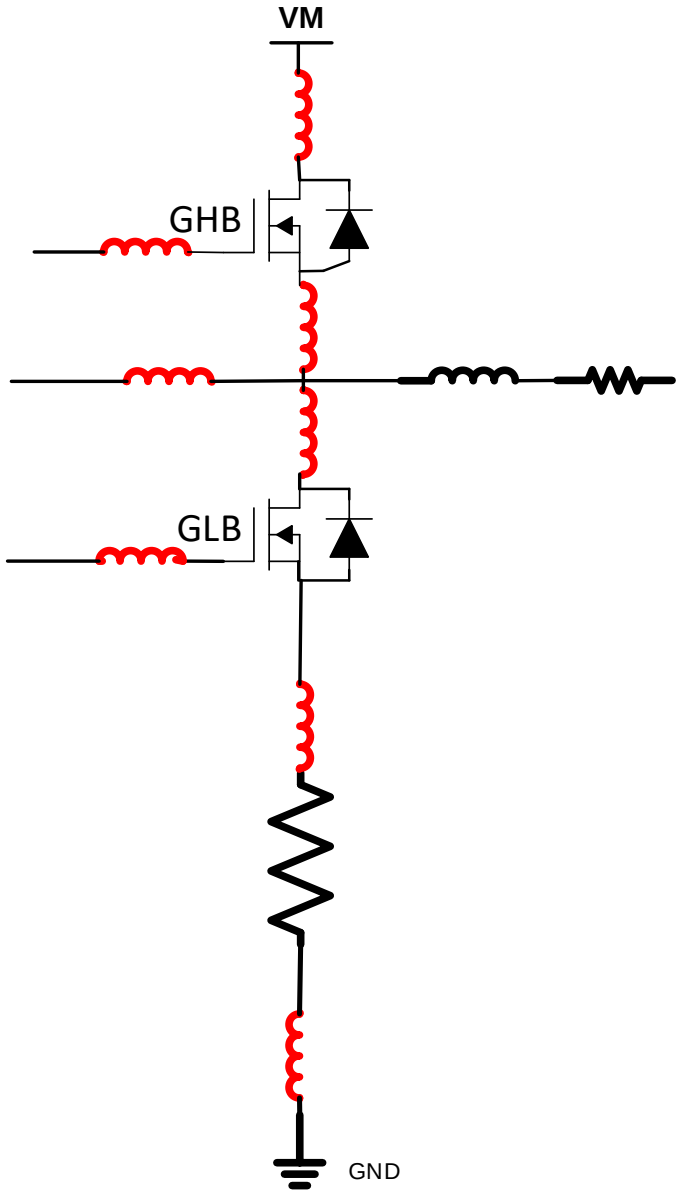
Why is layout so important?

- Layout is critical for proper device operation.
- Improper layout techniques can lead to poor thermal performance, poor motor commutation, and even device damage.
- For high power applications, the effects of board parasitics become even more magnified.
- Layout reviews help catch mistakes that could otherwise lead to board revisions or device failures down the road.



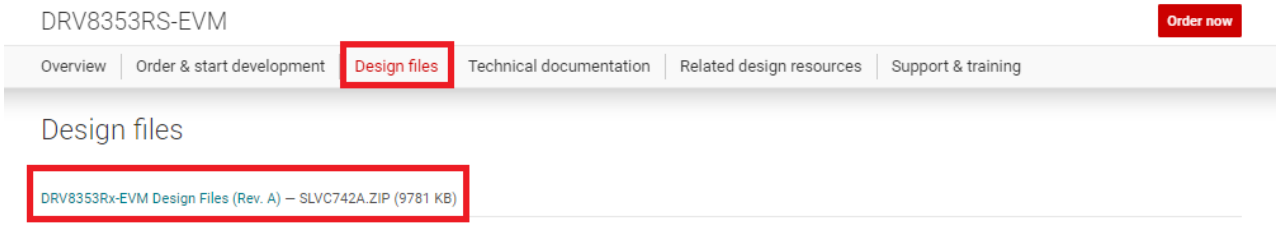
Importance of a layout review

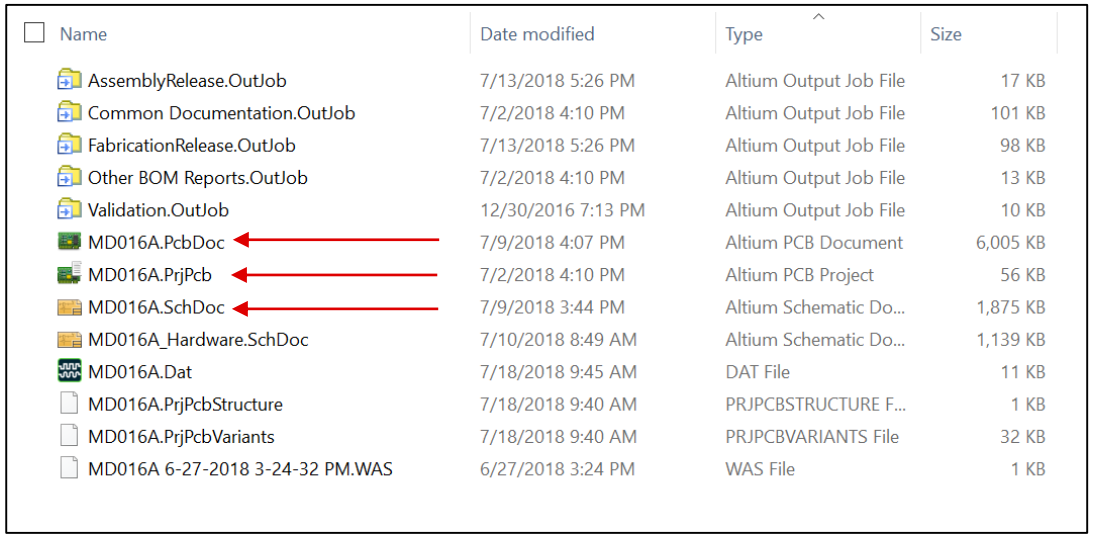
- Think the schematic hasn’t changed? Think again.
- Main concern is adding inductance.
- Other concerns are added capacitance and resistance.



EVM hardware files

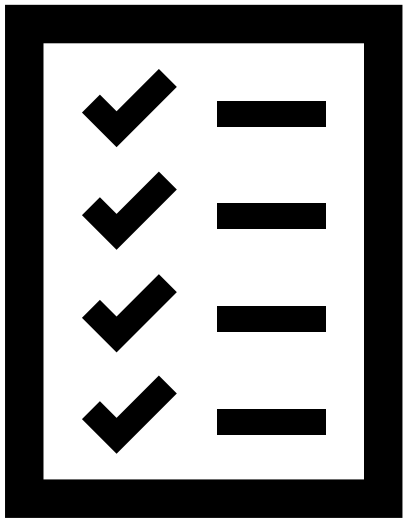
- Can be downloaded from the EVM product page under “Design Files”.
- Altium EVM layout file can be used as a reference for layout review.
- Note: many EVMs don’t have all the best practices implemented, so prioritize following the best practices mentioned in this Power Point.





Planning out a motor driver layout

- Determine board size needed, number of layers, and thickness of top/bottom layers.
- Isolate high-current circuits from low-current circuits.
- Grounding strategy for mixed-signal PCBs.
- High level component placement.

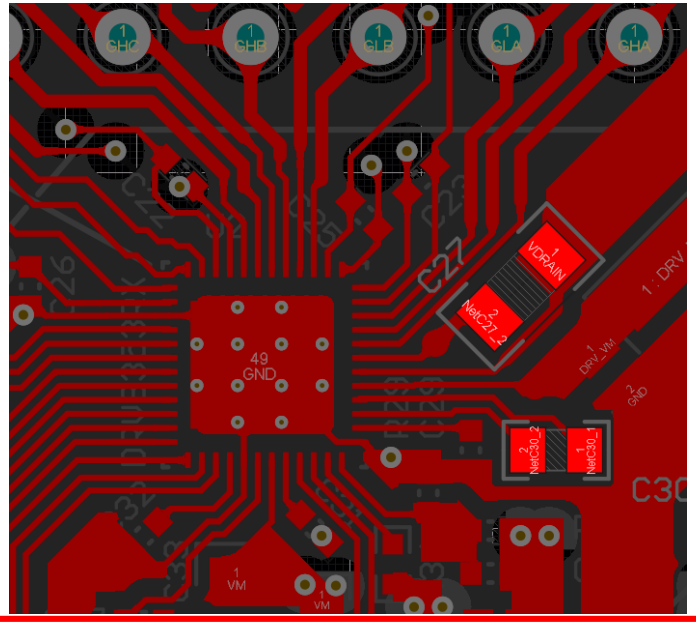


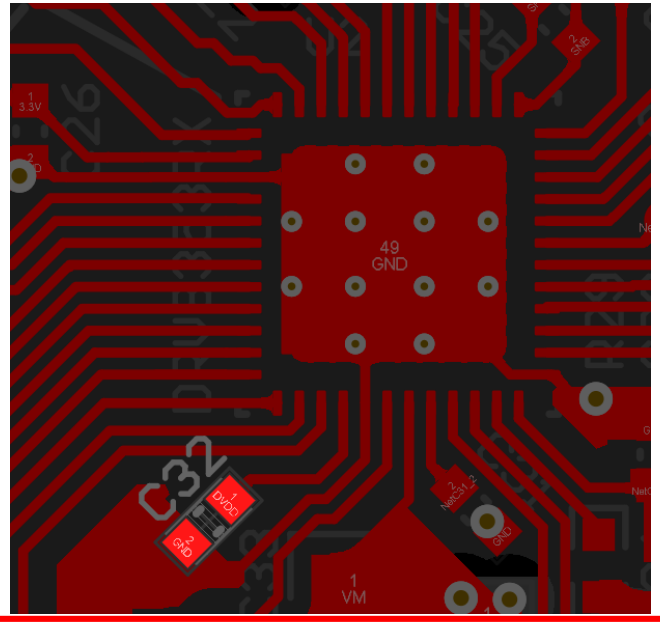
Important layout considerations for motor drivers

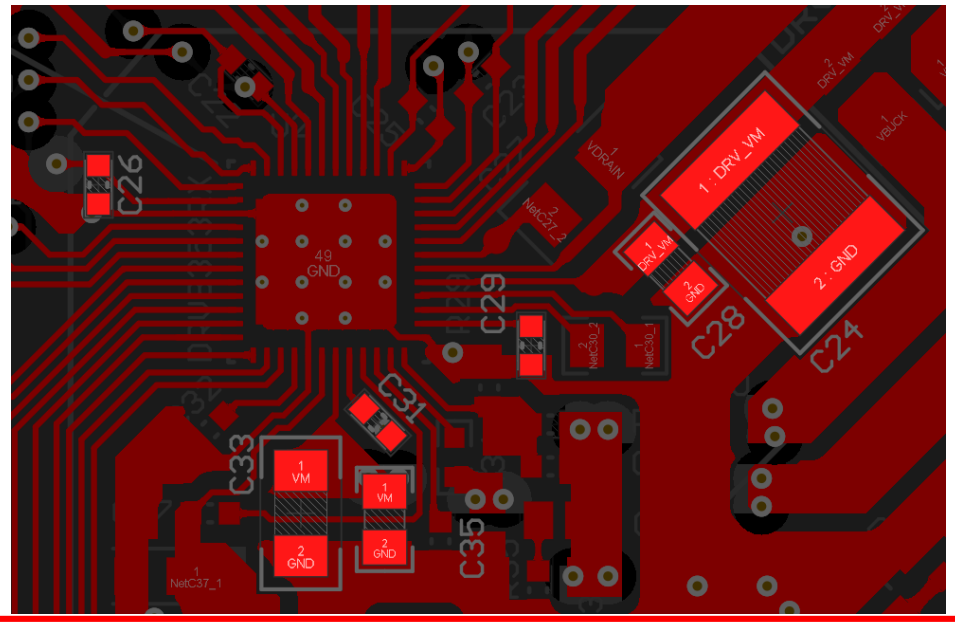
- ✓ **DRV-related**: place bypass and bulk capacitors as close as possible to the DRV device (VCP, CPH-CPL, bootstrap, GVDD, VM/PVDD, VGLS, DVDD, AVDD, PVDD, etc.).
- ✓ **Gate drive-related**: gate drive outputs routed as short and wide as possible, with a recommended width of at least 15-20mil to mitigate parasitic effects.
- ✓ **Power stage-related:** motor current paths routed using copper pours, repeated layers, and thermal/stitching vias to minimize parasitics.
- ✓ **Supply/GND related:** proper placement and layout of supply paths, bulk capacitances, and sufficient grounding strategies to provide current return paths.
- ✓ **Analog related:** fast switching signals routed differentially with filtering components placed near input pins of IC.
- ✓ **Digital related:** fast switching signals routed differentially with higher priority over slow switching signals.

DRV motor driver – capacitors

- Minimize current loops. Components further away = ***higher loop inductance.***
- 1st Priority: charge pump caps (VCP-VM and CPH-CPL caps) and/or bootstrap. caps closest to device.
- 2nd Priority: DVDD cap(For EMI considerations), GVDD cap.
- 3rd Priority: VM/PVDD, VGLS, GVDD, AVDD, VREF bypass and bulk caps.

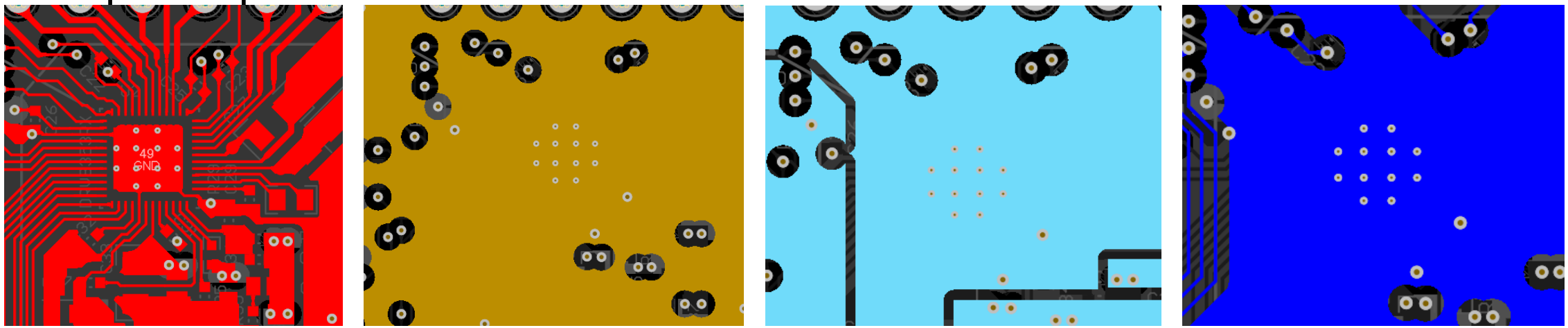






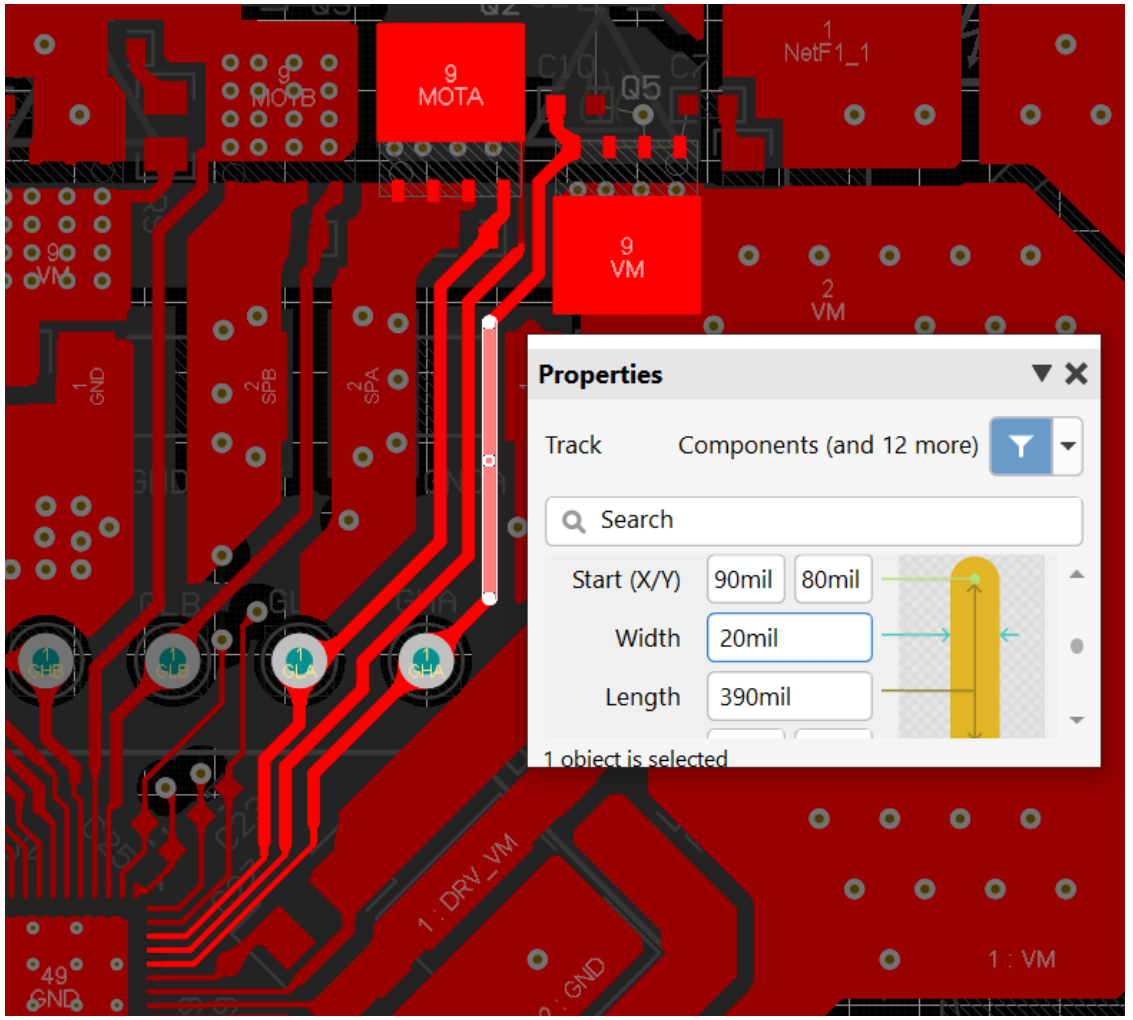
DRV motor driver – thermal pad

- Thermal pad is the primary source for device heat dissipation.
- Especially critical for integrated FET drivers.
- Use vias in thermal pad to connect to GND of inner and bottom layers.
- Wide GND copper pours help dissipate the heat from the driver.
- Keep in mind traces and vias can cut up ground planes and reduce thermal dissipation paths.

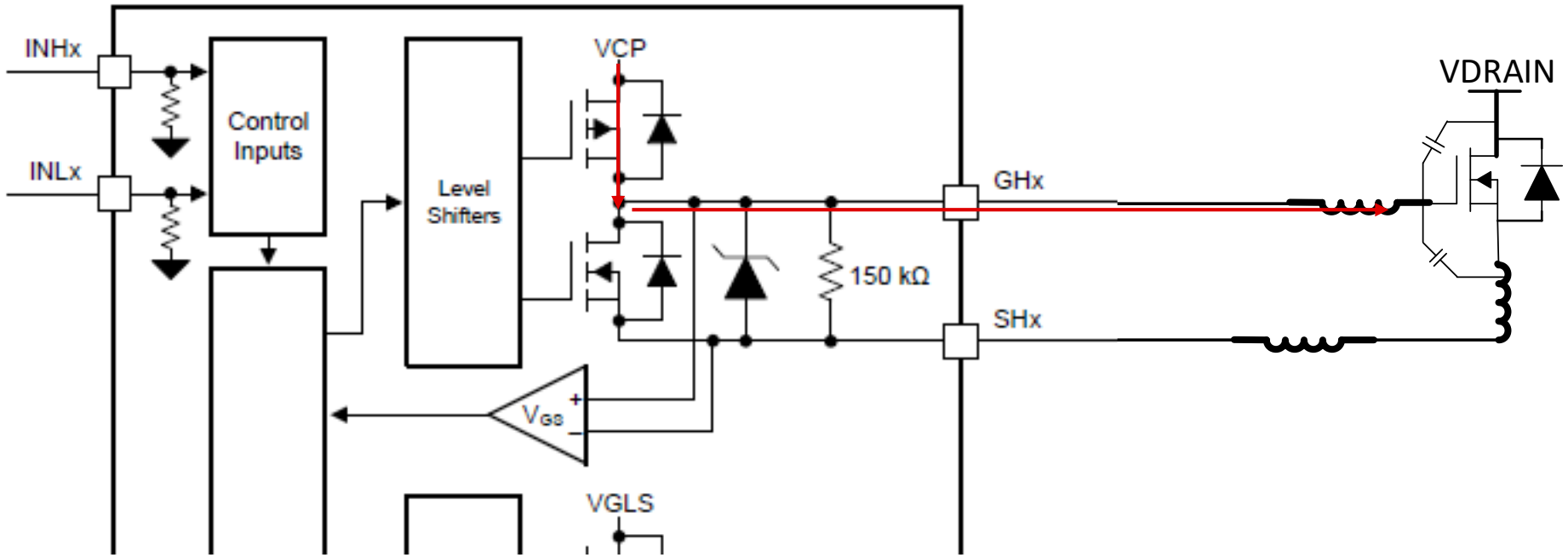


Gate drive outputs

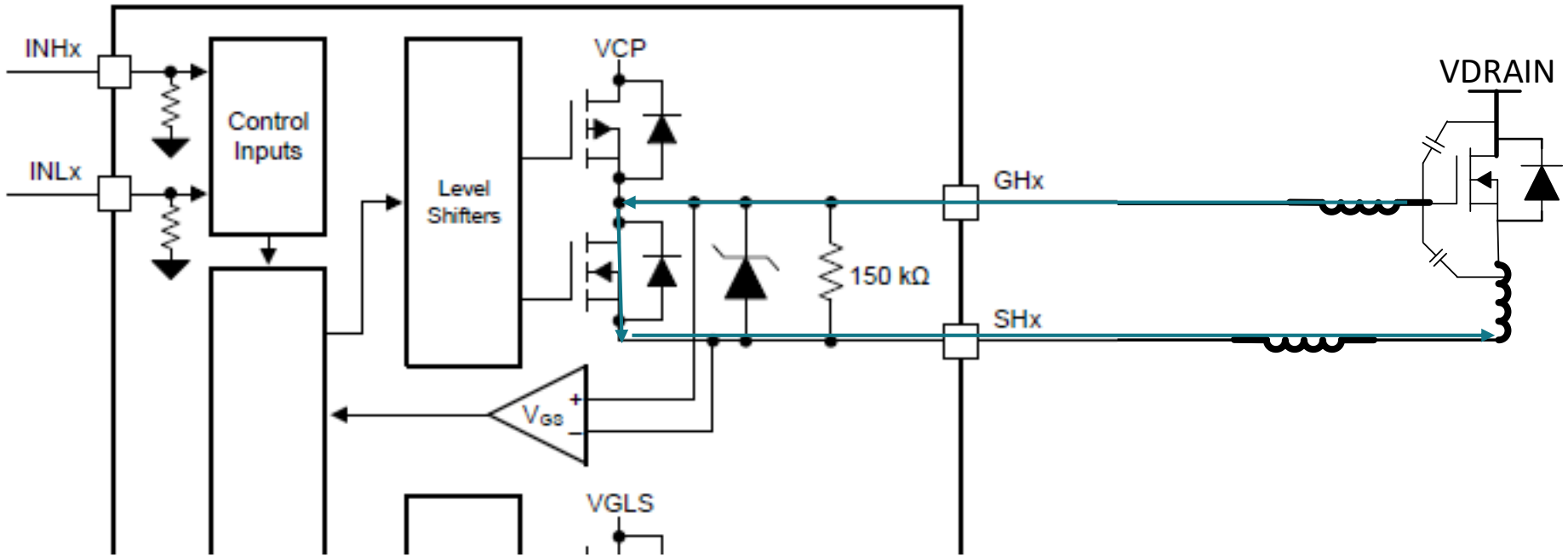
- Minimum of 15-20mil width on all GHx/GLx/SHx traces.
- Minimize trace length and have similar phase to phase implementation.
- Try to limit vias in GHx/GLx/SHx trace paths to 2 maximum.
  - Vias increase inductance.
- Try to shield gate traces from high current switching paths.
  - Ground layers can help shielding.



Gate drive outputs



Gate drive outputs

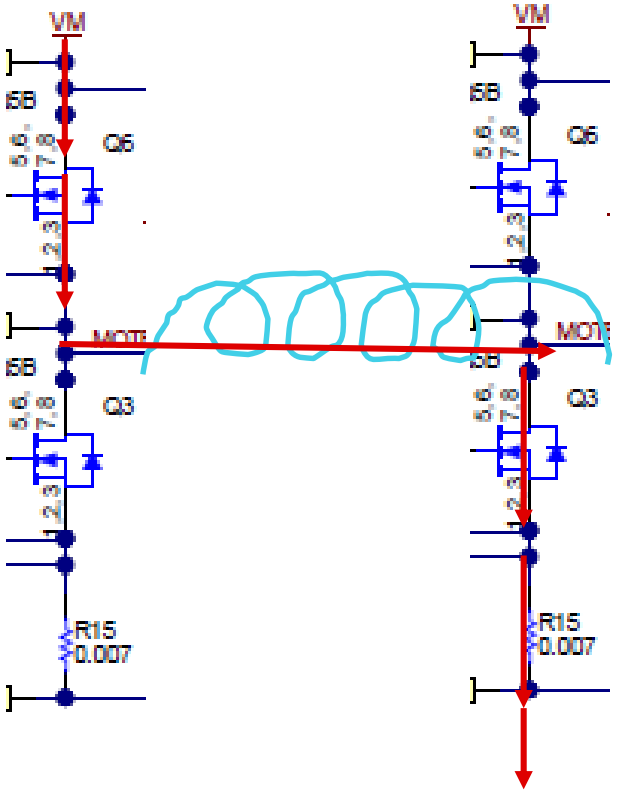


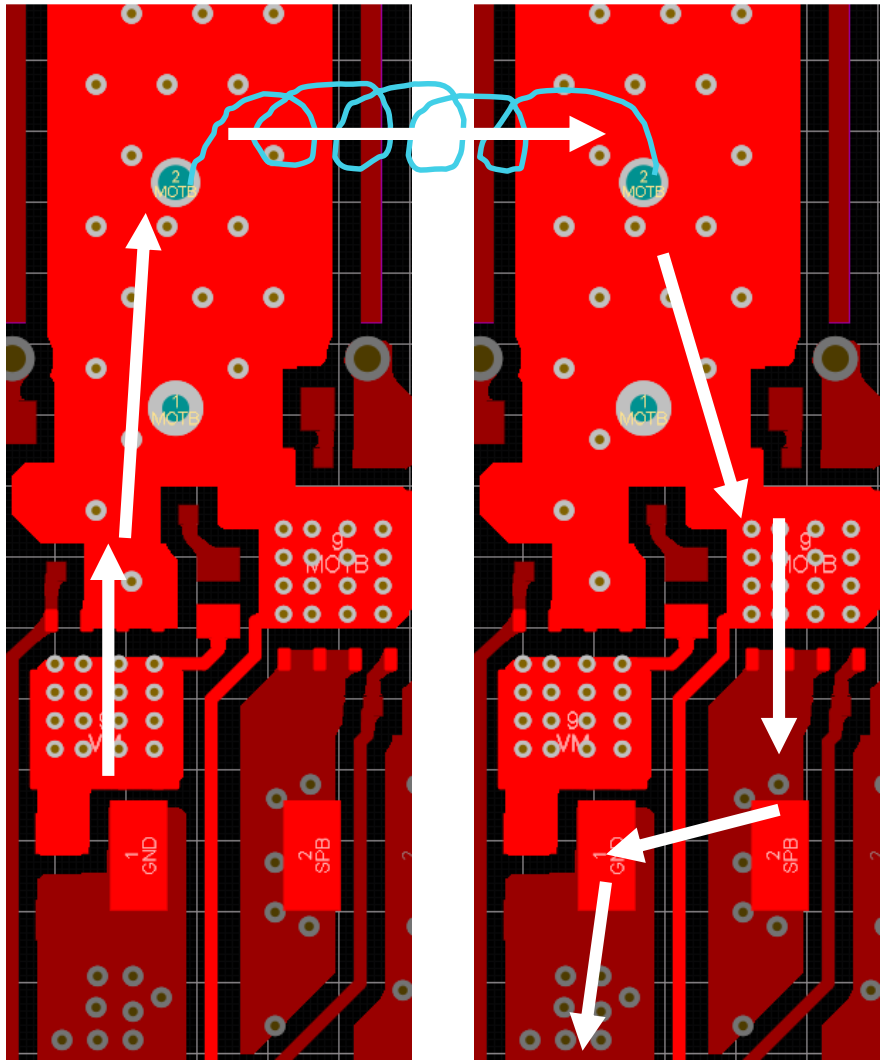
Power stage – motor current paths

- Keep FETs on same layer and place as close as possible to each other.
- Use large copper pours for motor current paths.

Supply → HS MOSFET
→ Switch node
→ LS MOSFET
→ Shunt resistor → Ground

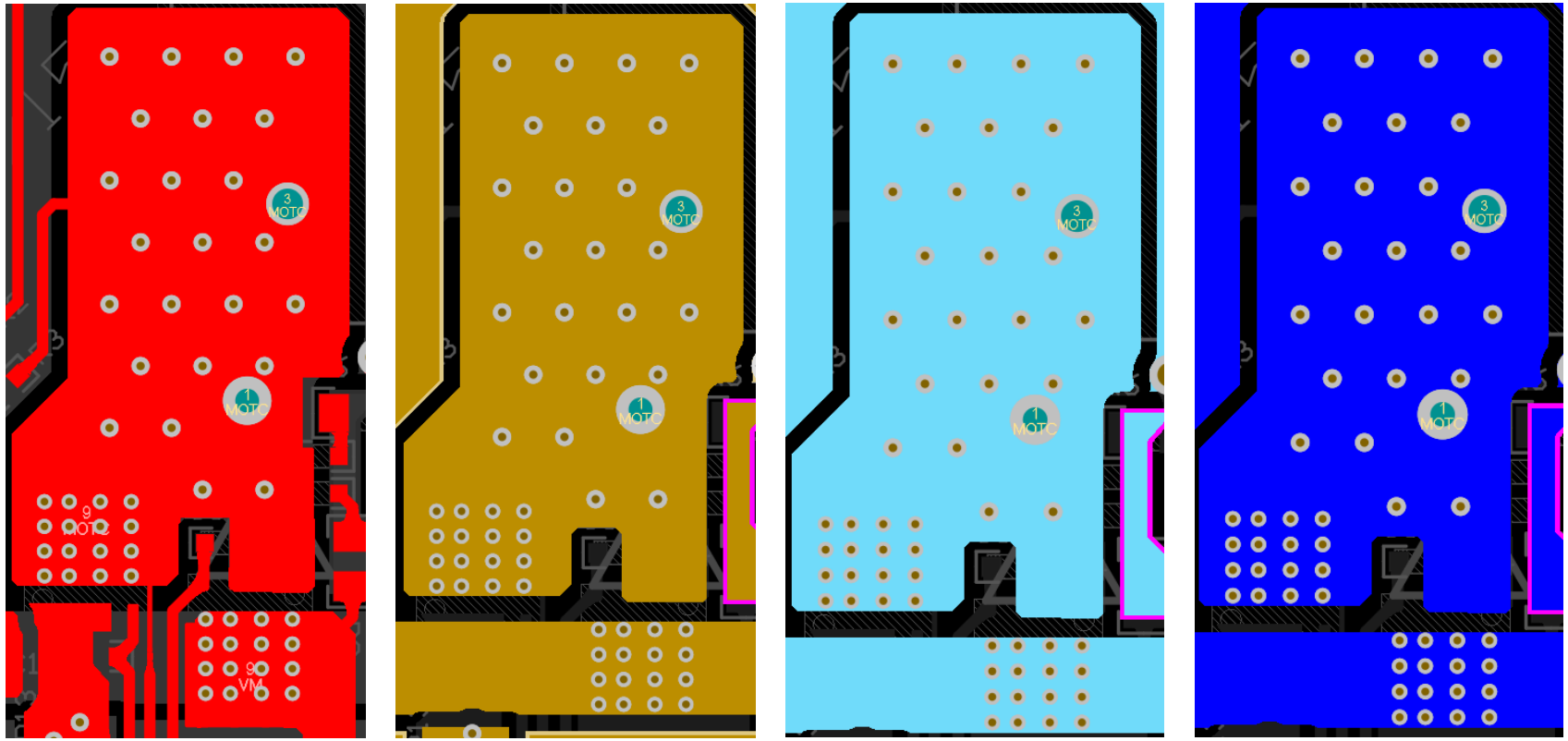
- Good via stitching for high current paths through multiple layers.





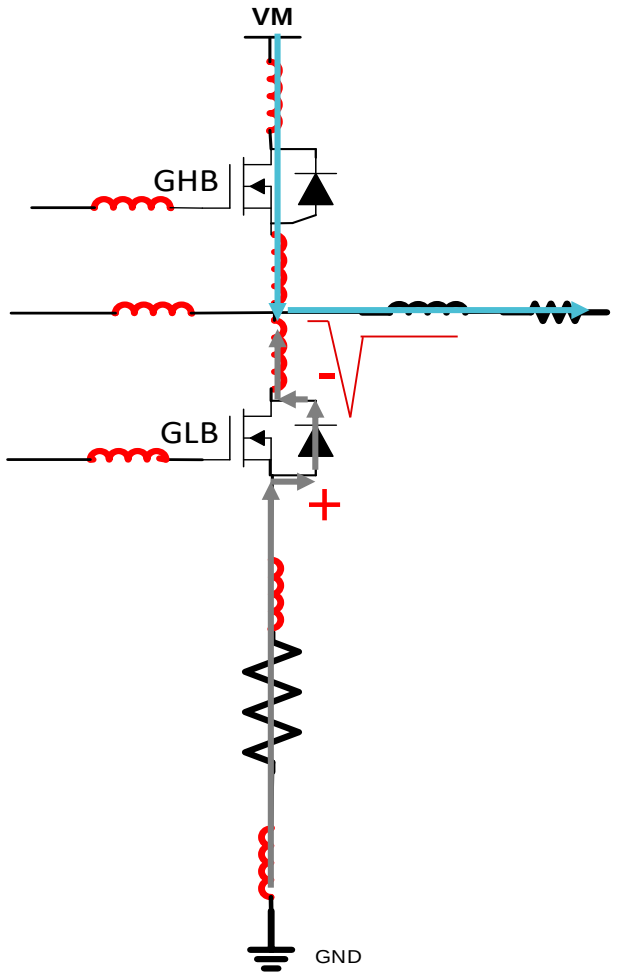
Power stage – placement & tips

- Phase node stitched together on multiple layers for better thermal dissipation and current flow.



Power stage – motor current paths

- Negative transients on SHx.
- Caused especially by reverse recovery of low side body diode.
- Ensure low inductance path on phase node and to ground.



Power stage – placement & tips

Placement

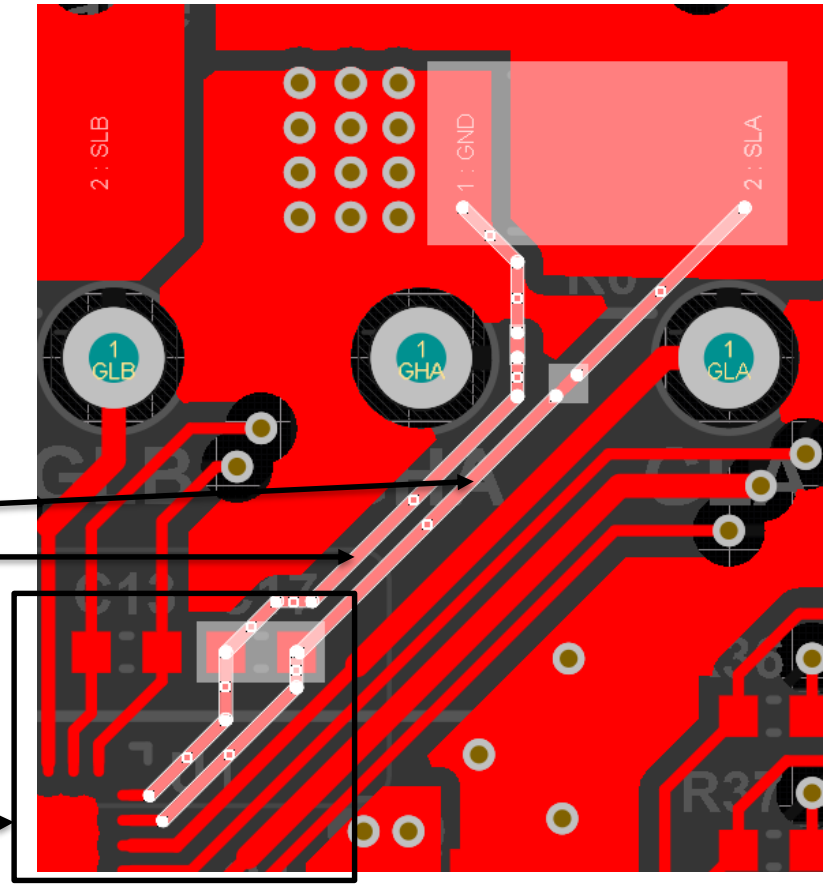
- Place gate resistors, if used, near gates of FET(s).
- Place VDRAIN bypass capacitors near HS drains of FET(s).
- Place VDRAIN-LSS caps near LS source of FET(s).
- Place RC snubbers parallel and close to the FET(s).

Layout

- Use polygon pours to mitigate parasitic inductance/resistance.
- Use repeated layers for high current paths and thermal dissipation.
- Use via stitching on high current paths.
- No right angles.

Power stage – shunt resistors & CSA inputs

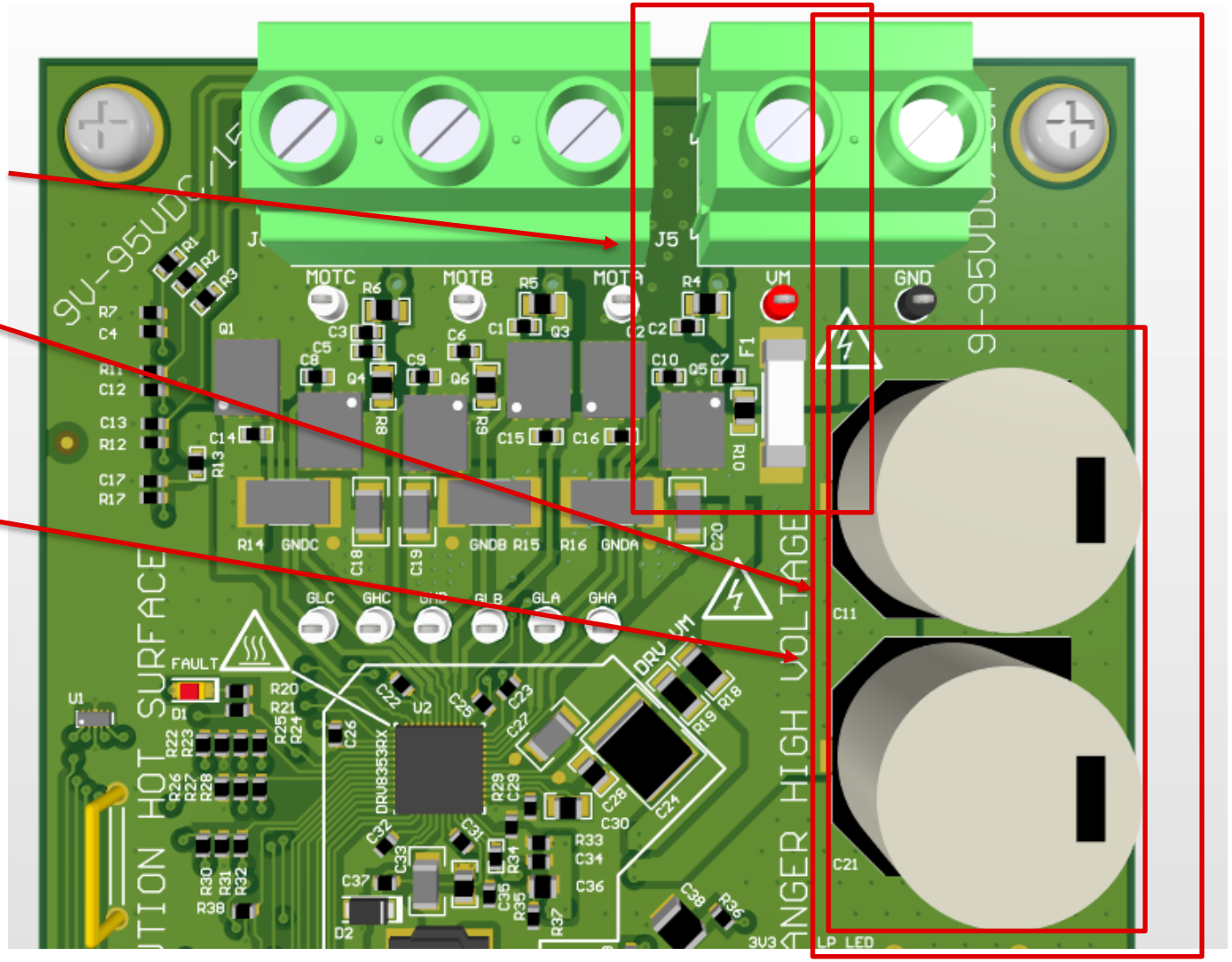
- Current sense amplifiers (CSAs) require accurate differential voltage measurements from the shunt resistor.
- Route SPx/SNx connections from the shunt resistor, use differential routing back to CSA inputs.
- Place input capacitor filtering near SPx/SNx pins if used.



Taken from DRV8323RxEVM layout

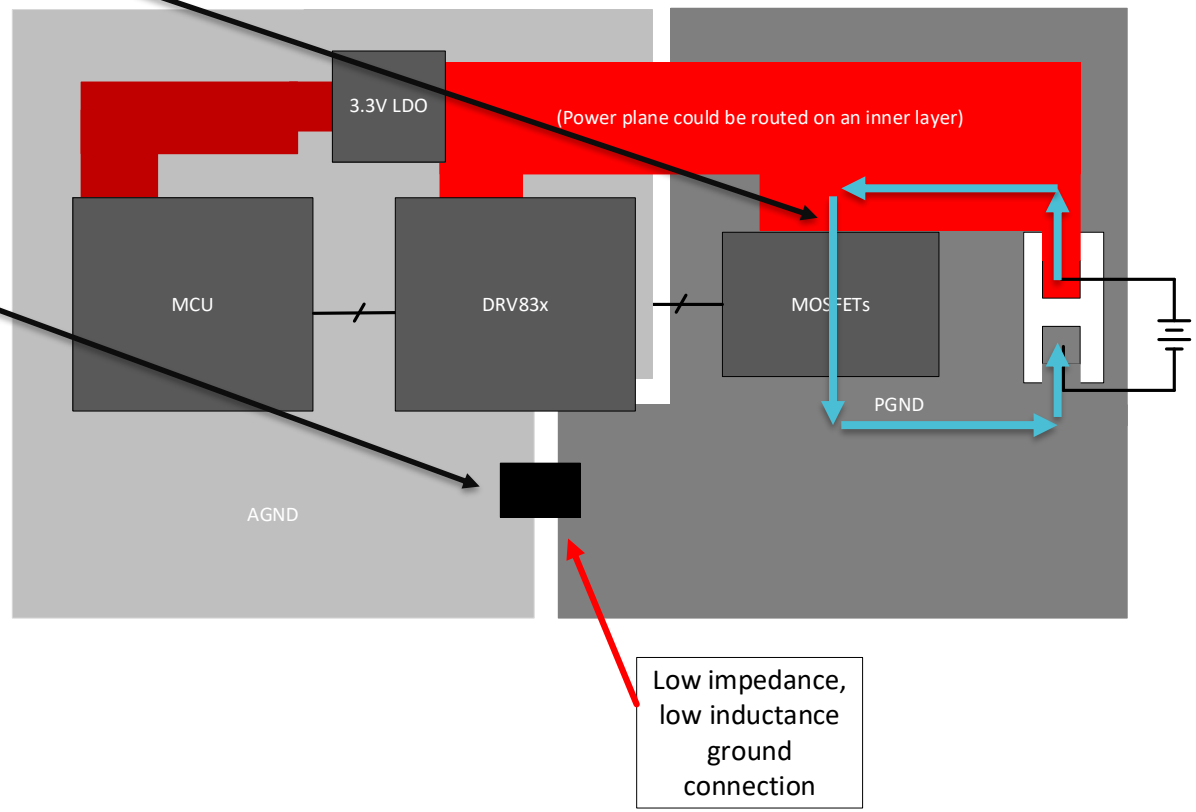
Supply and grounding

- Wide paths from power supply to HS drains of the MOSFET power stage.
- Bulk caps near power supply.
- Grounding needs wide paths for current flow and thermal dissipation.
- If split ground is used, grounds must be connected with a low impedance, low inductance connection near the driver (i.e. net tie, 0-ohm resistor).



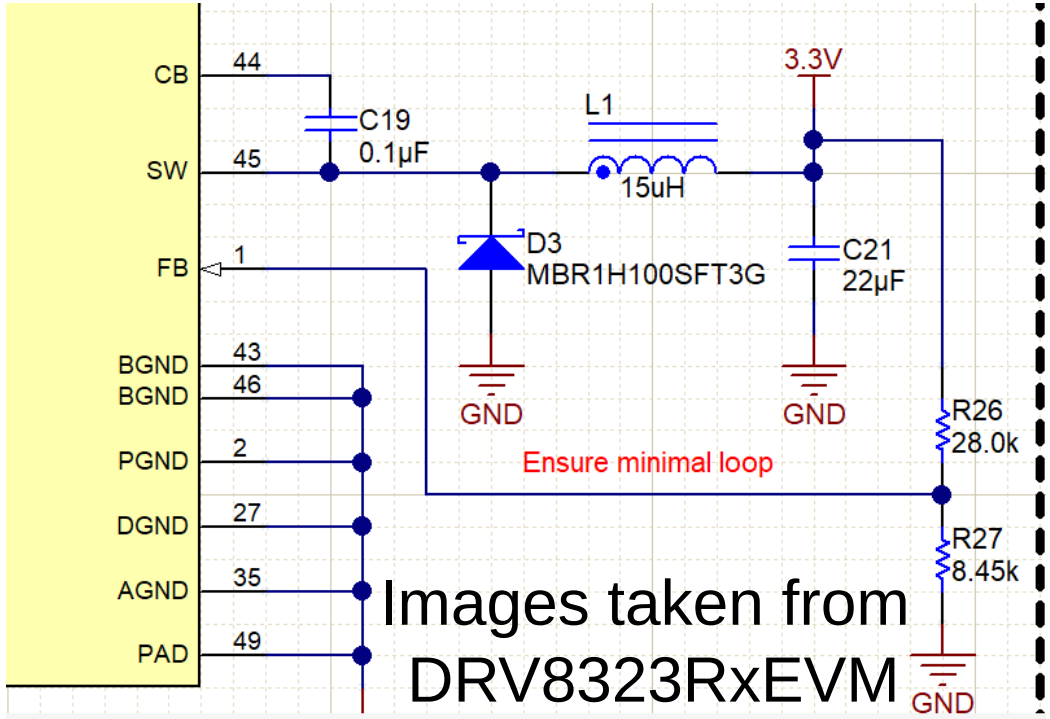
Supply and grounding – split ground example

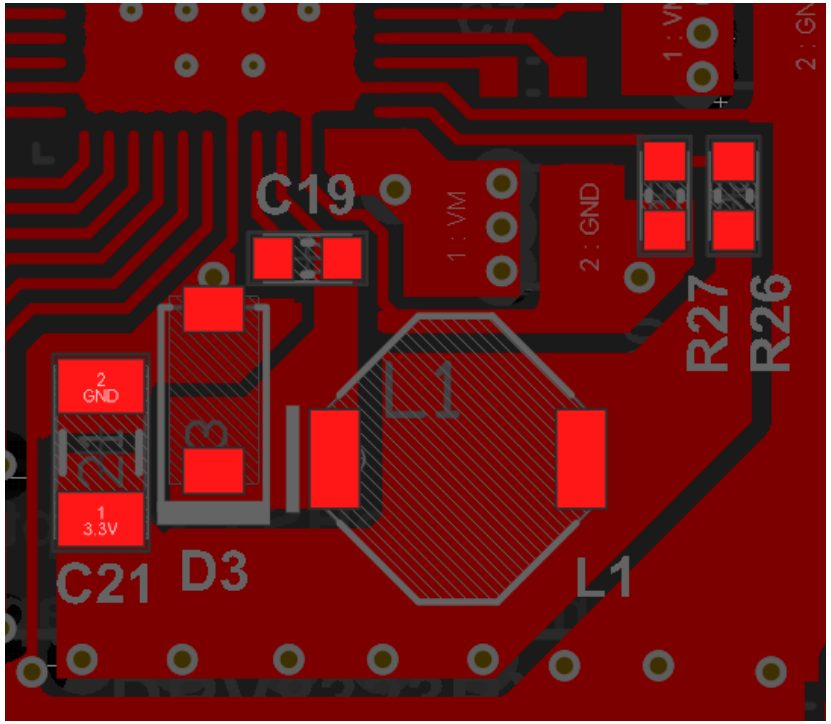
- Noisy MOSFET ground path doesn't flow over the quieter analog signals.
- Low impedance low inductance ground connection minimizes ground potential difference.
- Inner layers can be used for AGND and PGND connected to the supply.



Integrated buck layout tips

- Wide buck switch node connection/pour to reduce parasitic inductance.
- Short buck ground return loop for buck output.
- CB-SW cap placed as close to the device as possible.





Analog-related – VDS monitoring signals

- VDRAIN pin used for the drain sensing for all 3 high side VDS monitors.
- Have a dedicated trace from the VDRAIN pin back to the high side MOSFET drains.
- Want to accurately sense the VDS voltage drop across the MOSFETs.

Analog-related – CSA output & resistor inputs

- CSA output filtering components placed near the MCU's ADC pins.
- Voltage reference for CSAs should have low ripple with bypass capacitor placed near the DRV IC.
- External resistors for hardware variants should be placed close to the device for accurate analog voltages and hardware settings.

Digital-related

- SPI should be routed differentially away from sensitive analog signals (CSA outputs).
- Prioritize fast switching signals over slow-switching signals.
- Open-drain outputs such as SDO, nFAULT, and FGOUT should not be too long or else trace capacitance can affect RC time constant for the external pull-up.
  - Pullup resistor on the SDO line should be placed close to the pin of the DRV

Conclusion

- Hardware design files can be found on the EVM's product page, including schematic and layout files for comparison.
- Layout reviews should focus on mitigating parasitics in the motor driver paths, gate drive outputs, and power stage for robust motor performance.
- Prioritize motor driver component placement and layout based on most critical circuits.
- Consult TI reference designs and application notes for information on schematic design, layout practices and high-power system design.
  - System Design Considerations for High-Power Motor Driver Applications
  - Best Practices for Board Layout of Motor Drivers

To find more BLDC motor driver technical resources and search products, visit **ti.com/bldc**