Motor startup problem on Avenger Servo drives.

1. Background.
   An in-house designed BLDC servo drive unit used in a robotic vehicle drive track control has been in production for approx. 7 years. The drive uses the TI DRV8303 three phase gate drive controller as the power mosfet control gate drive IC interface between the uP control and the high power bridge.
   There were some initial problems in the early versions of the drive with overvoltage spikes damaging the DRV8303 devices. This was due to layout issues but these were resolved with a new layout and the addition protection devices. The units have run pretty much trouble free since then.

   However there has been an underlying problem with a small percentage of these drives since the start of production. On these small number of drives, the motors will not start immediately when a drive command is issued. Instead, the motor stays stationary for a number of seconds and then kicks into motion. The motor behaves normally after that.
   This is not a consistent problem i.e. it does not happen every time a motor start command is issued.
   The percentage of units affected has not been accurately determined but it is estimated to be approx. 1% of units.

   The problem units have been put aside for the last number of years but now it needs to be examined again to try to fully understand what is happening. It is important to eliminate the problem as there is a risk that these problem units could pass production test and only exhibit the problem in new vehicles in the field.

2. Detailed description of the problem.
   A drive command is issued to the drive via CAN. This command normally starts the drive to rotate at the requested speed. However in these problem drives, the motor does not start immediately and behaves as described above i.e. the motor stays stationary for a number of seconds and then kicks into motion and behaves normally after that. This is an intermittent behaviour on these problem drives but is relatively easy to reproduce.

   Further investigation of the problem shows the following:

   When the drive command is issued, the EN_GATE signal goes hi and the PWM signals are issued immediately to the DRV8303 from the uP.
   PWM frequency is 20kHz. The control mode is two phase control i.e. only two of the motor phases are activated at any one time like traditional trapezoidal BLDC control.
   When this problem occurs, even though the device is enabled, gate drive signals are not sent from the DRV8303 to the power mosfets. All gate drive signals are low.
   The device is not in a fault condition i.e. nFAULT and nOCTW remain hi.
   The drive sits un-activated for a number of seconds. At this stage the uP motor control S/W sees that there is no motion and increases the pwm duty cycle until it saturates and then flips over and activates the next phase sequence.

At this point the DRV8303 sends out gate control signals to the motor, the motor kicks into motion momentarily in a uncontrolled manner until control is regained. After that the unit behaves normally. This also indicates that there is no latched fault in the device as it recovers without any new enable signal being issued.
The problem is only associated with a very small percentage of drives and can be difficult to reproduce.

Has any operation like this been reported previously?
Any help or suggestions would be greatly appreciated.

Monitored the three PWMX_L signals (triggered off of the Gate_EN signal going hi. When the problem occurs any one of the three phases can be the non active phase.
Effect also related to battery voltage. When batteries were discharged or at a low voltage (approx. 33v) it was almost impossible to reproduce the problem. However with fully charged batteries (battery voltage approx. 37.3V) it was easy to reproduce the problem.

3. Scope plots.

General note on scope plots:
All the plots shown here relate to the C channel of the DRV8303 just for ease of interpretation. Channels A and B were also monitored and the behaviour is the same as for channel C.
Additionally the plots show the GL_C gate drive signal again for ease of interpretation. The GH_C was also monitored. When GL_C was not transmitted from the DRV8303 neither was the GH_C transmitted. It was the same for channels B and C. These additional plots can be submitted if required.

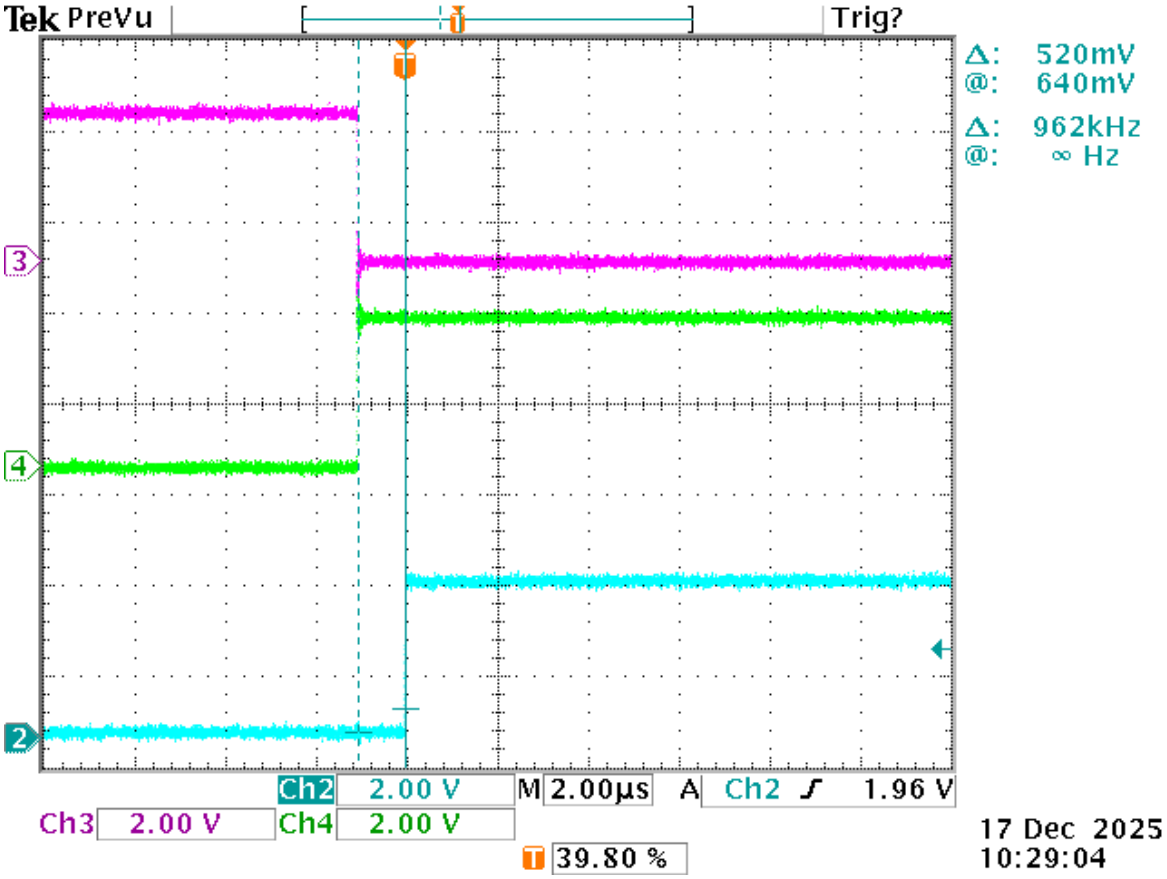

Fig1. Ch2: GATE_EN, Ch4: INL_C, Ch3: INH_C. Plot shows that the PWM signals are activated approx. 1uS before gate enable is issued. This plot was taken on an instance where the motor did not activate for a number of seconds. It's identical for the instance where the motor starts immediately.

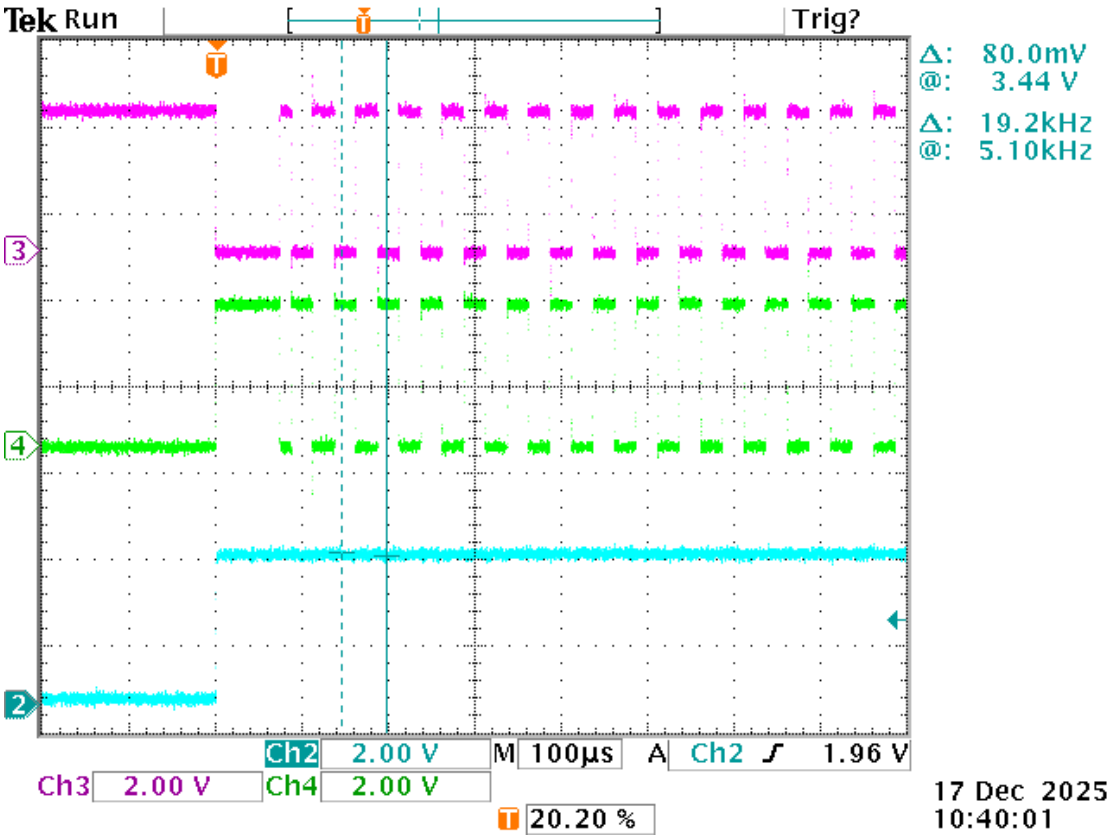

Fig2. Ch2: GATE_EN, Ch4: INL_C, Ch3: INH_C. Plot shows the PWM sequence for a longer period (longer timebase) after GATE_EN signal goes hi. This plot was taken on an instance where the motor did not activate for a number of seconds. It's identical for the instance where the motor starts immediately.

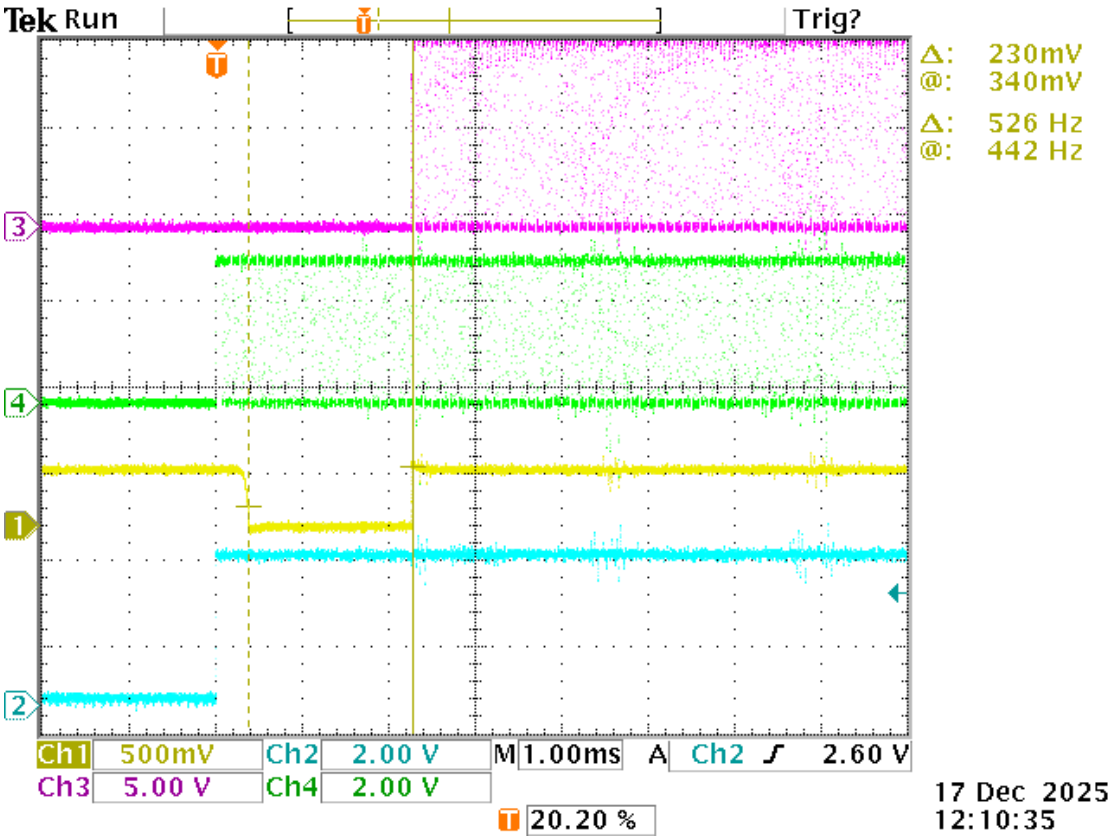

Fig3. Ch2: GATE_EN, Ch4: INL_C, Ch3: GL_C. Ch1 (5v/div): FAULT

Plot shows Gate_en going hi and INL_C signals starting at the same time. A little time after this we see FAULT going hi indicating that there is a fault in the chip. After 2ms approx. the fault is cleared automatically by the device and the GL_C gate drive signals are issued to the power FETs and the motor starts. We can see later in the plots below the reason for the short fault condition (Time for GVDD to reach good limits)

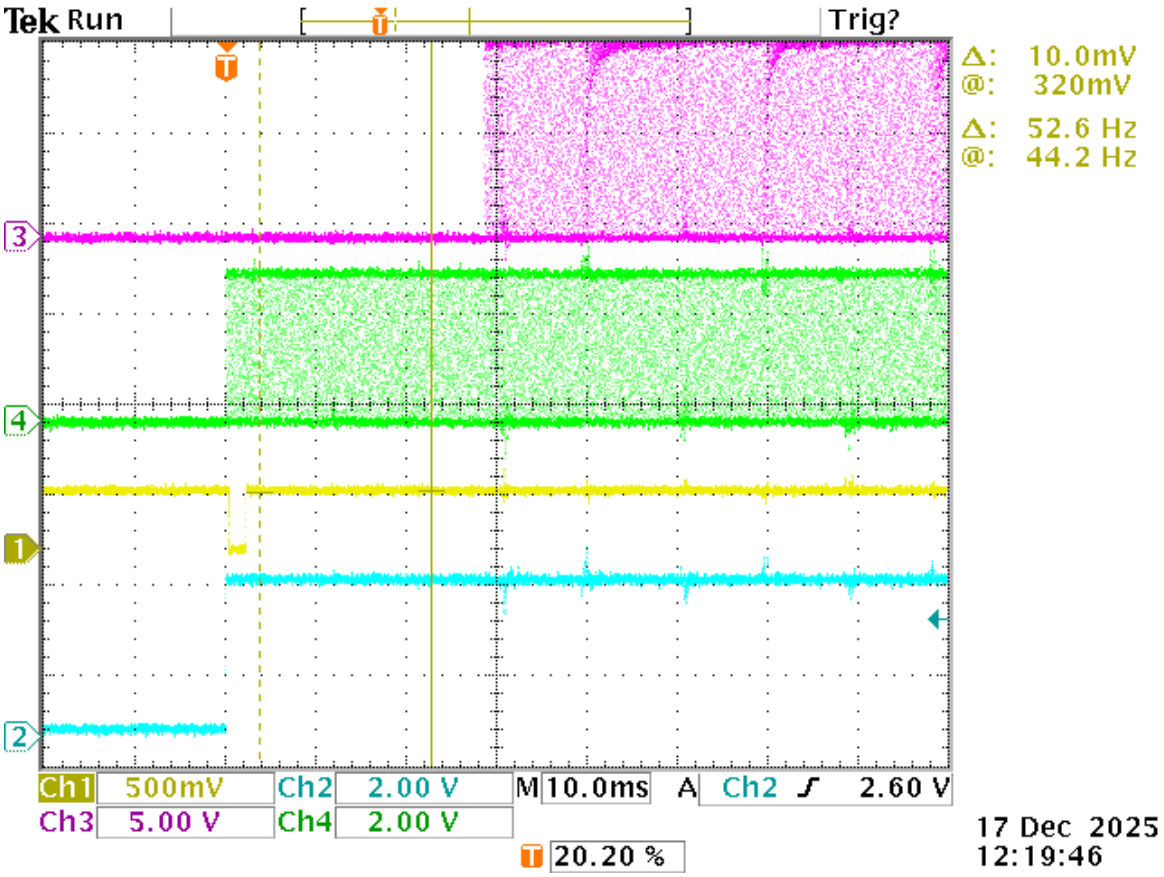

Fig4. Ch2: GATE_EN, Ch4: INL_C, Ch3: GL_C. Ch1 (5v/div): FAULT
Plot shows Gate_en going hi (Longer time base as opposed to Fig 3 above). A little time after this we see FAULT going hi indicating that there is a fault in the chip. After 2ms approx. the fault is cleared automatically by the device. However in this case there is a further unexplained delay of approx. 30mS before the GL_C gate drive signals are issued to the power FETs. Motor still starts in this scenario. The 30 mS delay is not noticeable.

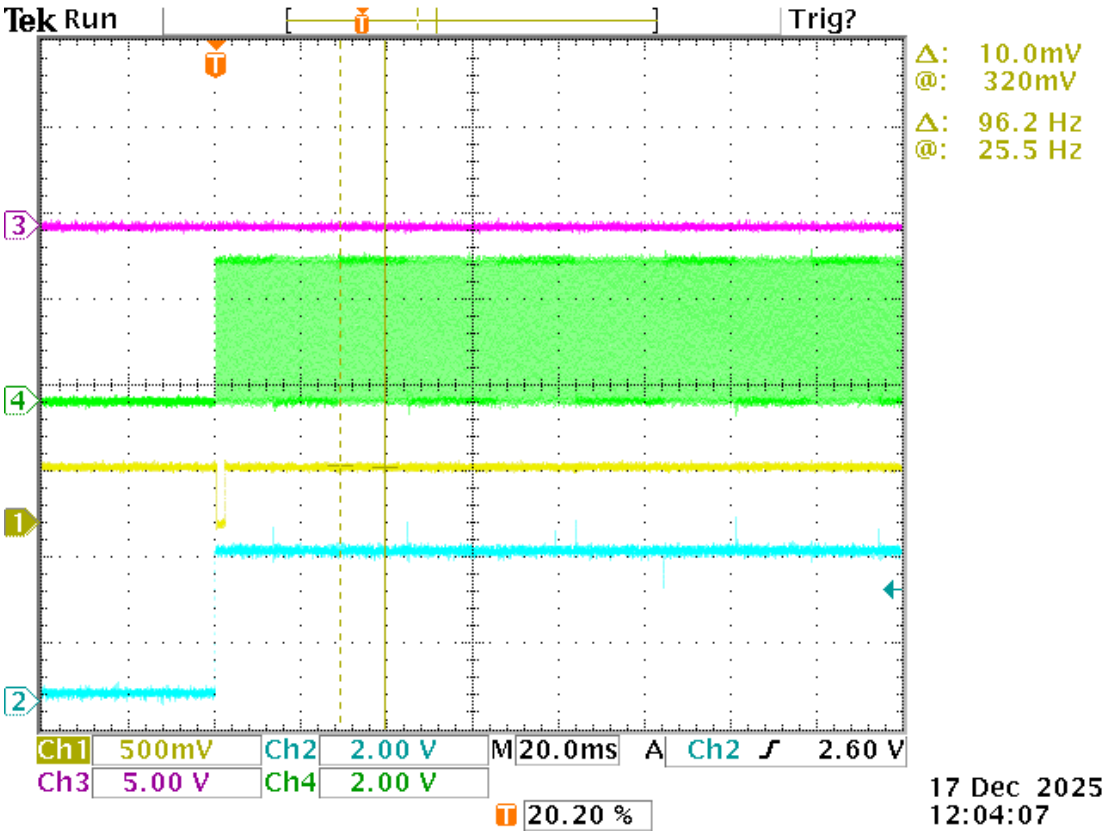

Fig5. Ch2: GATE_EN, Ch4: INL_C, Ch3: GL_C. Ch1 (5v/div): FAULT
Plot shows Gate_en going hi. A little time after this we see FAULT going hi indicating that there is a fault in the chip. After 2ms approx. the fault is cleared automatically by the device. However in this case the GL_C gate drive signals are not issued to the power mosfets for approx. 3-4 seconds. During this 3-4 second period the motor does not start.

Eventually after the 3-4 second period the motor control S/W saturates the phase that was not activated (BLDC two phase control scheme) now gets activated, As soon as the new set of PWM signals is activated by the uP the DRV8303 seems to ‘wake up’ and send gate drive signals to the power mosfets and the motor turns.

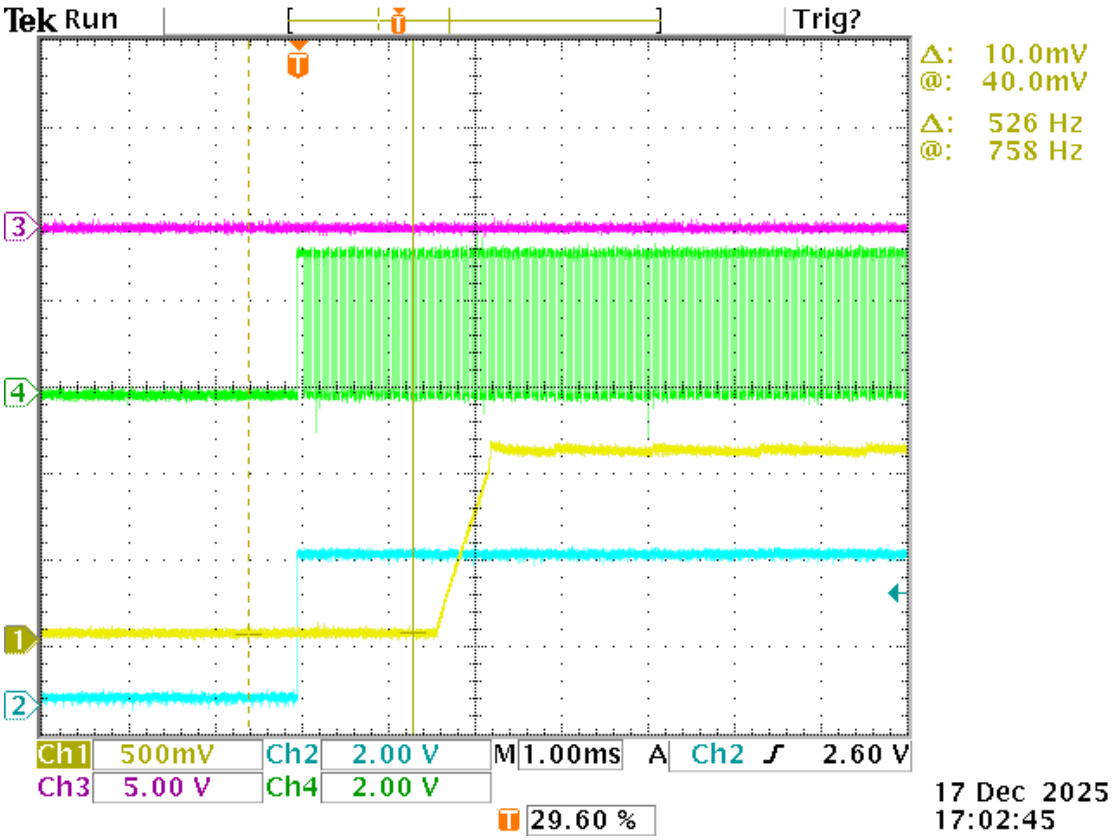

Fig6. Ch2: GATE_EN, Ch4: INL_C, Ch3: GL_C. Ch1 (5v/div): GVDD
Plot shows GATE_EN going hi. GVDD starts to charge 1.5mS later and is within limits after approx. 2mS. (this is the reason for the short FAULT condition in previous plots.)
In this instance the gate drive signals are not transmitted by the DRV8303 i.e. no signals on Ch3 above. (as yet unexplained) but are delayed for the 3-4 seconds (as described in Fig 5 above). The motor does not move until then.

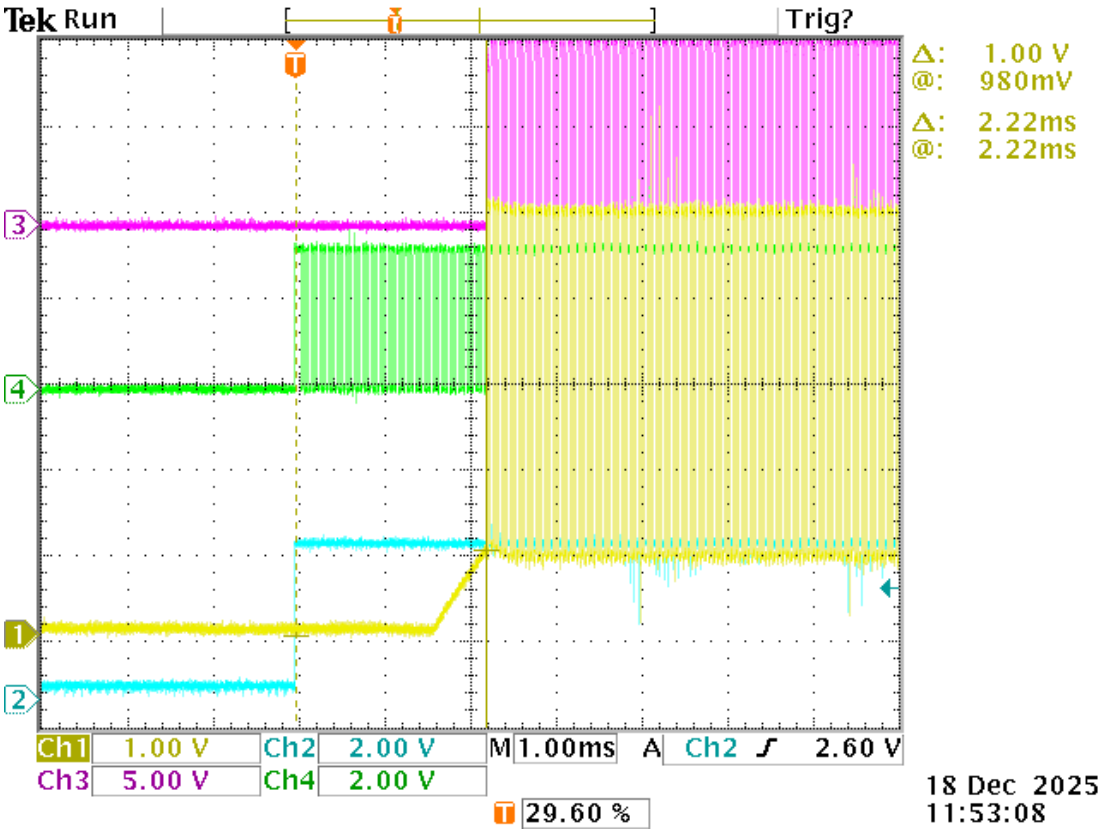

Fig7. Ch2: GATE_EN, Ch4: INL_C, Ch3: GL_C. Ch1 (10v/div): BST_C
Plot shows GATE_EN going hi. BST_C starts to charge 1.5mS later and is within limits after approx. 2.2mS. At this point the DRV8303 transmits the gate drive signals and the bridge starts to switch. BST_C then switches between GVDD level (when lower mosfet is on) and Vbus + GVDD (when upper mosfet is on).
In this instance the motor activated normally.

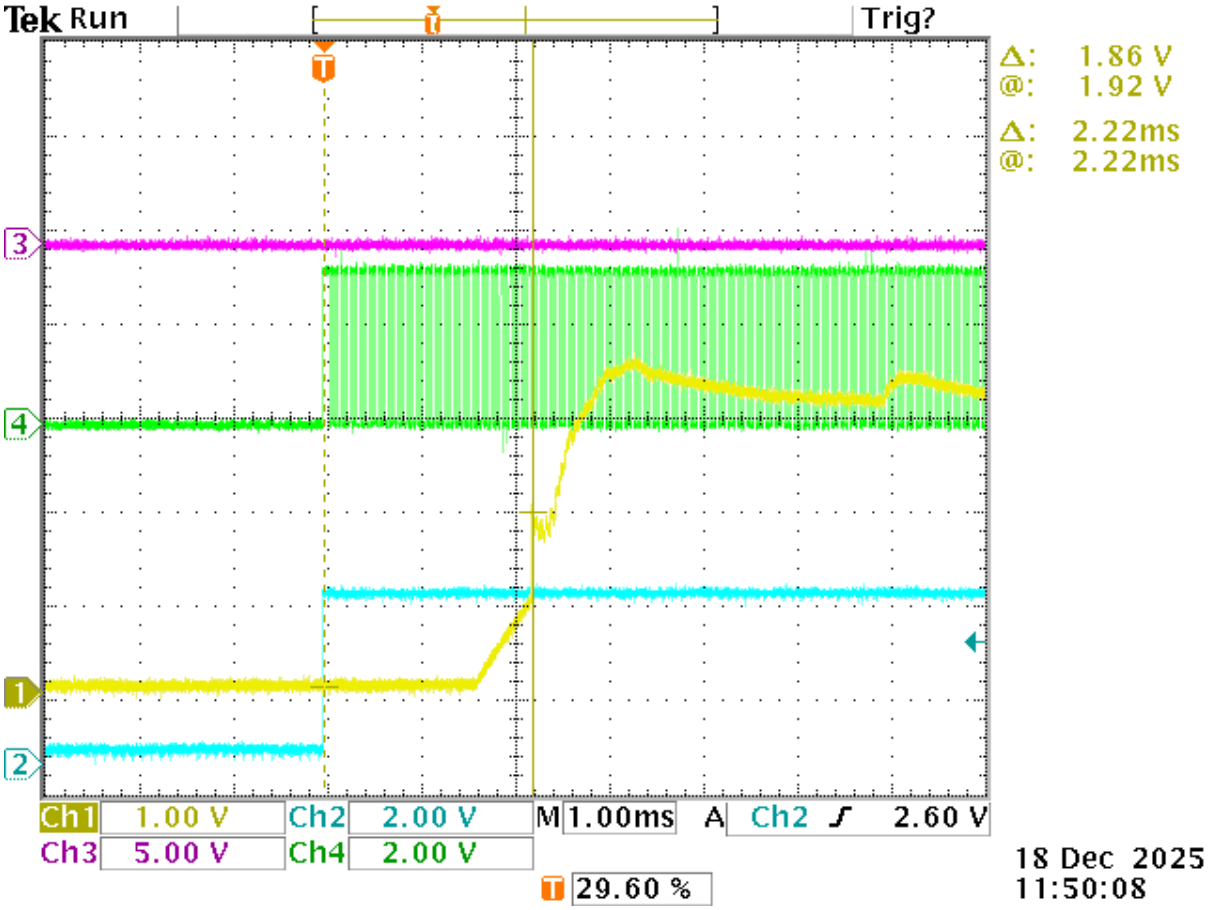

Fig8. Ch2: GATE_EN, Ch4: INL_C, Ch3: GL_C. Ch1 (10v/div): BST_C
Plot shows GATE_EN going hi. BST_C starts to charge 1.5mS later and is within limits after approx. 2.2mS. At this point in this case the DRV8303 does not transmit the gate drive signals as it should to the power mosfets. (Gate drive signals are not seen on Ch3 which is the gate drive signals to the lower C mosfet.) The BST_C voltage is not determined and this also shows that the bridge is not switching during this period.
In this instance the motor did not activate for a number of seconds i.e the fault condition that is as yet unexplained.

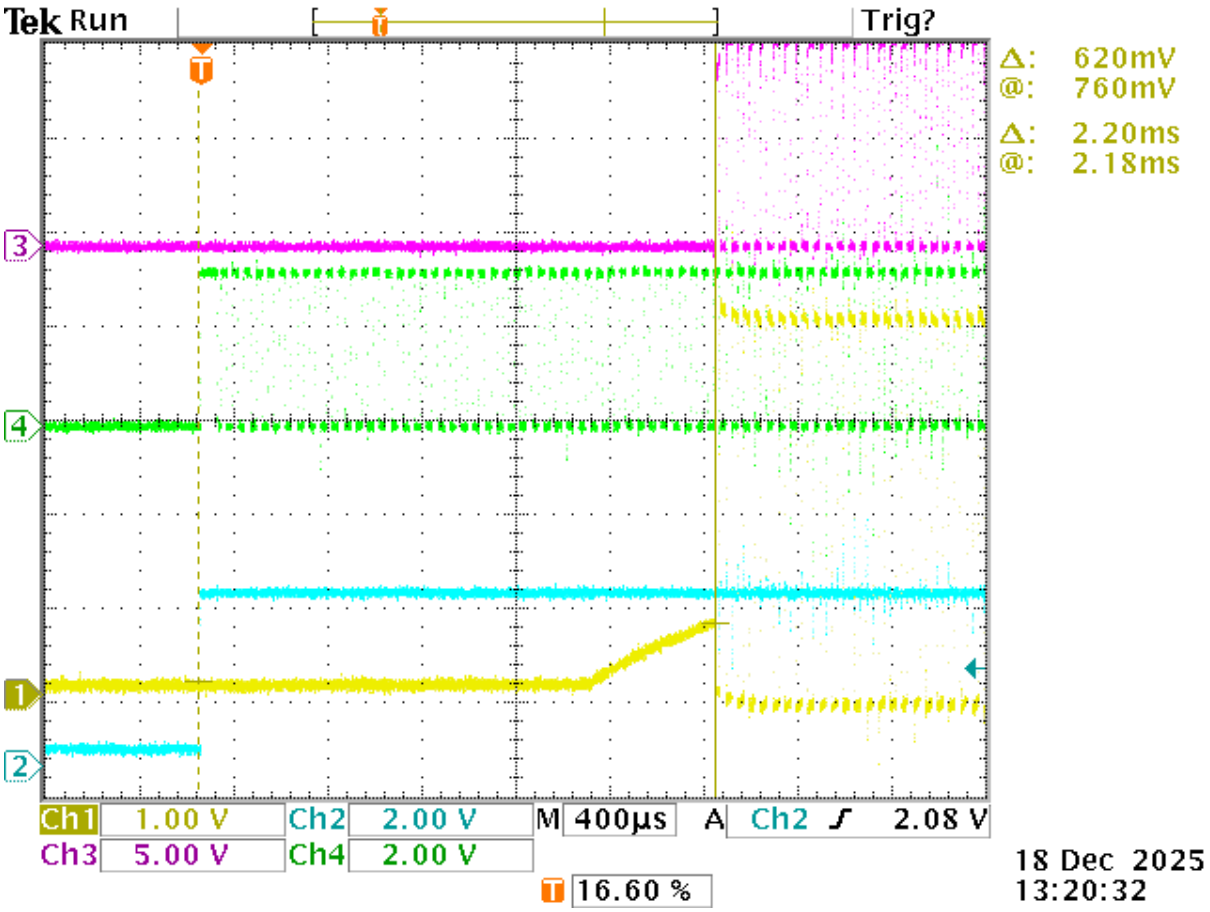

Fig9. Ch2: GATE_EN, Ch4: INL_C, Ch3: GL_C. Ch1 (10v/div): SH_C
Plot shows GATE_EN going hi. 2.2 mS later the DRV8303 transmits gate drive signals.

There is an errata in the datasheet 8.1.1 that states:

8.1.1 Gate Driver Power-Up Sequencing Errata
The DRV8301 gate drivers may not correctly power up if a voltage greater than 8.5 V is present on any SH_X pin when EN_GATE is brought logic high (device enabled) after PVDD power is applied (PVDD1 > PVDD_UV). This sequence should be avoided by ensuring the voltage levels on the SH_X pins are less than 8.5 V when the DRV8301 is enabled through EN_GATE.

This plot shows that the voltage on the SH_C pin is less than 8.5V on device. SH_B and SH_A were also monitored during gate enable going hi. Characteristic was the same as that shown for SH_C in fig 9 above.