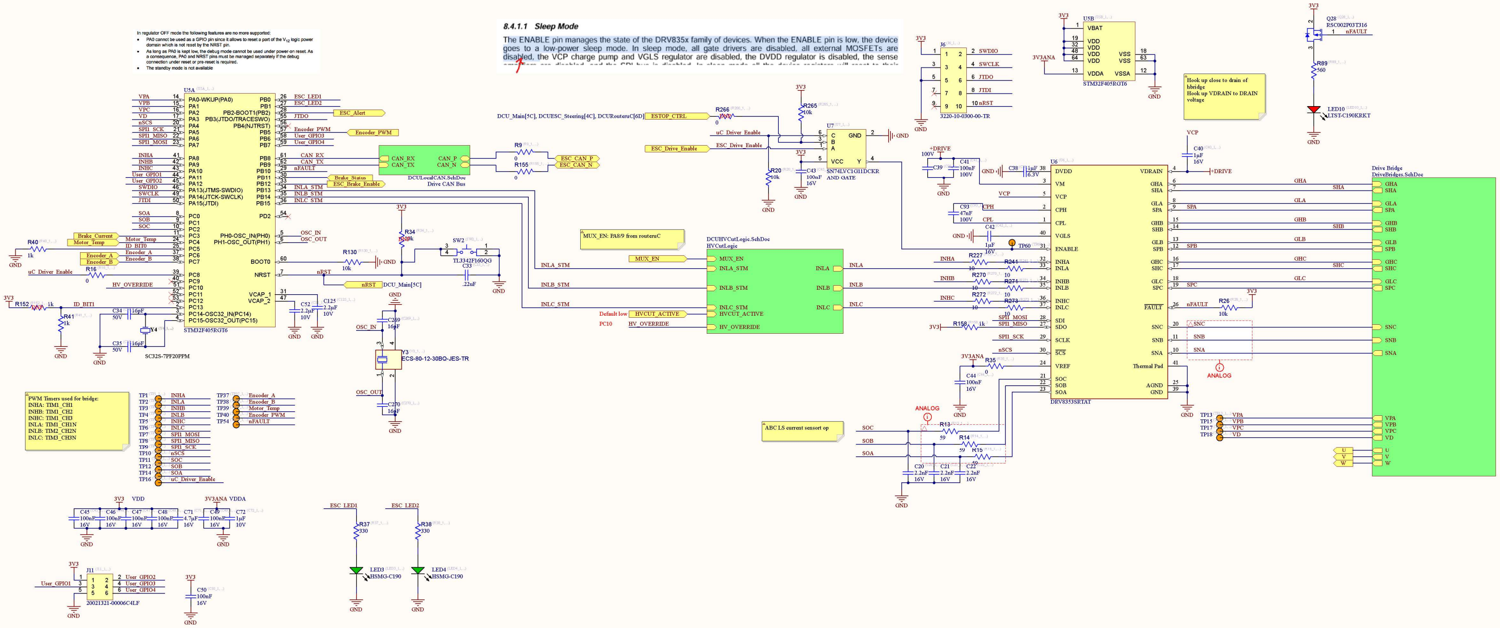
Bypass the VM pin to the GND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 μF. Place this capacitor as near to the VM pin as possible with a thick trace or ground plane connected to the GND pin. Additionally, bypass the VM pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10 μF.



In regulator OFF mode the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The standby mode is not available

8.4.1.1 Sleep Mode

The ENABLE pin manages the state of the DRV835x family of devices. When the ENABLE pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, all external MOSFETs are disabled, the VCP charge pump and VGLS regulator are disabled, the DVDD regulator is disabled, the sense

Hook up close to drain of hbridge
Hook up VDRAIN to DRAIN voltage

MUX_EN: PA8/9 from routeruC

PWM Timers used for bridge:
INHA: TIM1_CH1
INHB: TIM1_CH2
INHC: TIM1_CH3
INLA: TIM1_CH1N
INLB: TIM2_CH2N
INLC: TIM3_CH3N

ABC LS current sensort op

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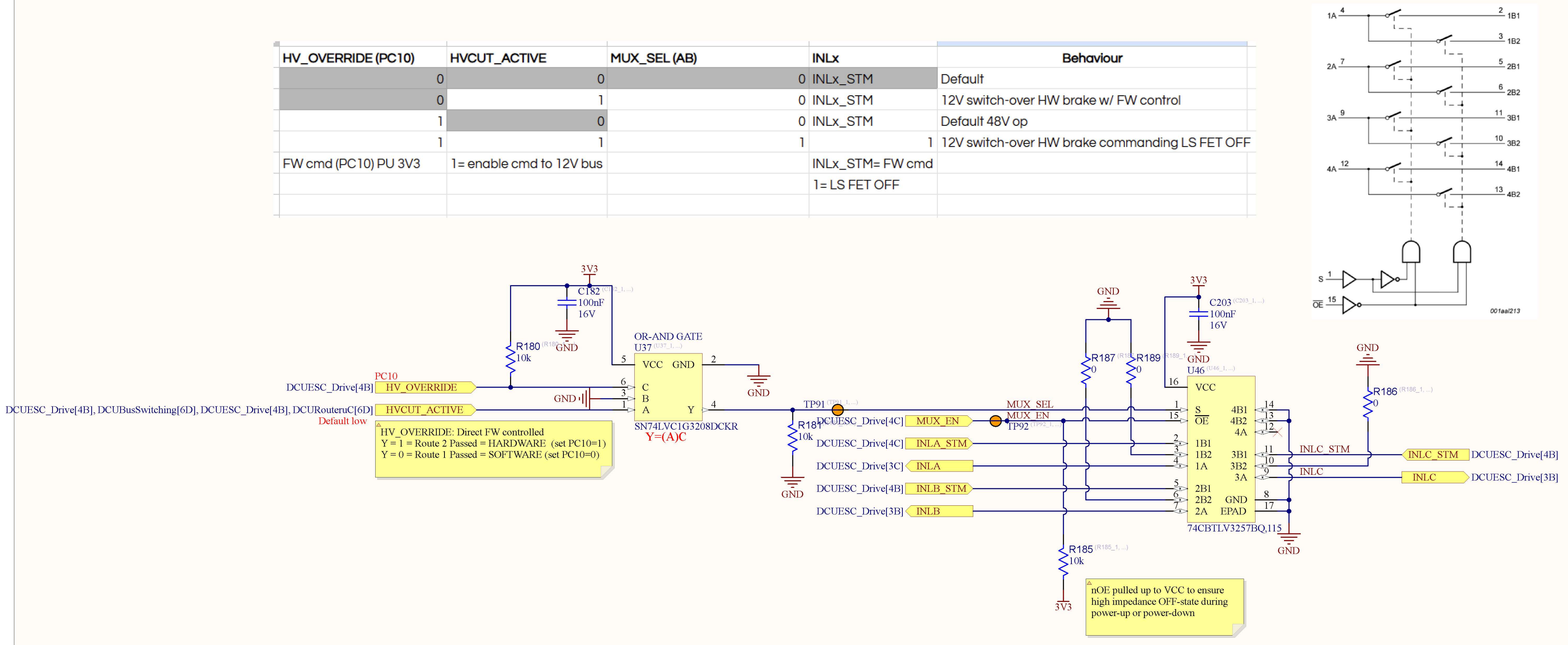
HV_OVERRIDE (PC10)	HVCUT_ACTIVE	MUX_SEL (AB)	INLx	Behaviour
0	0	0	INLx_STM	Default
0	1	0	INLx_STM	12V switch-over HW brake w/ FW control
1	0	0	INLx_STM	Default 48V op
1	1	1	1	12V switch-over HW brake commanding LS FET OFF
FW cmd (PC10) PU 3V3	1= enable cmd to 12V bus		INLx_STM= FW cmd	
			1= LS FET OFF	



HV_OVERRIDE: Direct FW controlled
Y = 1 = Route 2 Passed = HARDWARE (set PC10=1)
Y = 0 = Route 1 Passed = SOFTWARE (set PC10=0)

nOE pulled up to VCC to ensure high impedance OFF-state during power-up or power-down

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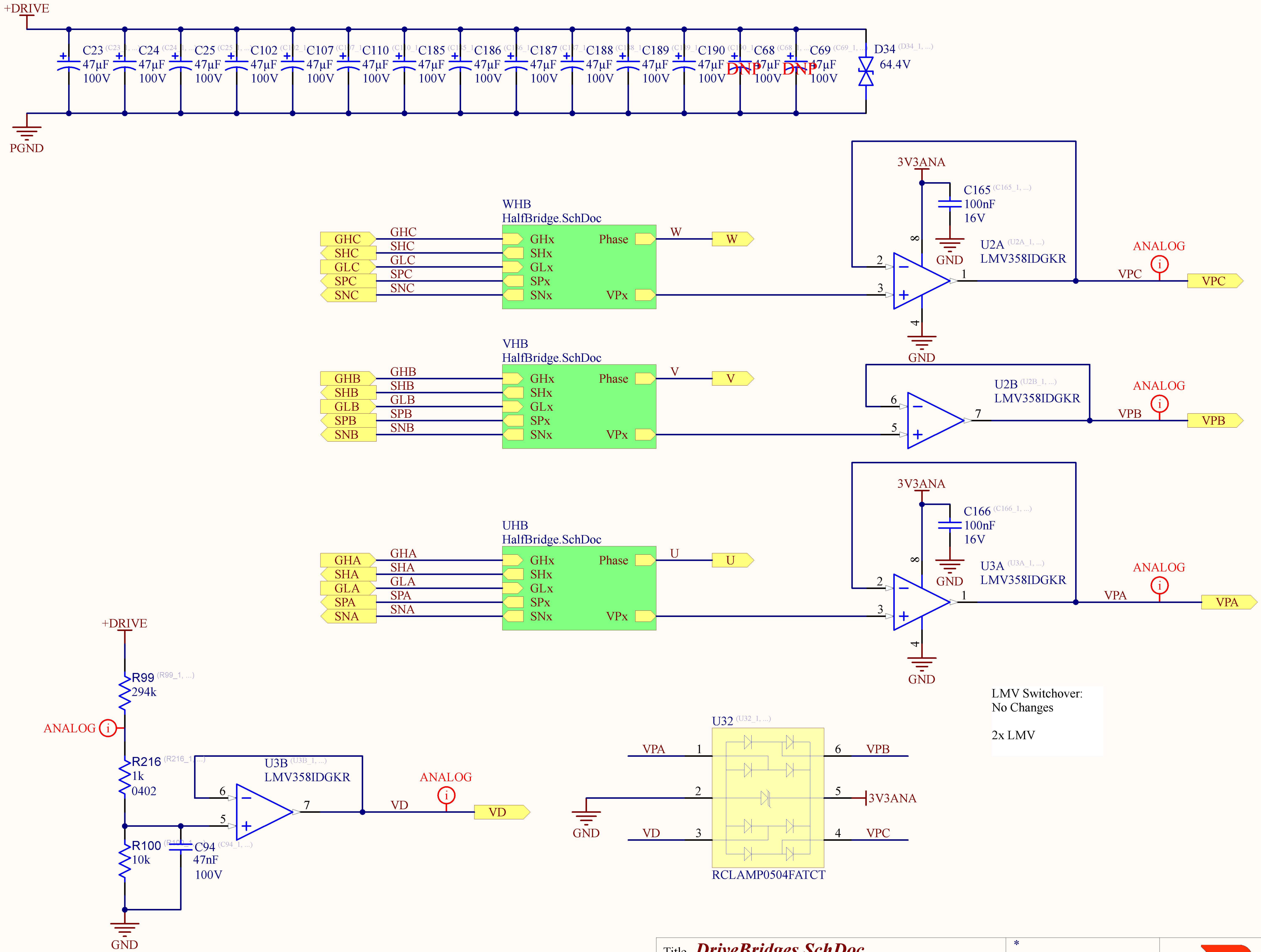

LMV Switchover:
No Changes

2x LMV

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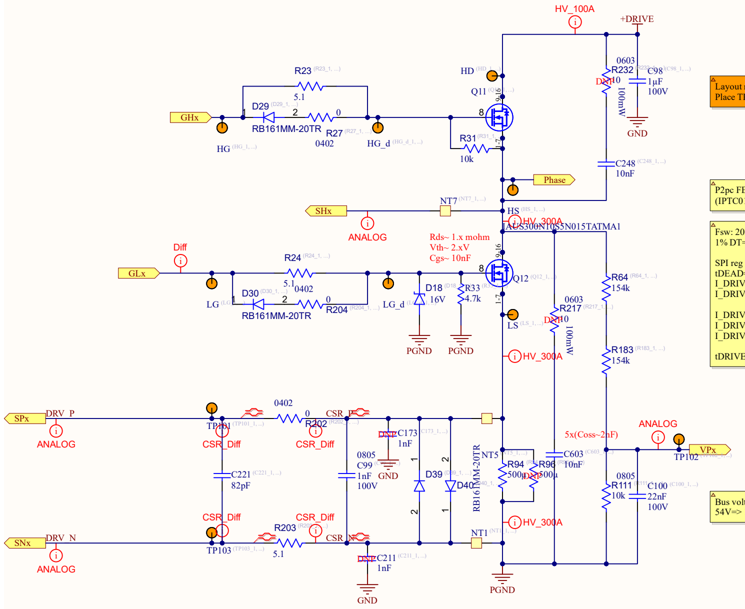
DRV8353S and DRV8353RS													
Fault Status 1	FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	R	0h
VGS Status 2	SA_OC	SB_OC	SC_OC	OTW	GDUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	R	1h
Driver Control	OCP_ACT	DIS_GDUV	DIS_GDF	OTW_REP	PWM_MODE		1PWM_COM	1PWM_DIR	COAST	BRAKE	CLR_FLT	RW	2h
Gate Drive HS	LOCK			IDRIVEP_HS				IDRIVEN_HS				RW	3h
Gate Drive LS	CBC	TDRIVE		IDRIVEP_LS				IDRIVEN_LS				RW	4h
OCP Control	TRETRY	DEAD_TIME		OCP_MODE		OCP_DEG		VDS_LVL				RW	5h
CSA Control	CSA_FET	VREF_DIV	LS_REF	CSA_GAIN		DIS_SEN	CSA_CAL_A	CSA_CAL_B	CSA_CAL_C	SEN_LVL		RW	6h
Reserved	Reserved										CAL_MODE	RW	7h



Layout notes:
Place TPs on this page on brd TOP layer

P2pc FET
(IPTC012N08NM5A

Fsw: 20kHz
1% DT= 1/(20e3)/100/1e-6= 500nS

SPI reg setting
tDEAD=11b (500ns DT i.e. 1% of Fsw)
I_DRIVEP (mid pull up)
I_DRIVEP_HS or I_DRIVEP_LS=1000b (550mA)

I_DRIVEN
I_DRIVEN_HS=100b (1000mA) moderate pull down when LS turn on
I_DRIVEN_LS= 111b (2000mA) strong pull down when HS turn on

tDRIVE= 11b default setting. No change.

Bus voltage 0.03X
54V=> 1.77V

t_{DEAD}	Gate drive dead time	SPI Device	DEAD_TIME = 00b	50	ns
			DEAD_TIME = 01b	100	
			DEAD_TIME = 10b	200	
			DEAD_TIME = 11b	400	
		H/W Device		100	
t_{DRIVE}	Peak current gate drive time	SPI Device	TDRIVE = 00b	500	ns
			TDRIVE = 01b	1000	
			TDRIVE = 10b	2000	
			TDRIVE = 11b	4000	
		H/W Device		4000	

I_{DRIVEP}	Peak source gate current	SPI Device	IDRIVEP_HS or IDRIVEP_LS = 0000b	50	mA
			IDRIVEP_HS or IDRIVEP_LS = 0001b	50	
			IDRIVEP_HS or IDRIVEP_LS = 0010b	100	
			IDRIVEP_HS or IDRIVEP_LS = 0011b	150	
			IDRIVEP_HS or IDRIVEP_LS = 0100b	300	
			IDRIVEP_HS or IDRIVEP_LS = 0101b	350	
			IDRIVEP_HS or IDRIVEP_LS = 0110b	400	
			IDRIVEP_HS or IDRIVEP_LS = 0111b	450	
			IDRIVEP_HS or IDRIVEP_LS = 1000b	550	
			IDRIVEP_HS or IDRIVEP_LS = 1001b	600	
			IDRIVEP_HS or IDRIVEP_LS = 1010b	650	
			IDRIVEP_HS or IDRIVEP_LS = 1011b	700	
			IDRIVEP_HS or IDRIVEP_LS = 1100b	850	
			IDRIVEP_HS or IDRIVEP_LS = 1101b	900	
			IDRIVEP_HS or IDRIVEP_LS = 1110b	950	
			IDRIVEP_HS or IDRIVEP_LS = 1111b	1000	
		H/W Device	IDRIVE = Tied to GND	50	
			IDRIVE = 18 kΩ ± 5% tied to GND	100	
			IDRIVE = 75 kΩ ± 5% tied to GND	150	
			IDRIVE = Hi-Z	300	
			IDRIVE = 75 kΩ ± 5% tied to DVDD	450	
			IDRIVE = 18 kΩ ± 5% tied to DVDD	700	
			IDRIVE = Tied to DVDD	1000	

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRIVEN}	Peak sink gate current	SPI Device	IDRIVEN_HS or IDRIVEN_LS = 0000b		100		mA
			IDRIVEN_HS or IDRIVEN_LS = 0001b		100		
			IDRIVEN_HS or IDRIVEN_LS = 0010b		200		
			IDRIVEN_HS or IDRIVEN_LS = 0011b		300		
			IDRIVEN_HS or IDRIVEN_LS = 0100b		600		
			IDRIVEN_HS or IDRIVEN_LS = 0101b		700		
			IDRIVEN_HS or IDRIVEN_LS = 0110b		800		
			IDRIVEN_HS or IDRIVEN_LS = 0111b		900		
			IDRIVEN_HS or IDRIVEN_LS = 1000b		1100		
			IDRIVEN_HS or IDRIVEN_LS = 1001b		1200		
			IDRIVEN_HS or IDRIVEN_LS = 1010b		1300		
			IDRIVEN_HS or IDRIVEN_LS = 1011b		1400		
			IDRIVEN_HS or IDRIVEN_LS = 1100b		1700		
			IDRIVEN_HS or IDRIVEN_LS = 1101b		1800		
			IDRIVEN_HS or IDRIVEN_LS = 1110b		1900		
			IDRIVEN_HS or IDRIVEN_LS = 1111b		2000		
		H/W Device	IDRIVE = Tied to GND		100		
			IDRIVE = 18 kΩ ± 5% tied to GND		200		
			IDRIVE = 75 kΩ ± 5% tied to GND		300		
			IDRIVE = Hi-Z		600		
			IDRIVE = 75 kΩ ± 5% tied to DVDD		900		
			IDRIVE = 18 kΩ ± 5% tied to DVDD		1400		
			IDRIVE = Tied to DVDD		2000		

Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz	-	12316	16011	pF
Output capacitance	C_{oss}		-	1920	2496	
Reverse transfer capacitance	C_{rss}		-	84	126	

Continuous low-side source sense pin voltage (SLx)	–1	1	V
Transient 200-ns low-side source sense pin voltage (SLx)	–5	5	V
Continuous shunt amplifier input pin voltage (SNx, SPx)	–1	1	V
Transient 200-ns shunt amplifier input pin voltage (SNx, SPx)	–5	5	V

7.1 Absolute Maximum Ratings

at T_A = –40°C to +125°C (unless otherwise noted)(1)

	MIN	MAX	UNIT
GATE DRIVER			
Power supply pin voltage (VM)	–0.3	80	V
Voltage differential between ground pins (AGND, BGND, DGND, PGND)	–0.3	0.3	V
MOSFET drain sense pin voltage (VDRAIN)	–0.3	102	V

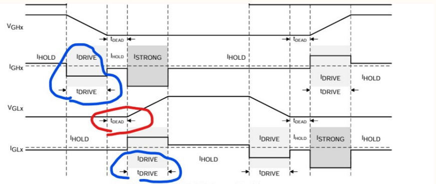
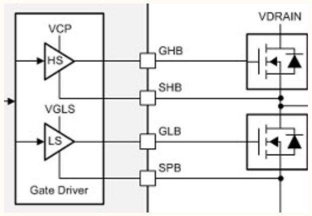


Figure 33. TDRIVE State Machine



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