TPS51372 3-V to 24-V, 6.5-A Synchronous Buck Converter With 2-Bit VID and Low-Power Mode

1 Features

- VIN Input Voltage Range: 3 V to 24 V
- VCC Input Voltage Range: 4.5 V to 5.5V
- VCCIO/PRIMCORE/V1.05A Compatible for IMVP8
- Compatible for Intel Kaby Lake/Sky Lake platforms
- Support 6.5 A Continuous Output Current
- Support 7.5 A Peak Output Current
- ±1% Output Voltage at Room Temperature
- Integrated 27 mΩ/12 mΩ $R_{DS(ON)}$ Internal Power Switch
- 78 uA Quiescent Current
- 2-Bit VID to Adjust Output Voltage
- D-CAP3™ Control Mode for Fast Transient Response
- Support POSCAP and All MLCC Output Capacitor Usage
- Build in Output Discharge Function
- 600 kHz Switching Frequency
- Power Good Indicator to Monitor Output Voltage
- Internal 1.0 ms Soft Start
- Latched Output OV/ UV Protection
- Non-Latch UVLO/ Over Temperature Protection
- Small 3.0 mm × 2.0 mm HotRod™ VQFN Package

2 Applications

- PC and Notebooks
- Embedded PC
- Industrial PC
- Merchant network and server PSU
- Distributed Power Systems

3 Description

The TPS51372 is a cost effective, high-voltage input, synchronous buck converter with integrated FETs. It has 2-bit VID (C0,C1) for VCCIO/PRIMCORE/V1.05A power rails in Intel Sky Lake/ Kaby Lake platforms, and supports 6.5A continuous output current. LP# pin supports Low Power Mode. LP# combined with VID pins help the system to minimize the power consumption in different applications. With wide operating input-voltage range of 3V to 24V, this device is ideally suited for system which is powered by 2s, 3s, 4s cells Li-Ion battery system or related adaptors. Latched OV/UV, and non-latched UVLO/ thermal shutdown protections are also available.

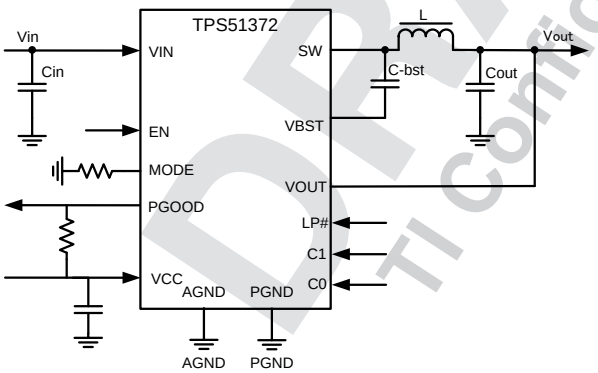
TPS51372 is available in a 3.00 mm × 2.00 mm thermal enhanced 13-pin HotRod™ VQFN package and is designed to operate from –40°C to 125°C junction temperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51372	VQFN (13)	3.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Efficiency vs Output Current

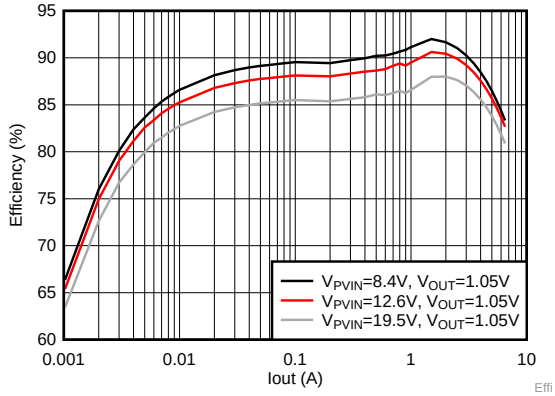


Table of Contents

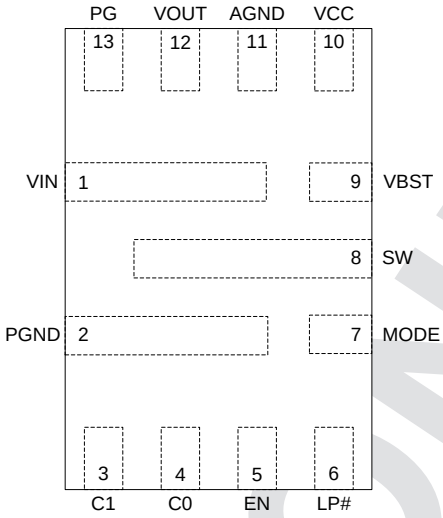
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2019	*	Advance Information release.

5 Pin Configuration and Functions

RJN Package
13-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	P	Input power supply for buck converter. Connect the input decoupling capacitors between VIN and PGND as close to VIN as possible.
PGND	2	G	Power GND terminal for the controller circuit and the internal circuitry.
C1,C0	3,4	I	2-bit VID control inputs. Set C1 and C0 with MODE to get different voltage references for different rails. Internal 2uA pulldown current to disable converter if leave these pins open.
EN	5	I	Enable pin of buck converter. EN pin is a digital input pin, decides turn on or off buck converter. Internal 2uA pulldown current to disable converter if leave this pin open.
LP#	6	I	Low power mode input pin. Internal 2uA pulldown current to disable converter if leave this pin open.
MODE	7	I	Selection pin for IMVP8 VCCIO/PRIMCORE/V1.0A/EDRAM/EOPOP with external 1% resistors.
SW	8	O	Switch node terminal. Connect the output inductor to this pin.
VBST	9	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between VBST and SW.
VCC	10	I	External 5V VCC input for controller and driver. Decouple with a minimum 1 μF ceramic capacitor as close to VCC as possible.
AGND	11	G	Analog ground pin.
VOUT	12	I	Output voltage sense pin of buck converter. Connect this pin to the output capacitor of the regulator directly.
PG	13	O	Open Drain Power Good Indicator. It is asserted low if output voltage is out of PGOOD threshold, overvoltage or if the device is under thermal shutdown, EN shutdown or during soft start.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Input voltage	VIN	–0.3	26	V
		VCC	–0.3	6	V
		VBST –SW	–0.3	6	V
		VBST	–0.3	31	V
		VOUT, EN, C0, C1, LP#, MODE	–0.3	6	V
		PGND	–0.3	0.3	V
		AGND	-0.3	0.3	V
	Output voltage	SW	–0.3	26	V
		SW (10-ns transient)	–4	28	V
		PG	–0.3	6	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Input voltage	VIN	–0.3	24	V
		VCC	–0.3	5.5	V
		VBST –SW	–0.3	5.5	V
		VBST	–0.3	29	V
		VOUT, EN, C0, C1, LP#, MODE	–0.3	5.5	V
		PGND	–0.3	0.3	V
		AGND	-0.3	0.3	V
	Output voltage	SW	–0.3	24	V
		SW(10 ns transient)	–4	26	V
		PG	–0.3	5.5	V
I_{OUT}	Output current (1)			6.5	A
T_J	Operating junction temperature		–40	125	°C
T_{stg}	Storage temperature		–40	150	°C

(1) In order to be consistent with the TI reliability requirement of 100k Power-On-Hours at 105°C junction temperature, the output current should not exceed 7.5A continuously under 100% duty operation as to prevent electromigration failure in the solder. Higher junction temperature or longer power-on hours are achievable at lower than 7.5A continuos output current.

6.4 Thermal Information

THERMAL METRIC(1)		TPS51372 RJN (VQFN) 13 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.0	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance with TI EVM	34.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{VIN} = 12 V, V_{VCC} = 5V, T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input Voltage Range		3		24	V
VCC	Input Voltage Range		4.5	5	5.5	V
I_{VCC}	VCC Supply Current	No load, V_{EN}=3.3V, R_{MODE}=100KΩ, Non Switching		78		µA
I_{VCC_LP}	VCC Stand-by Current	No load, V_{EN}=3.3V, R_{MODE}=0Ω, LP#=0V, C1=0V, C0=0V		47		µA
I_{INSDN}	VCC Shutdown Current	No load, V_{EN}=0V		6		µA
UVLO						
UVLO	VCC Under-Voltage Lockout	Wake up VCC voltage		4.2	4.4	V
		Shut down VCC voltage	3.5	3.7		V
		Hysteresis VCC voltage		500		mV
LOGIC THRESHOLD						
$V_{EN(ON)}$	EN Threshold High-level		1.6			V
$V_{EN(OFF)}$	EN Threshold Low-level				0.8	V
I_{EN}	EN Pull Down Current	V_{EN} = 0.8		2		uA
$V_{C0(H)}$	C0 Threshold High-level		1.6			V
$V_{C1(L)}$	C0 Threshold Low-level				0.8	V
I_{C0}	C0 Pull down Current	V_{C0} = 0.8		2		uA
$V_{C1(H)}$	C1 Threshold High-level		1.6			V
$V_{C1(L)}$	C1 Threshold Low-level				0.8	V
I_{C1}	C1 Pull Down Current	V_{C1} = 0.8		2		uA
$V_{LP(H)}$	LP Threshold High-level		1.6			V
$V_{LP(L)}$	LP Threshold Low-level				0.8	V
I_{LP}	LP Pull Down Current	V_{LP} = 0.8		2		uA
I_{MODE}	MODE Sourcing Current			10		uA
VOUT VOLTAGE						
V_{OUT}	V_{OUT} Voltage	T_J=25°C R_{MODE}=0Ω, LP=C0=3.3V,C1=0V	866.2	875	883.8	mV
		T_J=-40~125°C R_{MODE}=0Ω, LP=C0=3.3V, C1=0V	861.8	875	888.2	mV
T_{LP_EXIT}	Low Power Mode Exit Time	MODE=0 or 100K, C1=3.3V, C0=3.3V			100	uS
		MODE=200K, C1=3.3V, C0=3.3V			30	uS
		MODE=200K, C1=3.3V, C0=0V			26	uS
SR_{VID}	VID Change Slew Rate		12	14.5	17	mV/uS

Electrical Characteristics (continued)

V_{VIN} = 12 V, V_{VCC} = 5V, T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET						
$R_{DS\ (ON)HI}$	High Side MOSFET Rds(on)	T_J=25°C		27		mΩ
$R_{DS\ (ON)LO}$	Low Side MOSFET Rds(on)	T_J=25°C		12		mΩ
I_{OCL}	Over Current Threshold	Valley current set point	6.7	7.6	8.9	A
I_{NOCL}	Negative Over Current Threshold			3.2		A
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching Frequency			600		kHz
T_{MIN_ON}	Minimum On-time			50		ns
T_{MIN_OFF}	Minimum Off-time				180	ns
OUTPUT DISCHARGE and SOFT START						
R_{DIS}	Discharge Resistance	V_{VOUT} =0.5V, V_{EN}=0V		40		Ω
t_{SSRAMP}	Soft Start Time (Ramp-up)	VOUT=0% to VOUT=95%		1.0		ms
POWER GOOD						
T_{PGDLY}	PG Low to High Delay	PG from low to high		160		us
T_{PGDLY}	PG High to Low Delay	PG from high to low		32		us
V_{PGTH}	PG Threshold	VOUT falling (fault)		90		%
		VOUT rising (good)		95		%
		VOUT rising (fault)		115		%
		VOUT falling (good)		105		%
I_{PG}	PG Sink Current	V_{PGOOD} =0.5V		50		mA
I_{PGLK}	PG Leak Current	V_{PGOOD} =5.5V			1	uA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP Trip Threshold	VOUT rising		125		%
t_{OVPDLY}	OVP Prop Deglitch			32		us
V_{UVP}	UVP Trip Threshold	VOUT falling		60		%
t_{UVPDLY}	UVP Prop Deglitch			256		us
THERMAL PROTECTION						
T_{OTP}	OTP Trip Threshold			150		°C
T_{OTPHSY}	OTP Hysteresis			20		°C

6.6 Typical Characteristics

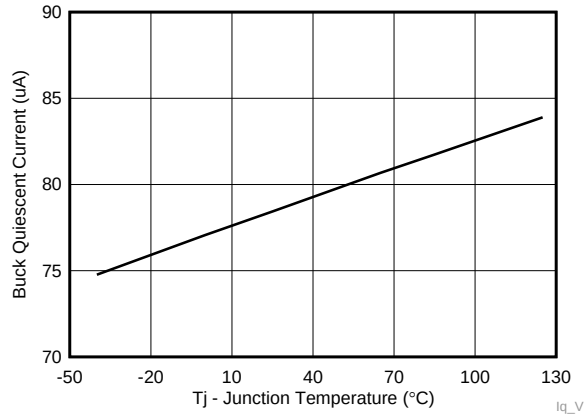


Figure 1. Quiescent Current vs Temperature

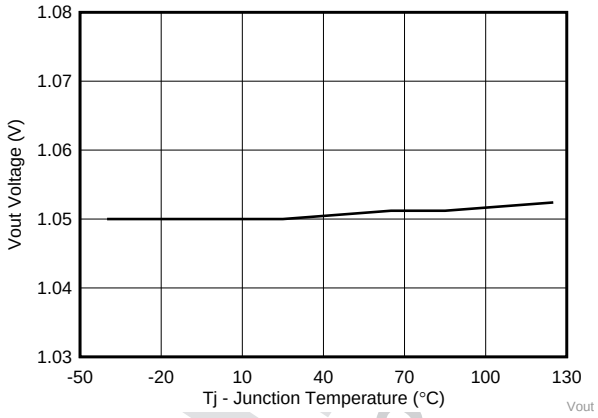


Figure 2. VOUT Voltage vs Temperature

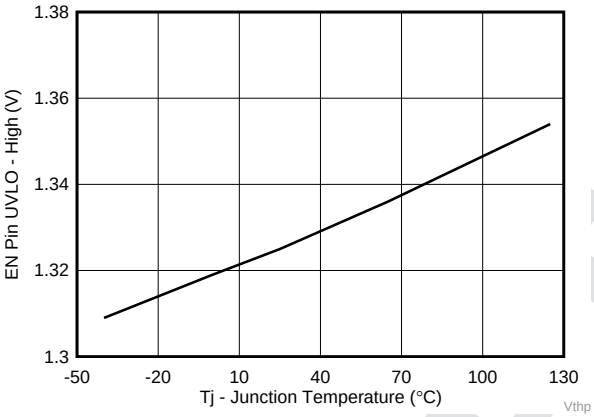


Figure 3. Enable On Voltage vs Temperature

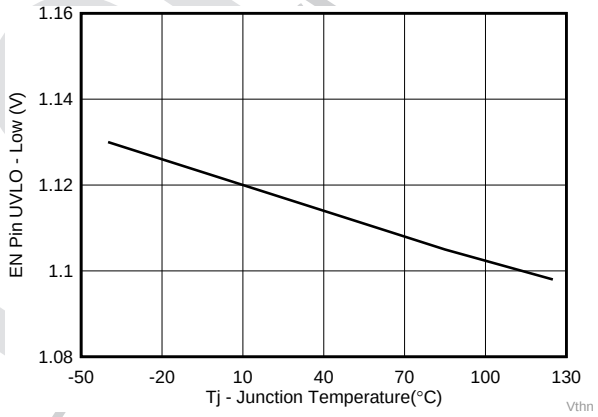


Figure 4. Enable Off Voltage vs Temperature

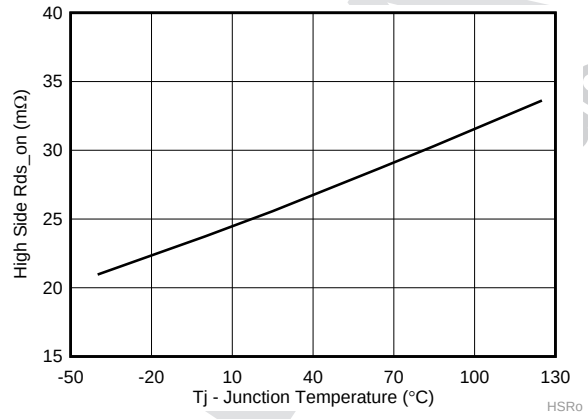


Figure 5. High-Side $R_{DS(on)}$ vs Temperature

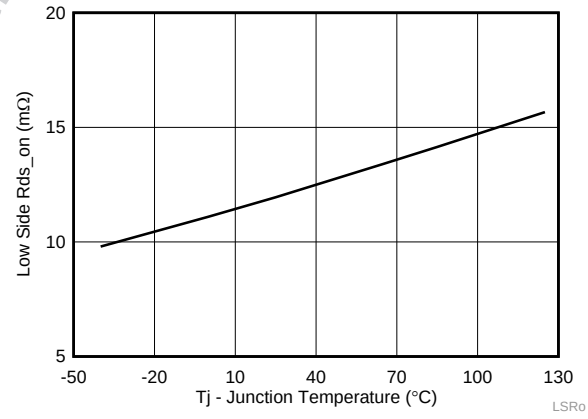


Figure 6. Low-Side $R_{DS(on)}$ vs Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

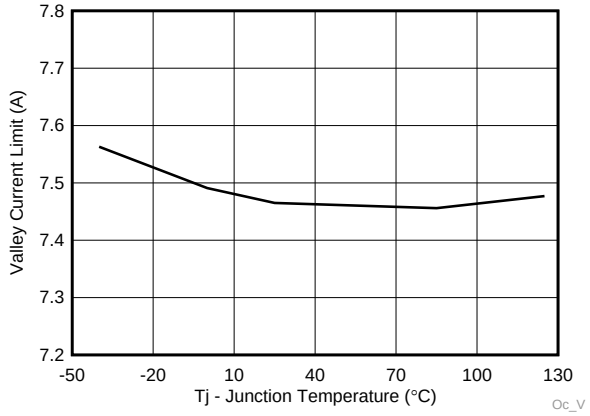


Figure 7. Valley Current Limit vs Temperature

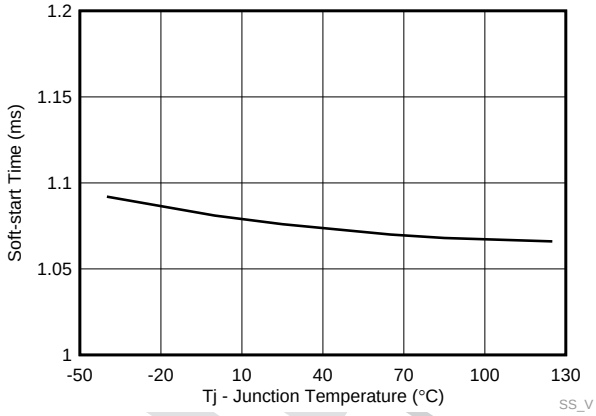


Figure 8. Soft-Start Time vs Temperature

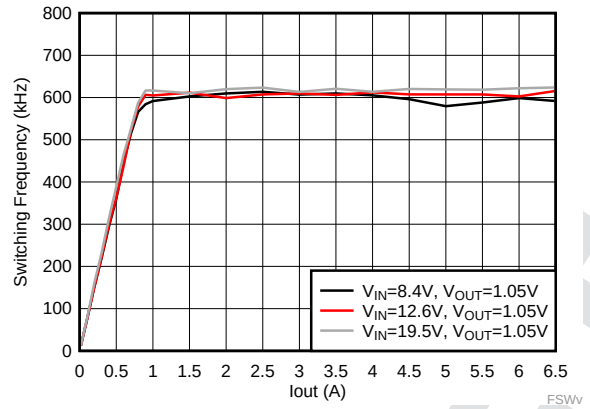


Figure 9. Switching Frequency vs Output Current

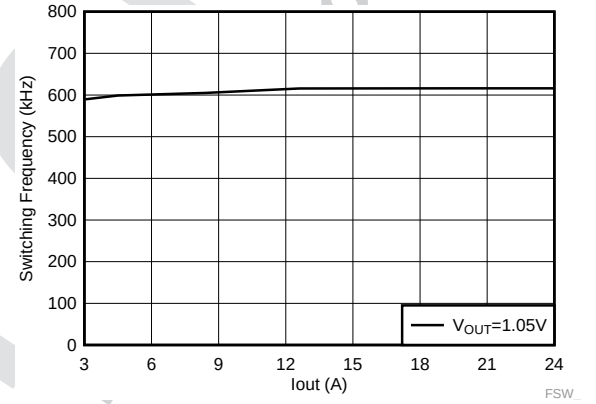


Figure 10. Switching Frequency vs Input Voltage

7 Detailed Description

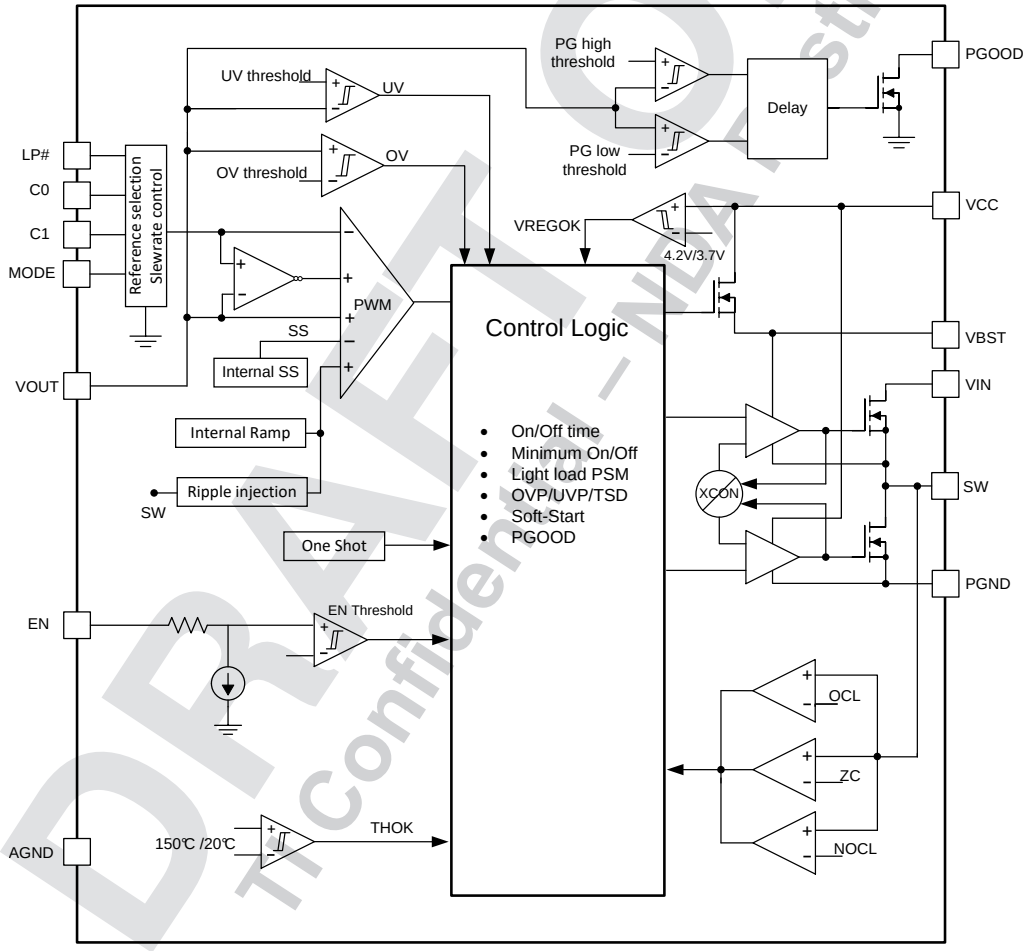
7.1 Overview

TPS51372 is a 6.5-A integrated FET synchronous step-down converter which can operate from 3 V to 24 V input voltage (V_{IN}). The proprietary D-CAP3™ mode enables low external component count, easy of design, optimization of the power rail for cost, size and efficiency. The key feature of this device is ultra-low quiescent current (ULQ™) mode to maintain high efficiency at light load. This feature is beneficial for long battery life in system standby mode. TPS51372 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The TPS51372 needs a external 5V supply to power the internal control circuitry. The undervoltage lockout (UVLO) circuit monitors the VCC pin voltage to protect the internal circuitry from low input voltages. The device has an internal pull-down current source to keep the EN pin low when its floating, so need external pull-up circuit to enable buck converter. TPS51372 is fixed 600kHz switching frequency and is built in 1.0ms internal soft-start time to simplify the design circuit and reduce the external components.

The TPS51372 supports 2-bits VID and Low Power Mode to dynamically change the Vout voltage to satisfy the IMVP8 applications— VCCIO, VPRIMCORE, V1.0A/EDRAM/EOPOP.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control

The main control loop of the buck is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3™ mode control. The DCAP3™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS51372 also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, VOUT, and is inversely proportional to the converter input voltage, VIN, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3™ control topology.

For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS51372 is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in Equation 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS51372. The low-frequency L-C double pole has a 180 degree drop in phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is related to the switching frequency. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency (F_{SW}).

7.3.2 Eco-Mode™ Control

The advanced Eco-mode™ control scheme to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The light load current where the transition to Eco-mode™ operation happens ($I_{OUT(LL)}$) can be calculated from Equation 2. Equation 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance (LOUT) so that the inductor peak-to-peak ripple current is approximately between 30% and 40% of the $I_{OUT(max)}$ (peak current in the application). It is also important to size the inductor properly so that the valley current does not hit the negative low-side current limit..

7.3.3 Enable and Shutdown

When the EN pin is set high, the device begins operation. The EN pin allows sequencing from a host or power good output of another device. When part is in shutdown mode, the internal power MOSFETs as well as the entire control circuitry are turned off. The output capacitor is smoothly discharged by a 40-Ω internal resistor through the VOUT pin. 2uA internal pulldown current is connected and maintains EN logic low, if the pin is floating.

Feature Description (continued)

7.3.4 Undervoltage Lockout

If the input voltage VCC drops, the under-voltage lockout prevents mis-operation of the device by switching off both power MOSFETs. The UVLO threshold is set to 3.7 V (typical). The device is operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter begins operation again when the input voltage exceeds the threshold by a hysteresis of 500 mV (typical).This is a non-latch protection.

7.3.5 Output Voltage Selection (VIDx and LP#)

As listed in Table 1, the output voltage of the TPS51372 is selected by two VIDx pins and one LP# pin. 2uA internal pulldown current is connected to the VIDx pins and LP# pin to ensure a proper logic level if the pin is high impedance or floating.

Table 1. TPS51372 Output Voltage Selection

VOLTAGE RAILS	MODE	LP# LOGIC	C1	C0	VOUT(V)
VCCIO	0	0	X	X	0
		1	0	0	0.85
		1	0	1	0.875
		1	1	0	0.95
		1	1	1	0.975
V1.0A/EDRAM/EOPOP	100K	0	X	X	0
		1	0	0	0.80
		1	0	1	0.95
		1	1	0	1.00
		1	1	1	1.05
Others (Fixed design only, LP,C0,C1 are not allowed to change on the fly)	150K	0	X	X	1.10
		1	0	0	1.20
		1	0	1	1.50
		1	1	0	1.80
		1	1	1	1.35
PRIM_CORE	200K above or floating	0	X	X	0.70
		1	0	0	0.85
		1	0	1	0.90
		1	1	0	0.95
		1	1	1	1.00

7.3.6 Power Good

The Power Good (PGOOD) pin is an open drain output. Once the VOUT pin voltage is between 95% and 110% of the internal reference voltage (VREF) the PGOOD is de-asserted and floats after a 160us de-glitch time. A pull-up resistor of 100 kΩ is recommended to pull it up to VCC. The PGOOD pin is pulled low when the VOUT pin voltage is lower than V_{UVP} or greater than V_{OVP} threshold or in an event of thermal shutdown or during the soft-start period. PGOOD error(from high to low) deglitch time is 32us.

Table 2 lists the PG logic status in different operation conditions. The PG pin can be left floating if not used. In low power mode, the PG signal is latched as high impedance. When the device exits low power mode, the PG has a 160µs blanking time to ensure that the output voltage returns to the nominal value.

Table 2. TPS51372 Power Good Pin Status

Condition		PG Logic	
		High	Low
Enable	EN=high, LP#=high, 0.95*Vout_set<Vout<1.05*Vout_set	√	
	EN=high, LP#=high, Vout<0.9*Vout_set or Vout>1.05*Vout_set		√
LP#	EN=high, LP#=low, Vout_set=0	√	
	EN=high, LP#=low, Vout_set≠0, 0.95*Vout_set<Vout<1.05*Vout_set	√	
	EN=high, LP#=low, Vout_set≠0, Vout<0.9*Vout_set or Vout>1.05Vout_set		√
Shutdown	EN=low		√
Thermal shutdown			√
UVLO	V_{VCC}<V_{UVLO}		√

7.3.7 Low Power Mode

The device has a low power mode(LPM) where the output voltage is reduced or disabled by using the LP# pin. For VCCIO application, shown in Figure 11, once LP# is set to low, TPS51372 will stop switching and decay to 0V, and PG output remains high during Vout transition and in low power mode condition. For Vprimcore and V1.0A/EDRAM/EOPOP, shown in Figure 12, once LP# is set to low, TPS51372 will stop switching and decay to target Vout, and will resume switching if Vout is lower than target. PG output remains high during Vout transition. Once LP# pin set to high, the VOUT will ramp up to certain voltage within the specific time shown in Table 3.

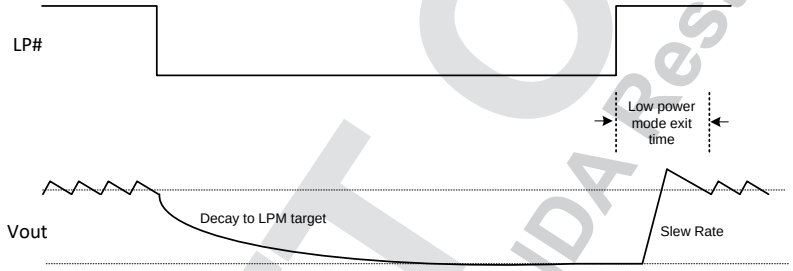


Figure 11. VCCIO Low Power Mode Enter and Exit Timing

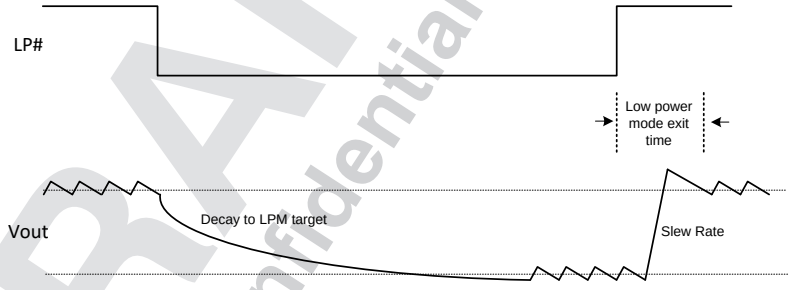


Figure 12. PRIMCORE and V1.0A/EDRAM/EOPOP Low Power Mode Enter and Exit Timing

Table 3. TPS51372 Low Power Mode Exit Time

	TPS51372		
	PRIMCORE	VCCIO	V1.0A/EDRAM/EOPOP
LPM Target(V)	0.70	0	0
Low Power Mode Enter	Decay	Decay	Decay
Low Power Mode Exit Time(µs)	30	100	100
PG status in Low Power Mode	Depends on Vout	High	High

7.3.8 Overcurrent Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage , output voltage, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current IOUT. If the measured drain to source voltage of the low-side FET is above the voltage proportional to current limit, the low side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it and shuts down the device after a wait time of 256us. In this type of valley detect control the load current is higher than the OCL threshold by one half of the peak to peak inductor ripple current. This protection is latch function, fault latching can be re-set by EN going low or VCC power cycling.

7.3.9 MODE Pin Configuration

By connecting different resistor from MODE to GND, TPS51372 is configured to support different power rails in IMVP8 applications, shown in Table 4, including VCCIO, PRIMCORE, V1.0A/EDRAM/EOPOP.

Table 4. TPS51371 Output Voltage Selection

MODE Resistor to GND	TPS51372
0	VCCIO
100k	V1.0A/EDRAM/EOPOP
150k	Others
200K above or floating	PRIMCORE

7.3.10 Over Voltage Protection

TPS51372 detects overvoltage and undervoltage conditions by monitoring the feedback VOUT voltage. When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and both the high-side MOSFET driver and the low-side MOSFET driver is turned off, will open discharge resistor to discharge output when OVP is enabled. This function is a latching operation, so need to reset by EN going low or VCC power cycling.

7.3.11 Output Voltage Discharge

The device has a 40-Ω discharge switch that discharges the V_{OUT} through VOUT pin during any event of fault like output overvoltage, output undervoltage , thermal shutdown , VCC voltage below the UVLO and the EN pin voltage (V_{EN}) below the turn-on threshold.

7.3.12 Thermal Shutdown

The device monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SDN} typically 150°C) the device shuts off. This is a non-latch protection. The device re-starts switching when the temperature goes below the thermal shutdown recovery threshold.

7.4 Device Functional Modes

7.4.1 Light Load Operation

When the TPS51372 is in the normal DCM operating mode and the switch current falls to 0 A, the TPS51372 begin operating in pulse skipping Eco-Mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VOUT voltage falls below the Eco-Mode threshold voltage. As the output current decreases, the perceived time between switching pulses increases. The Eco-Mode™ maintains higher efficiency at light load with a lower switching frequency.

7.4.2 Standby Operation

The TPS51372 can be placed in standby mode by pulling the LP# pin low. The device operates with a 65uA current in standby condition.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The schematic of Figure 13 shows a typical application schematic for TPS51372. This design converts an input voltage range of 3 V to 24 V down to 1.05 V with a maximum output current of 6.5 A.

8.2 Typical Application

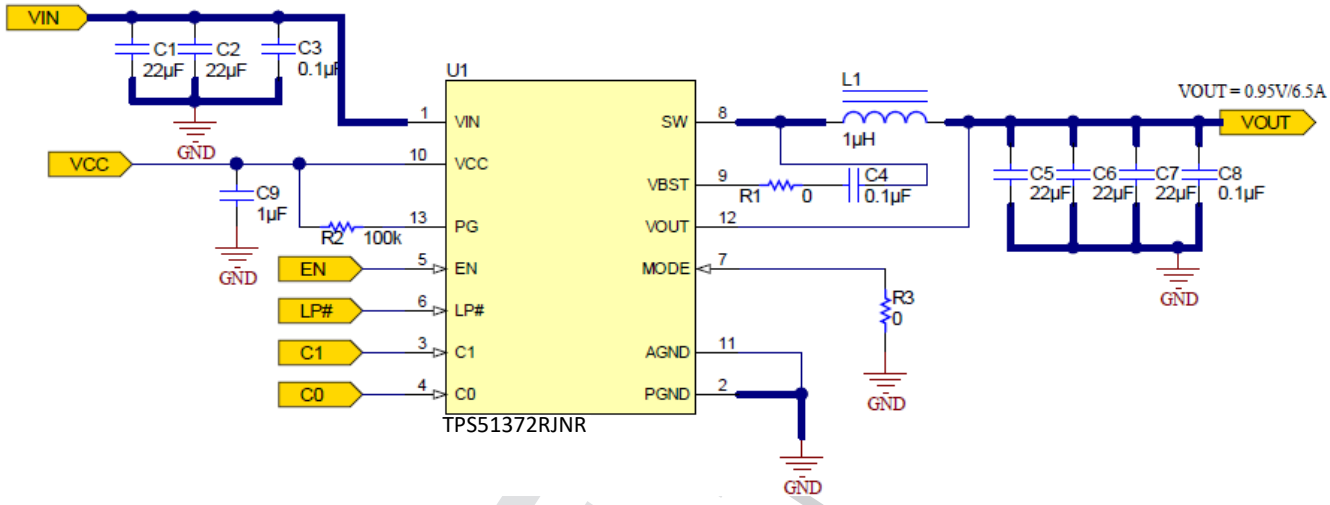


Figure 13. fApplication Schematic

8.2.1 Design Requirements

Table 5. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			0.95		V
I_{OUT}	Output current			6.5		A
ΔV_{OUT}	Transient response	4.5-A load step		±50		mV
V_{IN}	Input voltage		3	19	24	V
$V_{OUT(ripple)}$	Output voltage ripple			35		$mV_{(P-P)}$
	Start input voltage	Input voltage rising		Internal UVLO		V
	Stop input voltage	Input voltage falling		Internal UVLO		V
F_{SW}	Switching frequency			600		kHz
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See Table 6 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using Equation 3 and Equation 4. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{\left(I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT} \right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right)^2 \right)} \quad (3)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (4)$$

During transient/short circuit conditions the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.2 Output Capacitor Selection

After selecting the inductor the output capacitor needs to be optimized. In DCAP3, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in Table 6

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$

Table 6. Recommended Component Values

V_{OUT} (V)	F_{sw} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)
1.05	600	1.0	44	250
	600	0.68	66	250

8.2.2.1.3 Input Capacitor Selection

The minimum input capacitance required is given in Equation 5.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (5)$$

TI recommends using a high quality X5R or X7R input decoupling capacitors of 22 µF on the input voltage pin. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 6 below:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT} \right)}{V_{IN(min)}}} \quad (6)$$

8.2.3 Application Curves

Figure 14 through Figure 31 apply to the circuit of Figure 13. V_{IN} = 19 V. T_a = 25 °C unless otherwise specified.

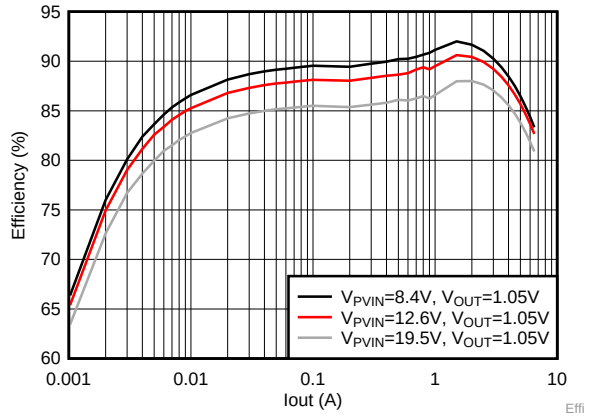


Figure 14. Efficiency Curve, V_{OUT} = 1.05 V

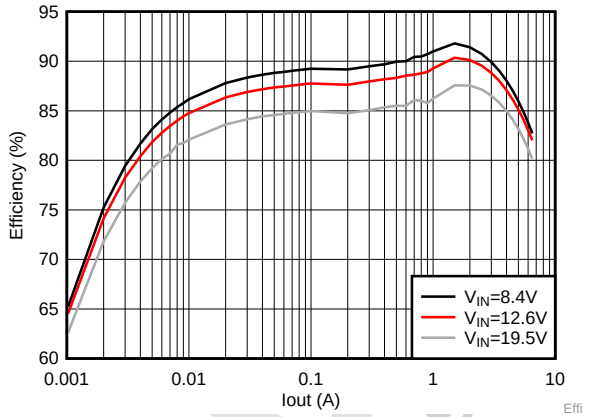


Figure 15. Efficiency Curve, V_{OUT} = 1.0 V

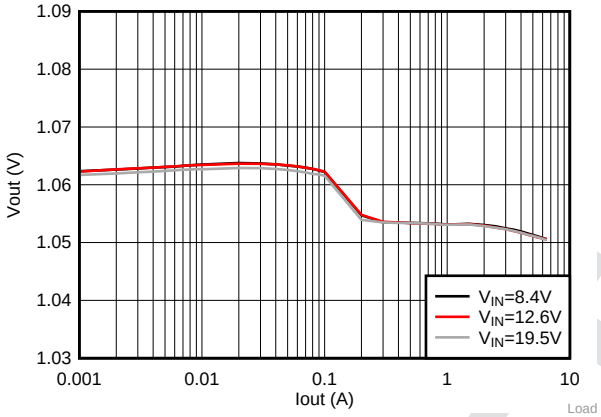


Figure 16. Load Regulation, V_{OUT} = 1.05 V

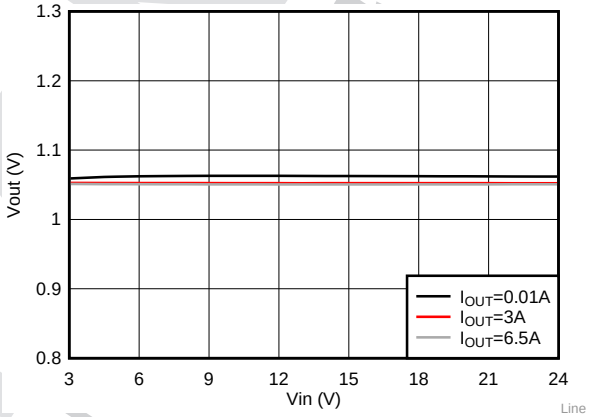


Figure 17. Line Regulation, V_{OUT} = 1.05 V

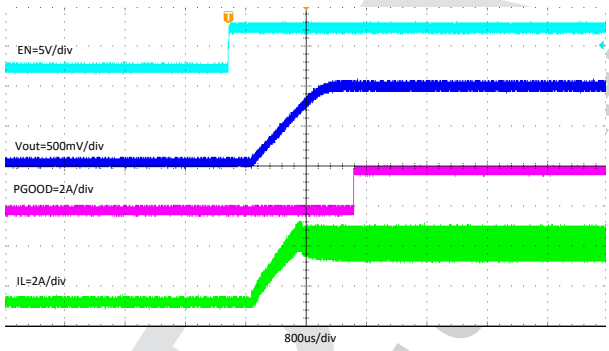


Figure 18. Start up Relative to EN Rising

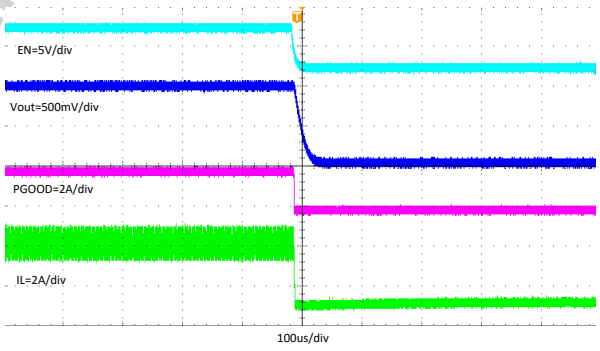


Figure 19. Shut Down Relative to EN Falling

ADVANCE INFORMATION

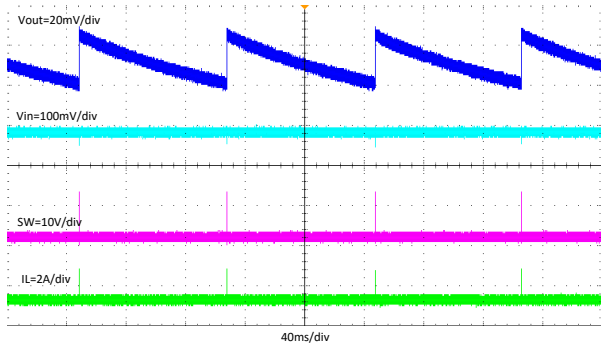


Figure 20. Output Voltage Ripple, I_{OUT} =0 A

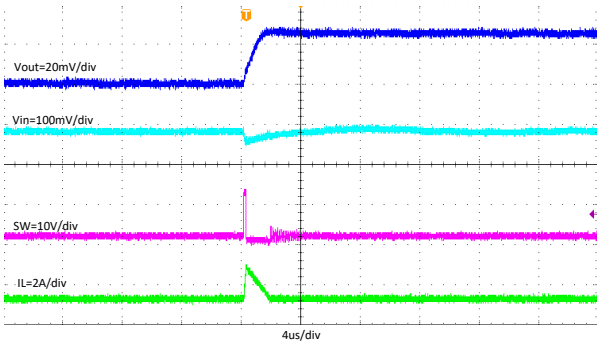


Figure 21. Output Voltage Ripple Zoom In, I_{OUT} =0 A

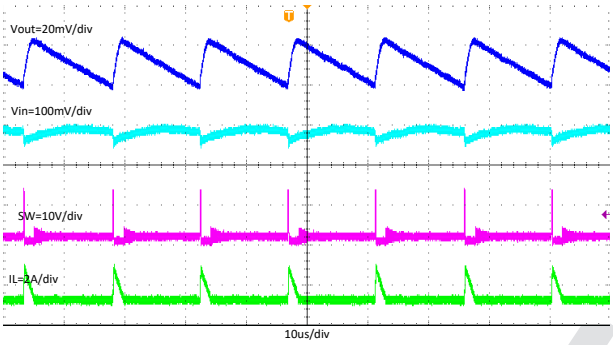


Figure 22. Output Voltage Ripple, I_{OUT} = 0.1 A

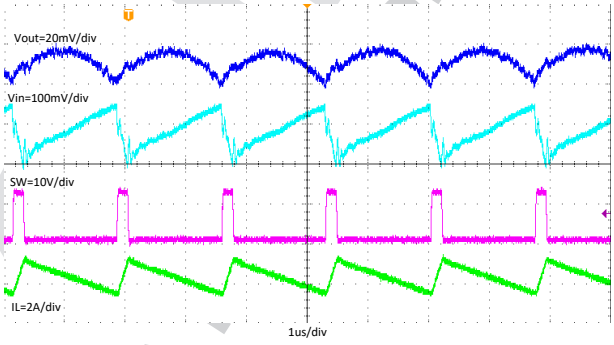


Figure 23. Output Voltage Ripple, I_{OUT} = 6.5 A

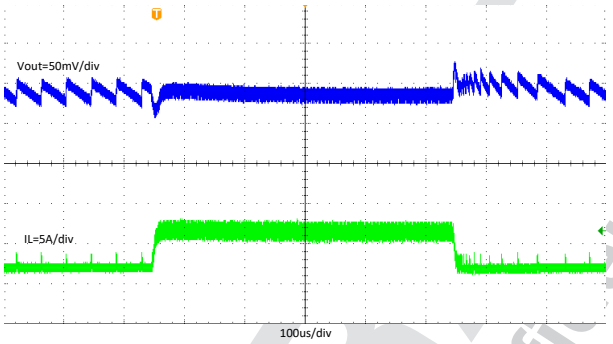


Figure 24. Transient Response, 10 mA to 4.5A with 2.5A/us SR

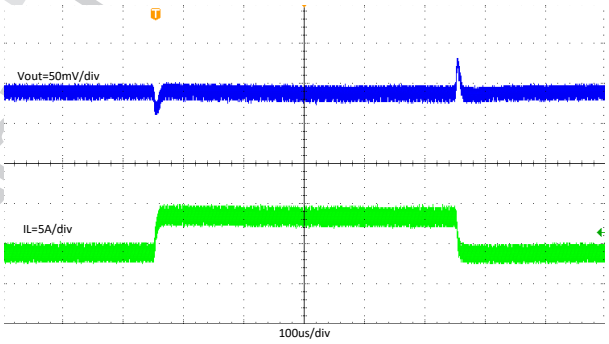


Figure 25. Transient Response, 2A to 6.5A with 2.5A/us SR

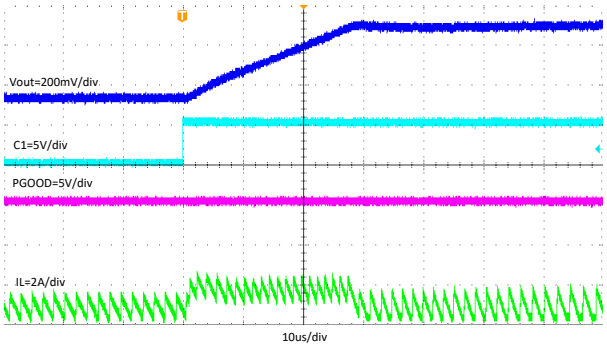


Figure 26. Low Power Mode Exit, V_{OUT}= 0.7V to 1.05V

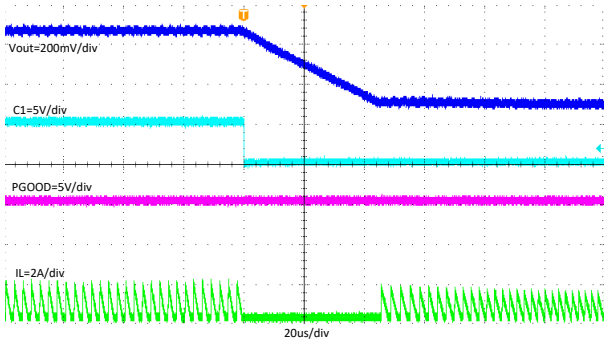


Figure 27. Low Power Mode Enter, V_{OUT}= 1.05V to 0.7V

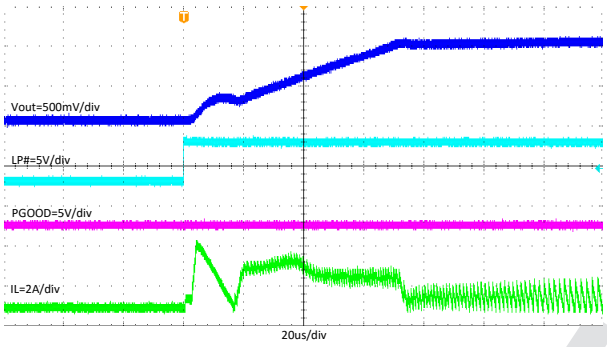


Figure 28. Low Power Mode Exit, V_{OUT} = 0V to 0.975V

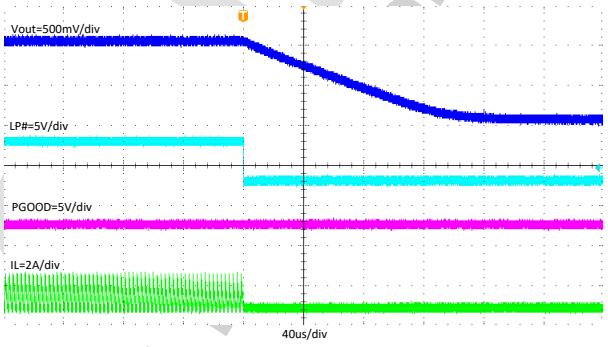


Figure 29. Low Power Mode Enter, V_{OUT} = 0.975V to 0V

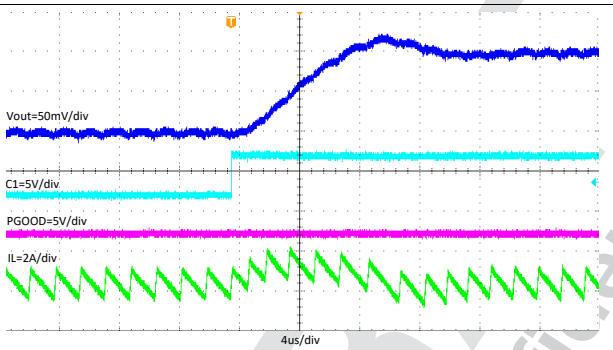


Figure 30. VID Transition, V_{OUT} = 0.95V to 1.05V

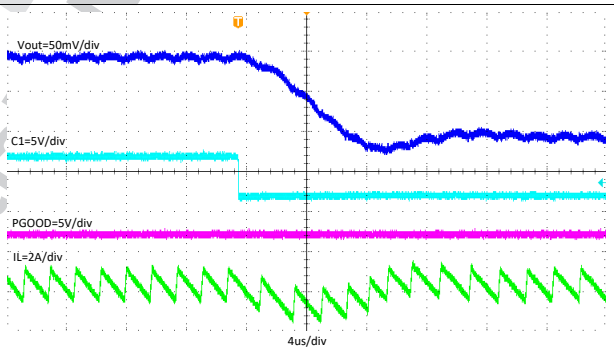


Figure 31. VID Transition, V_{OUT} = 1.05V to 0.95V

ADVANCE INFORMATION

9 Power Supply Recommendations

The TPS51372 is intended to be powered by a well regulated dc voltage. The input voltage range is 3 to 24 V. TPS51372 is buck converters, the input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS51372 circuit, some additional input bulk capacitance is recommended. Typical value is from 22 µF to 44 µF.

VIN is the power input for buck, VCC is power supply for internal control logic. Below lists the power on sequence scenarios.

- EN is high before VIN has the power input, VCC power supply must be provided after or same time with VIN, otherwise the output will be latched, this latch can be recovered by toggling the EN pin or re-power the VCC.
- EN is low before VIN and VCC has the power input, then there is no power supply input sequence requirement.

10 Layout

10.1 Layout Guidelines

- Recommend a four-layer PCB for good thermal performance and with maximum ground plane. 3" x 3", four-layer PCB with 2-oz. copper used as example.
- Recommend having two caps on VIN side of the IC. Place them right across VIN as close as possible.
- Inner layer 1 will be ground with the PGND to AGND net tie
- Inner layer2 has VIN copper pour that has vias to the top layer VIN. **Place multiple vias under the device near VIN and PGND and near input capacitors** to reduce parasitic inductance and improve thermal performance
- Bottom later is GND with the SW trace routing.
- VIN trace must be wide to reduce the trace impedance.

10.2 Layout Example

Figure 32 shows the recommended top side layout. Component reference designators are the same as the circuit shown in Figure 13.

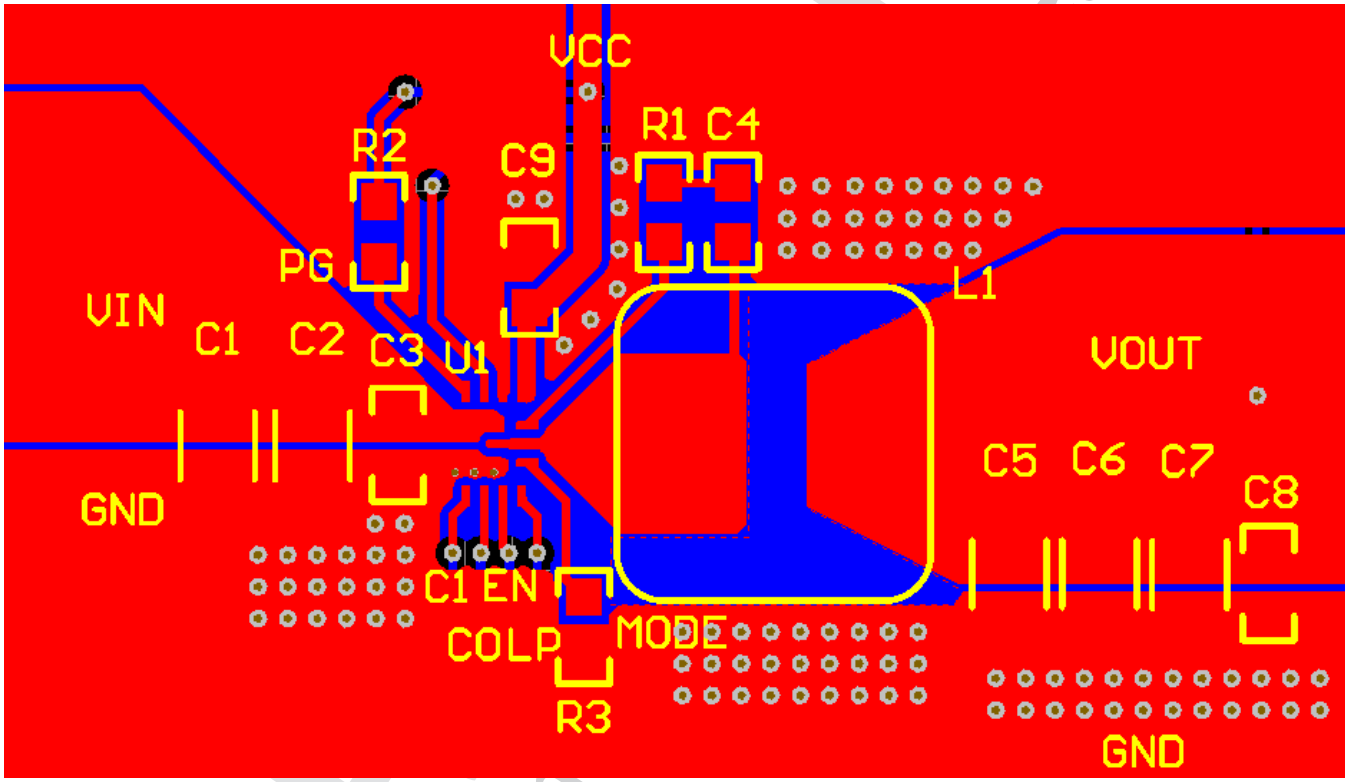


Figure 32. Top Side Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

D-CAP3, HotRod, Eco-Mode, E2E are trademarks of Texas Instruments.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
TPS51372RJNR	PREVIEW	VQFN	RJN	13	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 Year	–40 to 125	51371
TPS51372RJNT	PREVIEW	VQFN	RJN	13	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 Year	–40 to 125	51371

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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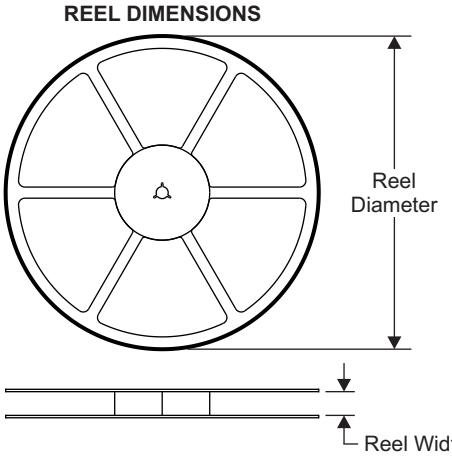
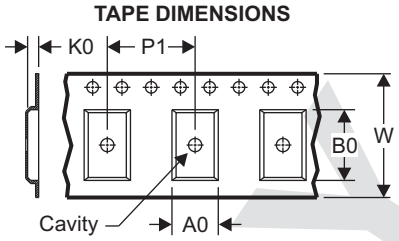
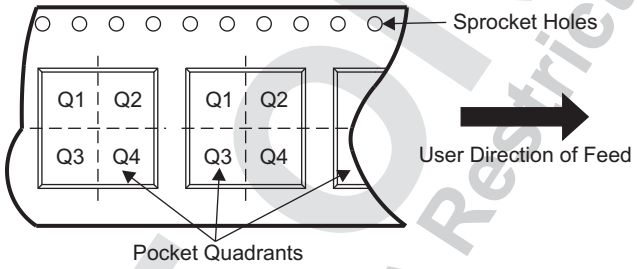
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

12.1.2 Tape and Reel Information



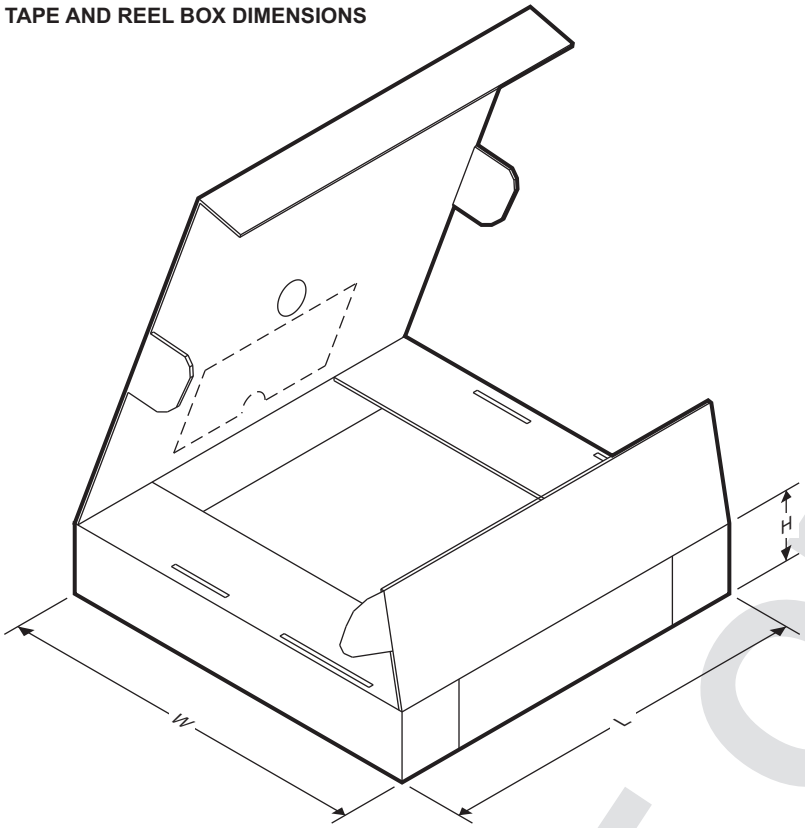


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51372RJNR	VQFN	RJN	13	3000								
TPS51372RJNT	VQFN	RJN	13	250								

TAPE AND REEL BOX DIMENSIONS



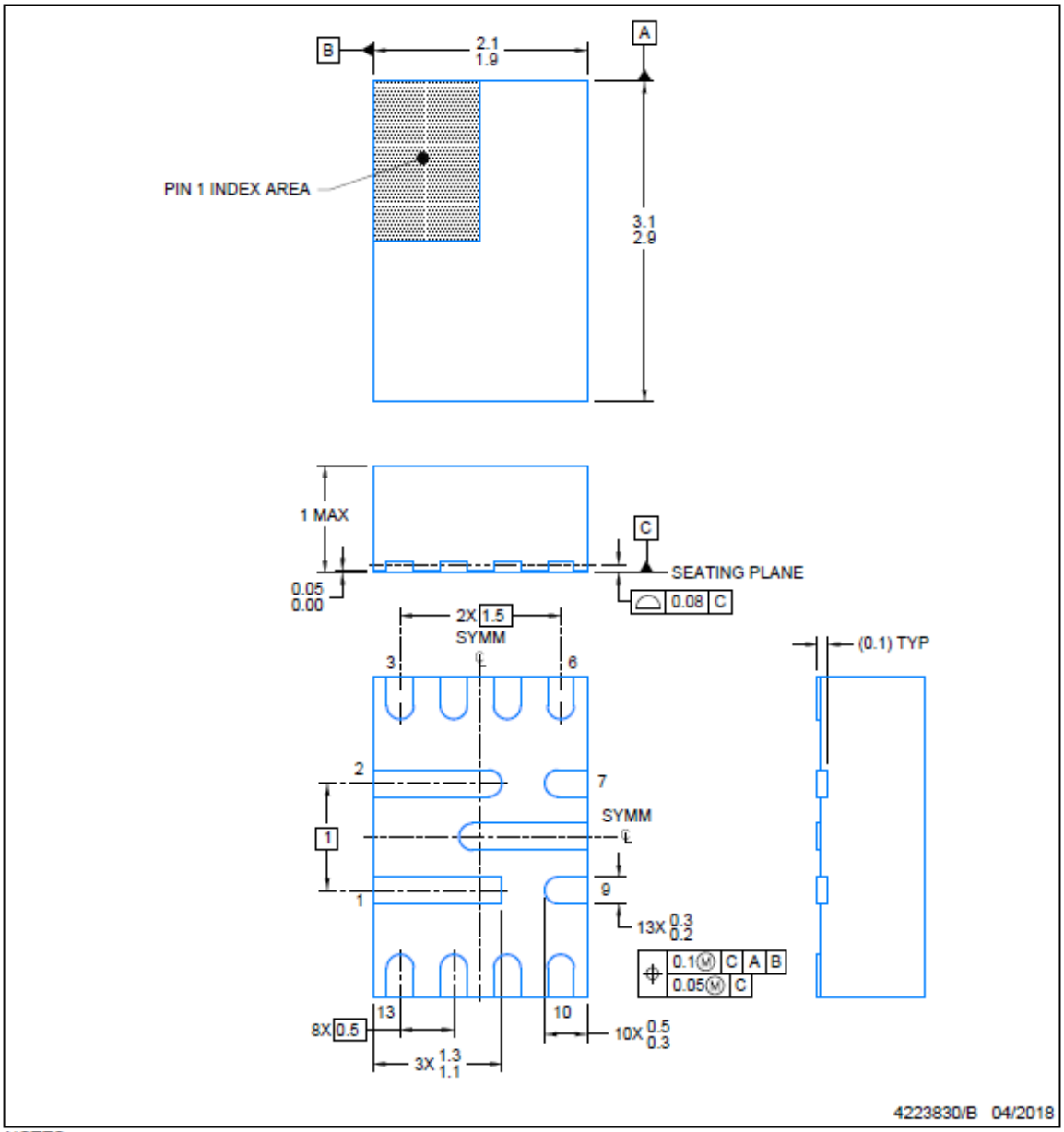
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51372RJNR	VQFN	RJN	13	3000	367	367	35
TPS51372RJNT	VQFN	RJN	13	250	367	367	35

ADVANCE INFORMATION

PACKAGE OUTLINE

RJN0013A — **VSON-HR - 1 mm max height**

PLASTIC SMALL OUTLINE- NO LEAD



NOTES:

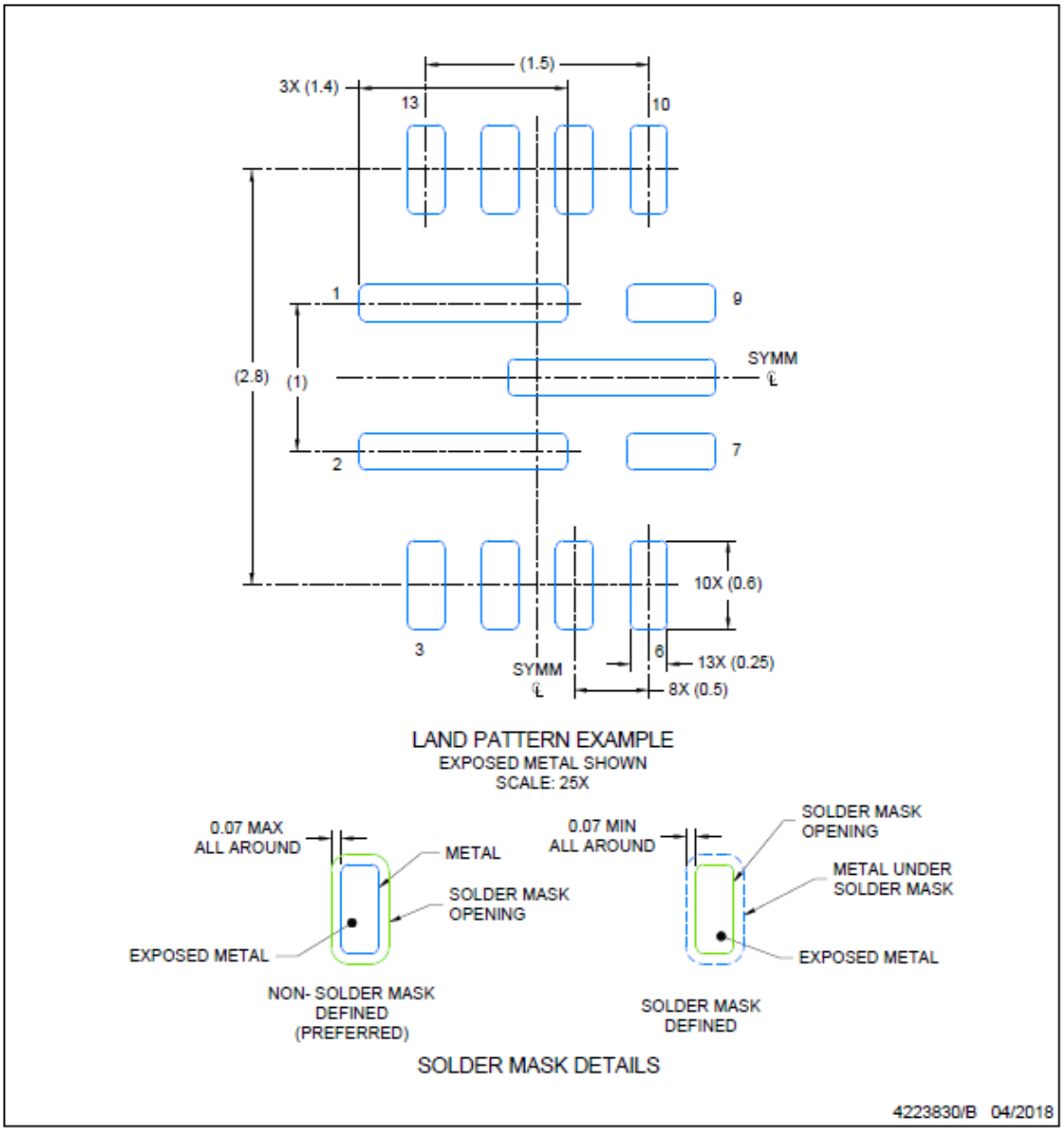
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RJN0013A

VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE- NO LEAD



NOTES: (continued)

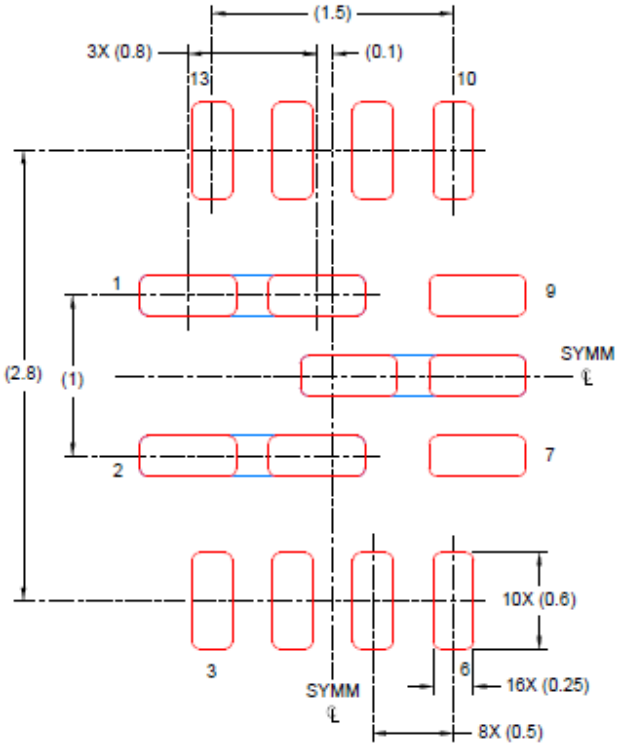
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RJN0013A — **VSON-HR - 1 mm max height**

PLASTIC SMALL OUTLINE- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
86% PRINTED COVERAGE BY AREA
SCALE: 25X

4223830/B 04/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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