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1-kW/36-V Power Stage for Brushless Motor in Battery Powered Garden and Power Tools

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Design Resources

TIDA-00285	Tool Folder Containing Design Files
CSD18540Q5B	Product Folder
DRV8303	Product Folder
TPS54061	Product Folder
OPA2374	Product Folder
TPD4S009	Product Folder
LMT84	Product Folder
TMS320F28027F	Product Folder
LAUNCHXL-F28027F	Tool Folder

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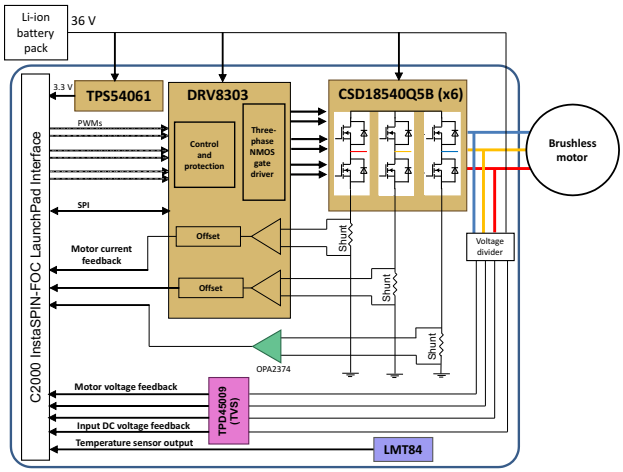
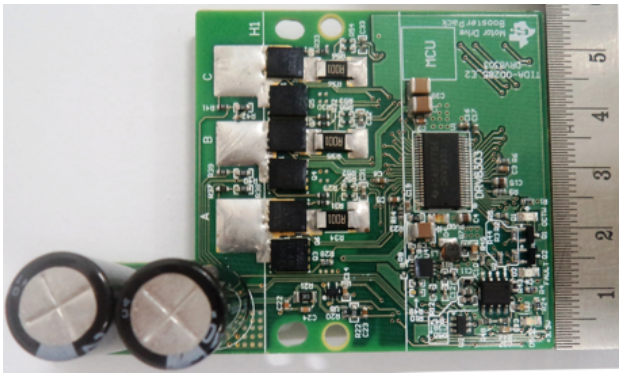
Featured Applications

- Power Tools
- Garden Tools
- Lawn Mover Robots
- Vacuum Cleaning Robots

Design Features

- 1-kW Power Stage With Field Oriented Control for Permanent Magnet Synchronous Motors
- Designed to Operate from 10-Cell Li-Ion Battery Voltage Ranging from 30 to 42 V
- Delivers up to 30-A_{RMS} Continuous Motor Current With an Airflow of 400 LFM
- Small PCB Form Factor of 57 × 59 mm Using 60-V/400-A_{PEAK}, 1.8-mΩ R_{DS_ON}, SON5x6 Package MOSFETs for Power Stage
- Uses DRV8303 Three-Phase Gate Driver, Which Can Operate from 6 to 60-V Input, Supporting Programmable Gate Current With Maximum Setting of 2.3-A Sink / 1.7-A Source
- Overcurrent Protection Configurable for Cycle-by-Cycle Control or Latch Shutdown
- Sense Feedback of Individual Phase Voltage, DC Bus Voltage, and Low-Side Current on Each Phase for Sensorless Control
- Can Support Brushless DC Motor Control Using Trapezoidal Method
- 3.3-V/0.15-A Step-Down Buck Converter for Powering MCU
- Designed to Operate at an Ambient Temperature of –20°C to 55°C





1 Introduction

This reference design is a power stage for brushless motors in battery-powered garden and power tools rated up to 1 kW. The power stage operates from a 10-cell lithium-ion battery with a voltage range from 36 to 42 V. The design uses CSD18540Q5B NexFETs featuring a very low drain-to-source resistance (R_{DS_ON}) of 1.8 mΩ in a SON5x6 SMD package, which results in a very small form factor of 57 × 59 mm. The three-phase gate-driver DRV8303 is used to drive the three-phase MOSFET bridge, which can operate from 6 to 60 V and support programmable gate current with maximum setting of 2.3-A sink / 1.7-A source. The power stage can be configured for a single-shunt or three-shunt current sensing. The design supports sensorless control for brushless DC (BLDC) and permanent magnet synchronous motors (PMSM) using trapezoidal control or field oriented control (FOC). The C2000™ Piccolo™ LaunchPad™ is used with the power stage to implement InstaSPIN™-FOC using the motor current and voltage feedback. The corresponding test report evaluates the thermal performance of the board and overcurrent protection features such as cycle-by-cycle control and latch control of the DRV8303.

Power tools are used in various industrial and household applications such as drilling, grinding, cutting, polishing, driving fasteners, various garden tools, and so on. The most common types of power tools use electric motors while some use internal combustion engines, steam engines, or compressed air.

Power tools can be either corded or cordless (battery-powered). Corded power tools use the mains power (the grid power) to power up the AC or DC motors. The cordless tools use battery power to drive DC motors. Most of the cordless tools use lithium-ion batteries, the most advanced in the industry. Lithium-ion batteries have high energy density, low weight, and greater life. These batteries have relatively low self-discharge (less than half that of nickel-based batteries) and can provide a very high current for applications like power tools. Cordless tools use brushed or BLDC motors. The brushless motors are more efficient and have less maintenance, low noise, and longer life.

Power tools have requirements on form factor and thermal performance. Therefore, high-efficient power stages with a compact size are required to drive the power tool motor. Small form factor of the power stage enables design flexibility for optimal cooling method and placement of the power stage close to the battery pack to minimize impedance on connections carrying high current. High efficiency provides maximum battery duration and reduces cooling efforts. High efficiency requirement in turn asks for switching devices with low R_{DS_ON}. The power stage should also take care of protections like motor stall or any other chance of high current.

The objective of this reference design is to provide a 1-kW/36-V power stage for brushless motors used in battery powered applications (like power tools, garden tools, and so on). This design demonstrates the power stage in a small form factor (57 × 59 mm) operating from a 36-V DC input (using a 10-cell Li-ion battery) and delivers up to 30-A_{RMS} continuous current output to motor. The design also provides scalability for lower voltage and current levels. At higher power levels, the cooling is provided by forced air, which allows for the small form factor.

2 Key System Specifications

Table 1. Key System Specifications of Power Stage

PARAMETER	SPECIFICATION
DC input voltage	36-V nominal (42-V maximum)
Maximum input DC current	30 A with 400 LFM airflow
Rated power capacity	1 kW
Inverter switching frequency	60 kHz
Operating ambient temperature	–20°C to 55°C
Inverter efficiency	≥ 97% (theoretical) at rated load
Power supply specification for MCU	3.3 V ±5%
Feedbacks	Three winding voltages, three winding currents (inverter leg currents), and input DC voltage
Protections	Overcurrent (cycle-by-cycle/latch), over temperature, input undervoltage
PCB	57 × 59 mm / 4-Layer, 2-Oz copper

3 System Description

Compared to their brushed motor counterpart, permanent magnet brushless motors are gaining importance because of their high efficiency, low maintenance, high reliability, low rotor inertia, low noise, and so on. A brushless PMSM has a wound stator and a permanent magnet rotor assembly. These motors generally use internal or external devices to sense rotor position. The sensing devices provide logic signals for electronically switching the stator windings in the proper sequence to maintain rotation of the magnet assembly. The sensor-based solution requires accurate mechanical assembly of sensors. The rotor position can also be estimated using sensorless algorithms implemented in microcontroller units (MCUs).

The electronic drive is required to control the stator currents in a brushless permanent magnet motor. The electronic drive consists of:

- A power stage with three-phase inverter having the required power capability
- MCU to implement the motor control algorithm
- Motor voltage and current sensing for sensorless control and closed loop speed or torque control
- Gate driver for driving the three-phase inverter
- Power supply to power up the MCU

3.1 Brushless Permanent Magnet Motors

Permanent magnet motors can be classified based on Back-EMF (BEMF) profiles: brushless direct current (BLDC) motor and permanent magnet synchronous motor (PMSM). Both BLDC motors and PMSMs have permanent magnets on the rotor but differ in the flux distributions and BEMF profiles. In a BLDC motor, the BEMF induced in the stator is trapezoidal, and in a PMSM, the BEMF induced in the stator is sinusoidal. Implementation of an appropriate control strategy is required to obtain the maximum performance from each type of motor.

3.1.1 Brushless DC Motor – Trapezoidal Control

The BLDC motor or the trapezoidal BEMF motor has the ampere conductor distribution of the stator, which ideally remains constant and fixed in space for a fixed interval known as the commutation interval. For a three-phase winding, the commutation interval is 60° electrical. At the end of each commutation interval, the ampere conductors are commutated to the next position. These motors use a two-phase ON control, where two phases of the motor will be energized at a time and the third winding will be open, The principle of the BLDC motor is, at all times, to energize the phase pair, which can produce the highest torque. The combination of a direct current with a trapezoidal BEMF makes it theoretically possible to produce a constant torque. In practice, the current cannot be established instantaneously in a motor phase as a consequence the torque ripple is present at each 60° phase commutation. Figure 1 describes the electrical wave forms in the BLDC motor in the two phases ON operation.

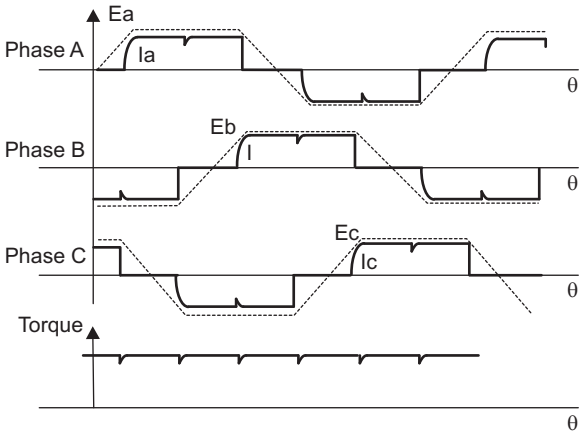


Figure 1. Electrical Waveforms in Two-Phase ON Control of BLDC Motor and Torque Ripple

A trapezoidal control has following advantages:

- Only one current at a time needs to be controlled
- Only one current sensor is necessary (or none for speed loop only)
- The positioning of the current sensor allows the use of low cost sensors as a shunt

For more details about trapezoidal control, see the application report *Sensorless Trapezoidal Control of BLDC Motors* (SPRABQ7)

3.1.2 PMSM – Field Oriented Control

The PMSM has a sinusoidal BEMF. The sinusoidal BEMF motor offers its best performances when driven by sinusoidal currents and constant torque will be produced. In sinusoidal current control, three phases of the motor are ON at the same time.

FOC is used to control the permanent magnet motor. FOC achieves better dynamic performance. The goal of the FOC (also called vector control) on the synchronous or asynchronous machine is to separately control the torque producing flux and magnetizing flux components. Several mathematical transforms are required to decouple the torque and magnetizing flux components of the stator current. The processing capability provided by the MCUs enables these mathematical transformations to be carried out very quickly. These transformations in turn imply that the entire algorithm controlling the motor can be executed at a fast rate, enabling a higher dynamic performance.

The FOC algorithm will enable real-time control of torque and rotation speed. As this control is accurate in every mode of operation (steady state and transient), no oversize of the power transistors is necessary. The transient currents are constantly controlled in amplitude. Moreover, no torque ripple appears when driving this sinusoidal BEMF motor with sinusoidal currents. The reference design uses InstaSPIN-FOC algorithm.

3.1.3 InstaSPIN-FOC

TI InstaSPIN-FOC technology enables designers to identify, tune, and fully control any type of three-phase, variable speed, sensorless, synchronous, or asynchronous motor control system. This new technology removes the need for a mechanical motor rotor sensor to reduce system costs and improve operation using TI's new software encoder (sensorless observer) software algorithm, FAST™ (flux, angle, speed, and torque), embedded in the read-only memory (ROM) of Piccolo devices. This ROM enables premium solutions that improve motor efficiency, performance, and reliability in all variable-speed and variable-torque applications. Figure 2 shows the block diagram of the InstaSPIN-FOC.

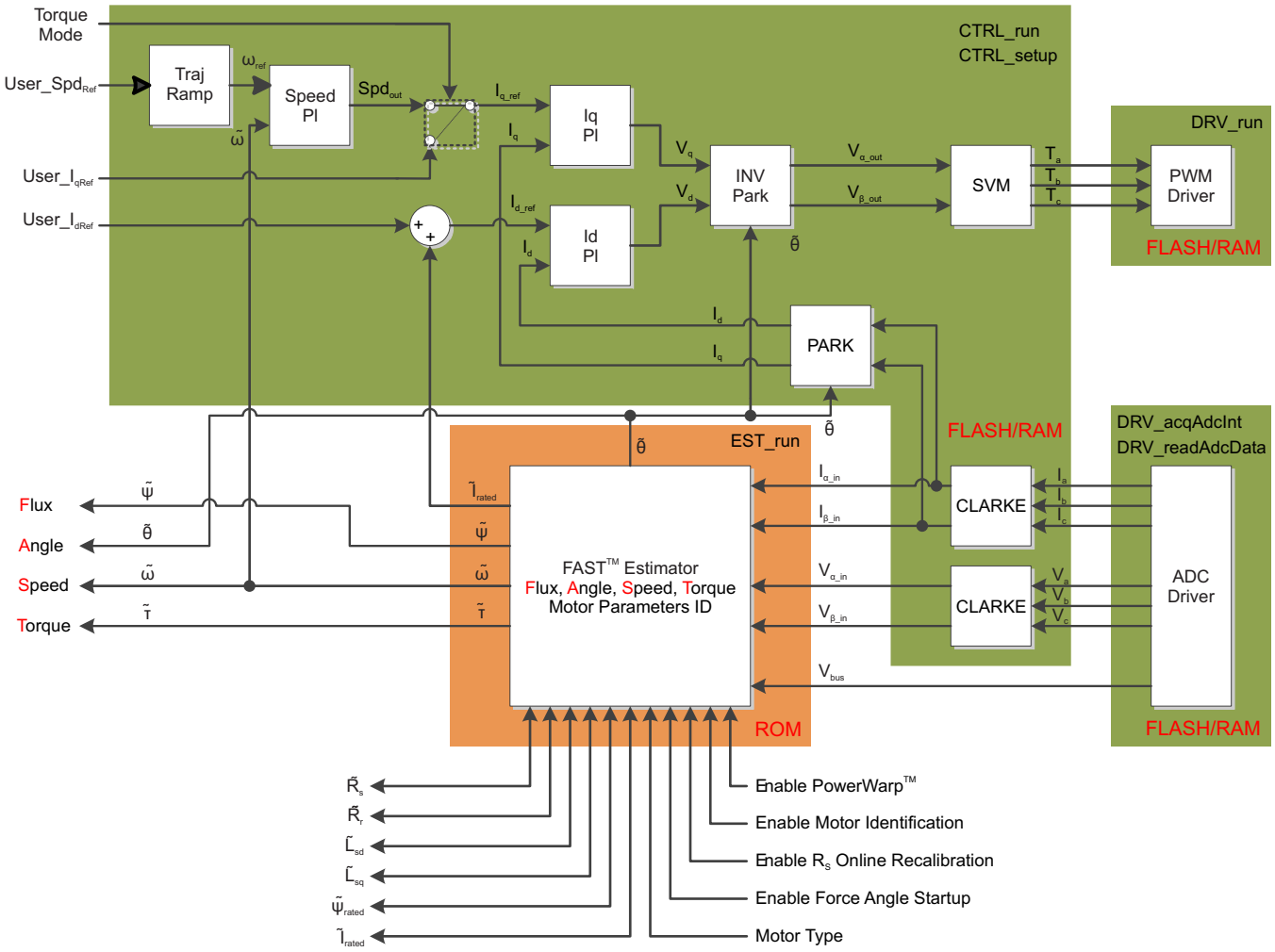


Figure 2. Block Diagram of InstaSPIN-FOC

InstaSPIN-FOC benefits:

- Includes FAST estimator to measure rotor flux magnitude, rotor flux angle, motor shaft speed and torque in a sensorless FOC system
- Automatic torque (current) loop tuning with option for user adjustments
- Automatic configuration of speed loop gains (Kp and Ki) provides stable operation for most applications and user adjustments required for optimum transient response
- Automatic or manual field weakening and field boosting
- Bus voltage compensation
- Automatic offset calibration insures quality samples of feedback signals

For more information on the InstaSPIN-FOC, see its technical reference manual (SPRUHP4).

3.2 Power Stage for the Motor Drive

The reference design provides a 1-kW/36-V power stage for brushless motor control in battery powered garden and power tools. The reference design uses the C2000 InstaSPIN-FOC-enabled LaunchPad as the MCU. The power stage is mounted as the booster pack. The sinusoidal voltage waveform applied to the motor is created by using the space vector modulation technique implemented in the LaunchPad MCU. Figure 3 shows the assembled power stage mounted with the LaunchPad.

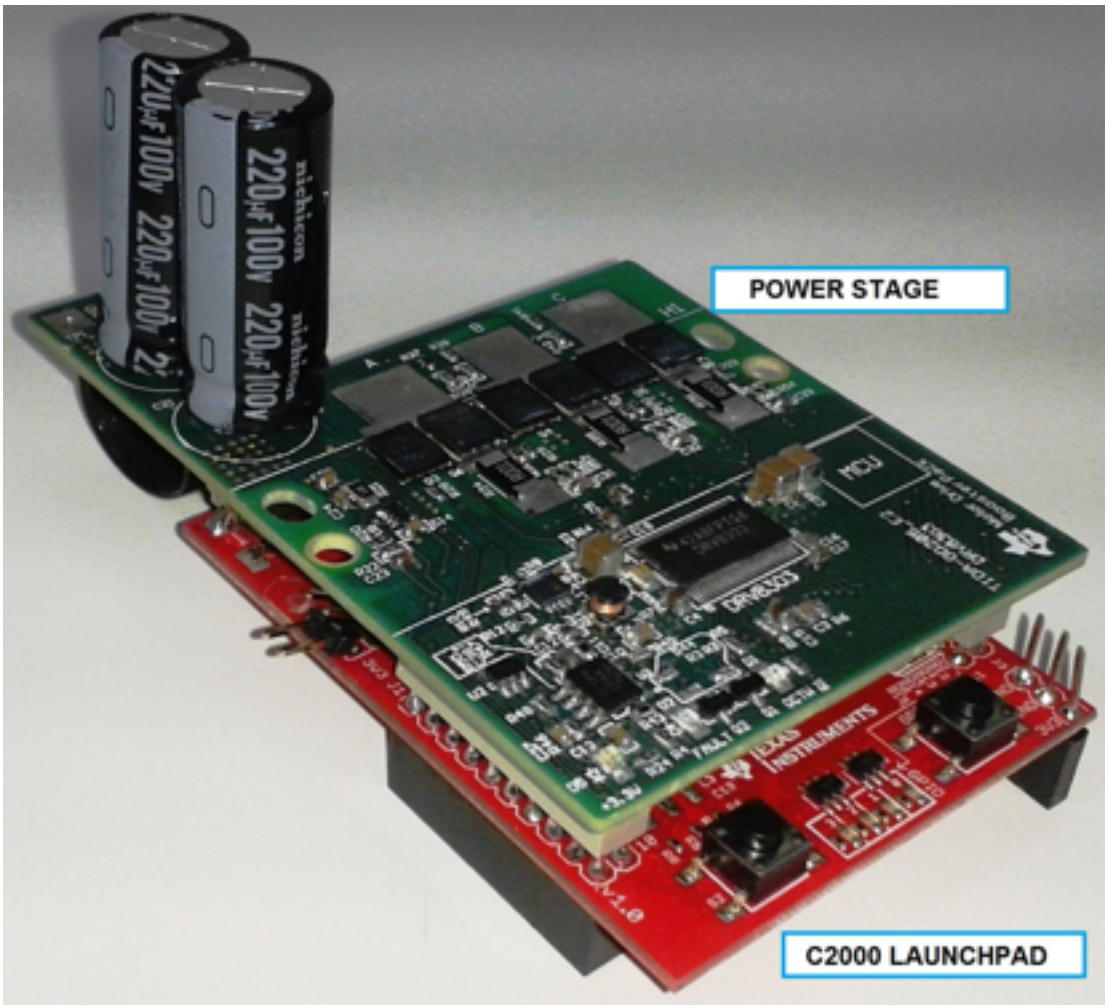


Figure 3. Assembled Power Stage Mounted With LaunchPad

The power stage is designed to operate from a 10-cell Li-ion battery. For a Li-ion battery, the maximum volt per cell is 4.2 V and nominal voltage is 3.6 V per cell. The power stage is designed to operate up to 42 V. The booster pack power stage consists of the high efficient, six miniature NexFET™ CSD18540Q5B to form the three-phase inverter bridge. The SON5x6 miniature package of the NexFET enables to make the power stage in a small form factor. The power stage is designed to handle the nominal power with a forced air cooling of 400 LFM. The low R_{DS_ON} of 1.8 mΩ of the FETs helps to reduce the power loss. which lessens heat dissipation in the FETs and makes the power stage thermally stable.

The FETs are driven by the three-phase gate driver DRV8303. The DRV8303 can operate from a 6-to 60-V power supply, which is suitable to work in the application voltage range. The DRV8303 has two internal current shunt amplifiers and provides overcurrent protection by sensing the drain-to-source voltage of the MOSFETs. These features make the DRV8303 apt for motor control. The different references and features of the DRV8303 can be configured through SPI programming. The DRV8303 driver has built-in overcurrent protection, shoot-through, and undervoltage protection.

The required voltage and current feedbacks are provided to support sensorless (trapezoidal control or FOC) operation. The 3.3-V power supply for the MCU is generated in the power stage board.

4 Block Diagram

Figure 4 depicts the block diagram of the power stage. The main parts of the power stage consists of the three-phase MOSFET bridge, the gate driver DRV8303, interface to C2000 MCU LaunchPad, 3.3-V step-down DC-DC converter, ESD protection, over temperature protection, and the sense feedback circuits.

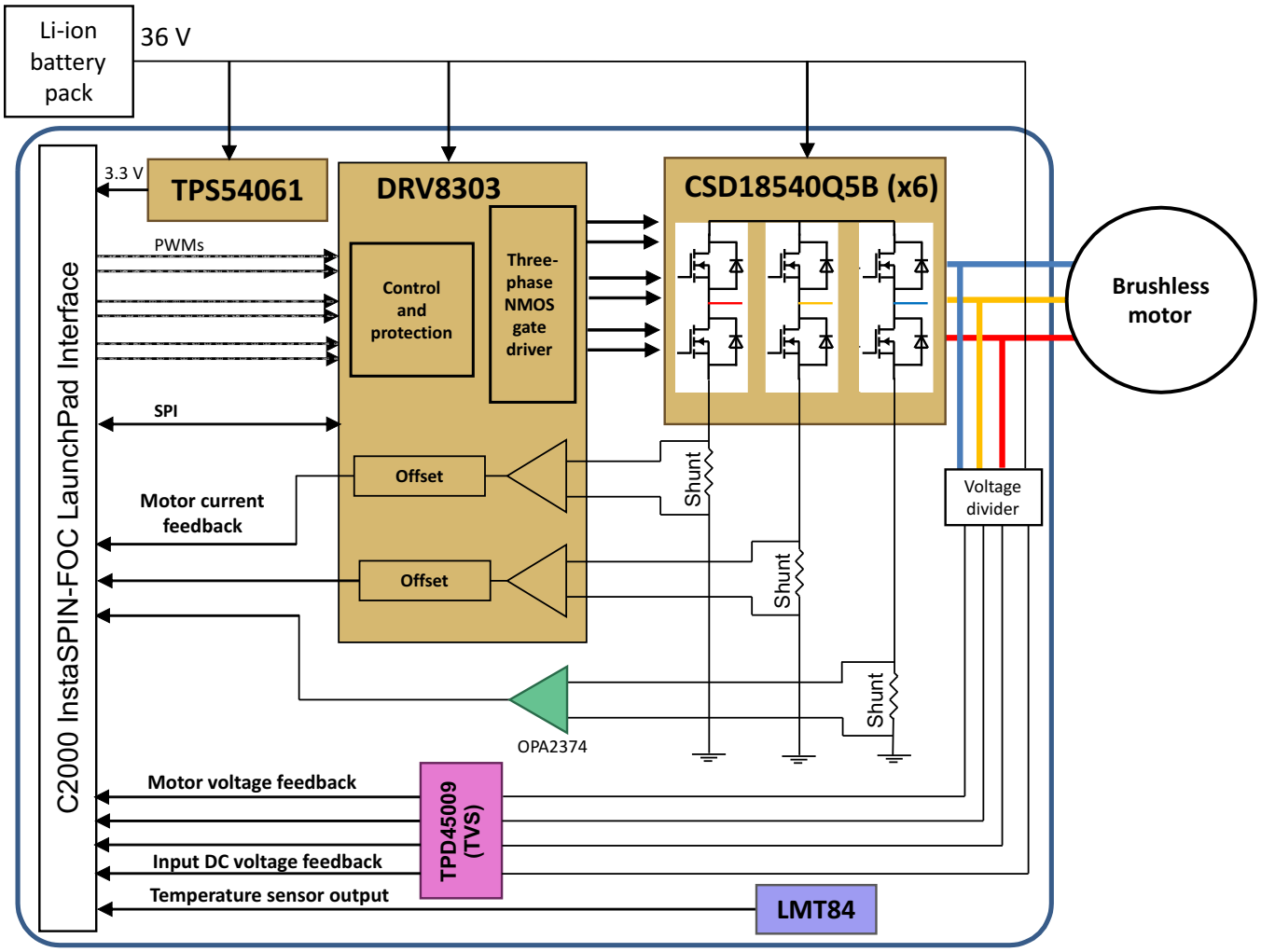


Figure 4. Block Diagram of Power Stage

The inverter is powered from a 36-V 10-cell Lithium-ion battery. The 3.3-V supply required for the MCU in the LaunchPad is generated using the step-down DC-DC converter TPS54061. The C2000 InstaSPIN-FOC LaunchPad is used as the control unit. The motor winding voltages and the inverter leg currents are sensed and fed to the LaunchPad using appropriate signal conditioning circuits. The LaunchPad configures the gate driver DRV8303 using SPI. The temperature sensor LMT84 is used to sense the heat sink temperature and is interfaced to the LaunchPad.

The DRV8303 is the gate driver IC used to drive the three-phase MOSFETs based on the PWM signals generated by the C2000 controller from the LaunchPad. The DRV8303 uses bootstrap gate drivers, and it can be programmed to provide dead time and drain-to-source voltage (V_{DS}) saturation protection. The DRV8303 includes two current shunt amplifiers for accurate current measurement. The third leg current is measured using an external op-amp circuit with the gain set same as the DRV8303 amplifier. The three-phase inverter bridge consists of six CSD18540Q5B power MOSFETs. The voltage feedback signals are ESD protected by the transient voltage suppressor (TVS) diode array TPD4S009 before feeding to the C2000 LaunchPad.

5 Highlighted Products

Key features of the highlighted devices are taken from product datasheets. The following are the highlighted products used in this reference design.

5.1 DRV8303

The DRV8303 is a gate driver IC for three-phase motor drive applications. The device provides three half-bridge drivers, each capable of driving two N-type MOSFETs (one for the high-side and one for the low-side). The DRV8303 supports up to a 2.3-A sink and a 1.7-A source peak current capability, and it only needs a single power supply with a wide range from 6 to 60 V. The DRV8303 uses bootstrap gate drivers with trickle charge circuitry to support 100% duty cycle. The gate driver uses automatic hand shaking when high-side FET or low-side FET is switching to prevent current shoot through. The V_{DS} of FETs is sensed to protect external power stage during overcurrent conditions. The DRV8303 includes two current shunt amplifiers for accurate current measurement. The current amplifiers support bi-directional current sensing and provide an adjustable output offset of up to 3 V. The SPI provides detailed fault reporting and flexible parameter settings such as gain options for current shunt amplifier and slew rate control of the gate driver.

5.2 CSD18540Q5B

The CSD18540Q5B is a 60-V N-Channel NexFET Power MOSFET with a very low R_{DS_ON} of 1.8 mΩ and features very low total gate charge requirement. The CSD18540Q5B is available in very small package, SON 5×6 mm with a peak current rating of 400 A.

5.3 TPD4S009

The TPD4S009 provide system level electrostatic discharge (ESD) solution for high-speed differential lines. These devices offer four ESD clamp circuits for dual pair differential lines. The TPD4S009 offers an optional V_{CC} supply pin, which can be connected to system supply plane. A blocking diode at the V_{CC} pin enables the I_{off} feature for the TPD4S009. The TPD4S009 can handle live signal at the D+, D– pins when the V_{CC} pin is connected to 0 V. The V_{CC} pin allows all the internal circuit nodes of the TPD4S009 to be at known potential during start up time. However, connecting the optional V_{CC} pin to board supply plane does not affect the system level ESD performance of the TPD4S009. The TPD4S009 is offered in DBV, DCK, DGS, and DRY packages. The TPD4S009 comply with IEC 61000-4-2 (Level 4) ESD. The TPD4S009 is characterized for operation over the ambient air temperature range of –40°C to 85°C.

5.4 OPA2374

The OPA2374 is a low-power and low-cost operational amplifier (op-amps) with excellent bandwidth (6.5 MHz) and slew rate (5 V/µs). The input range extends 200 mV beyond the rails and the output range is within 25 mV of the rails. The speed-to-power ratio and small size make these op-amps ideal for portable and battery-powered applications. Under logic control, the amplifiers can be switched from normal operation to a standby current that is less than 1 µA. These op-amps are specified for single or dual power supplies of 2.7 to 5.5 V, with operation from 2.3 to 5.5 V. The OPA2374 can work in the temperature range from −40°C to 125°C.

5.5 TPS54061

The TPS54061 device is a 60-V, 200-mA, synchronous step-down DC-DC converter with integrated high-side and low-side MOSFETs. Current mode control provides simple external compensation and flexible component selection. The non-switching supply current is 90 µA. Using the enable pin, shutdown supply current is reduced to 1.4 µA. To increase light load efficiency, the low-side MOSFET emulates a diode when the inductor current reaches zero. Undervoltage lockout is internally set at 4.5 V but can be increased using two resistors on the enable pin. The output voltage startup ramp is controlled by the internal slow start time. The adjustable switching frequency range allows efficiency and external component size to be optimized. Frequency fold back and thermal shutdown protects the part during an overload condition. The TPS54061 enables small designs by integrating the MOSFETs, boot recharge diode, and minimizing the IC footprint with a small 3×3-mm thermally enhanced VSON package.

5.6 LMT84

The LMT84 is precision CMOS integrated-circuit temperature sensors with an analog output voltage that is linearly and inversely proportional to temperature. Its features make it suitable for many general temperature sensing applications. The LMT84 can operate down to a 1.5-V supply with a 5.4-µA power consumption, making the device ideal for battery-powered devices. Multiple package options, including through-hole TO-92 and TO-126 packages, also allow the LMT84 to be mounted on board, off board, to a heat sink, or on multiple unique locations in the same application. Class-AB output structures gives the LMT84 strong output source and sink current capability that can directly drive up to 1.1-nF capacitive loads. This capability means the device is well suited to drive an analog-to-digital converter sample-and-hold input with its transient load requirements. The LMT84 has accuracy capability specified in the operating range of −50°C to 150°C. The accuracy, 3-lead package options, and other features also make the LMT84 an alternative to thermistors.

6 System Design Theory

6.1 Main Power Input

The main power input section is shown in Figure 5. The input bulk aluminum electrolytic capacitors C20 and C21 provide the ripple current and its voltage rating is de-rated by 50% for better life. These capacitors are rated to carry a high ripple current of 2.8 A. C22 and C24 are used as bypass capacitors to GND. D3 is the TVS having breakdown voltage of 9 V and maximum supply voltage of 6 V.

The input supply voltage +PVDD is scaled using the resistive divider network, which consists of R20, R22, and C23, and fed to the MCU. Considering the maximum voltage for the MCU ADC input as 3.3 V, the maximum DC input voltage measurable by the MCU is calculated as in Equation 1.

$$V_{DC}^{max} = V_{ADC\_DC}^{max} \times \frac{(2.20\ k\Omega + 34.8\ k\Omega)}{2.20\ k\Omega} = 3.3 \times \frac{(2.20\ k\Omega + 34.8\ k\Omega)}{2.20\ k\Omega} = 55.5\ V \quad (1)$$

Considering a 20% headroom for this value, the maximum recommended voltage input to the system is 55.5 × 0.8 = 44.4, so for a power stage with maximum operating voltage of 42 V, this voltage feedback resistor divider is ideal. Also, this choice gives optimal ADC resolution for a system operating from 36 to 42 V.

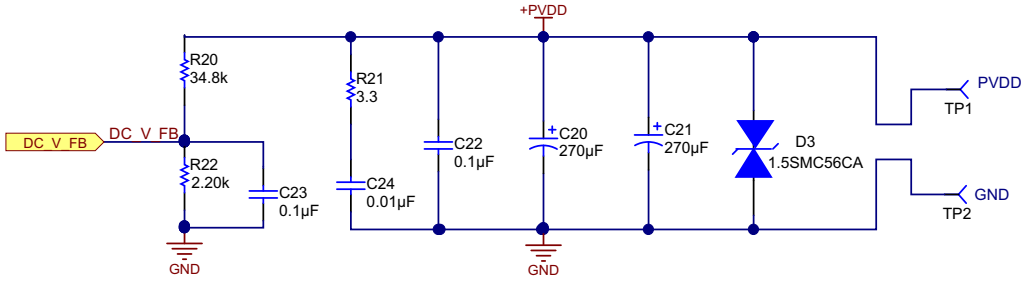


Figure 5. Main Power Input

6.2 Inverter Stage

The power circuit shown in Figure 6 consists of a three-leg MOSFET bridge. The leg currents are measured using three current sensors: R34, R35, and R36. The sensed currents are fed to the MCU through the current shunt amplifiers. A gate resistance of 10 Ω is used at the input of all MOSFET gates. C28, C29, and C30 are the decoupling capacitors connected across each inverter leg.

NOTE: Connect these decoupling capacitors very near to the corresponding MOSFET legs for better decoupling (see Section 10.3). An improper layout or position of the decoupling capacitors can cause undesired V_{DS} switching voltage spikes and unintentional fault detection by the V_{DS} sensing overcurrent operation of the DRV8303.

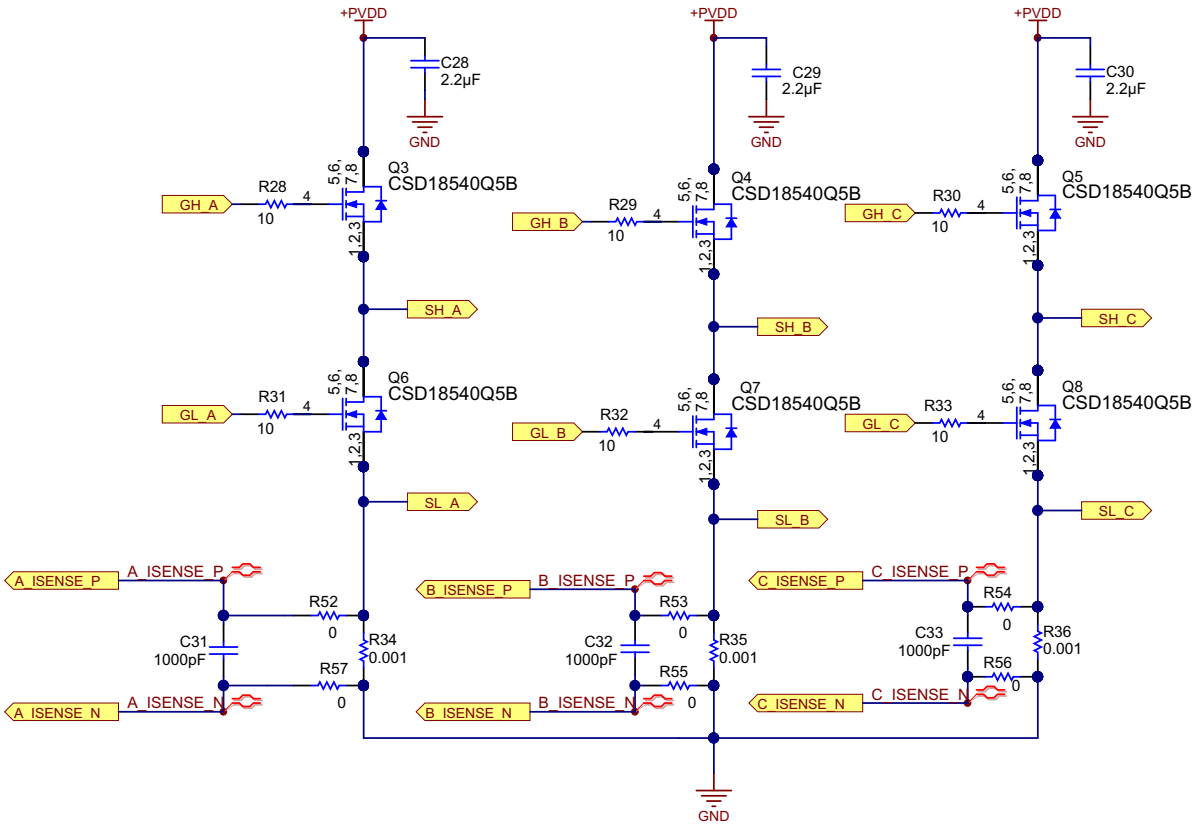


Figure 6. Three-Phase Inverter of Power Stage

6.2.1 Selection of the MOSFET

The board is designed to operate from a 10-cell Li-Ion battery voltage ranging from 30 to 42 V, meaning the maximum input DC voltage in the application is 42 V. Considering the safety factor and switching spikes, the MOSFET with a voltage rating of 1.5 times the maximum input voltage can be selected. A MOSFET with voltage rating greater than or equal to 60 V will be suitable for this application.

The current rating of the MOSFET depends on the peak winding current. The power stage has to provide a 30-A_{RMS} nominal current to the motor winding. The three-phase inverter bridge is switched such that, sinusoidal current is injected into the motor windings. Therefore, the peak value of the winding current = $\sqrt{2} \times I_{RMS}$ = 42.42 A. Considering an overloading 120%, the peak winding current will be 51 A.

For better thermal performance, select the MOSFETs with very low R_{DS_ON}. In the reference design, the MOSFET CSD18540Q5B is selected, which is a 60-V N-Channel NexFET power MOSFET with a very low R_{DS_ON} of 1.8 mΩ and features very low total gate charge requirement. It has continuous drain current capacity (package limited) of 100 A and a peak current capacity of 400 A.

6.2.2 Selection of the Sense Resistor

Power dissipation in sense resistors and the input offset error voltage of the op-amps are important in selecting the sense resistance values. The nominal RMS winding current in motor is 30 A. Therefore, the sense resistors will be carrying a nominal RMS current of 30 A with a peak value 30 × √2 = 42.42 A. A high sense resistance value increases the power loss in the resistors. The internal current shunt amplifiers of the DRV8303 have a DC offset error of 4 mV. The DRV8303 can calibrate the DC offset. However, it is required to select the sense resistor such that the sense voltage across the resistor is sufficiently higher than the offset error voltage to reduce the effect of the offset error.

Selecting a 1-mΩ resistor as the sense resistor, the power loss in the resistor at 30 A_{RMS} is given by Equation 2:

$$\text{Power loss in the resistor} = I_{RMS}^2 \times R_{SENSE} = 30^2 \times 0.001 = 0.9\ \text{W} \quad (2)$$

Therefore, a standard 2-W, 2512-package resistor can be used. For the nominal 42.42 A_{PEAK} sinusoidal winding current, the sense voltage have a peak value of 42.42 mV, which sufficiently larger than the offset error of the op-amp.

6.3 DRV8303 — Three-Phase Gate Driver

The DRV8303 is used as the gate driver IC for the three-phase motor drive. It provides three half-bridge drivers, each capable of driving two N-type MOSFETs, one for the high-side and one for the low-side. Figure 7 shows the schematic of the gate driver section.

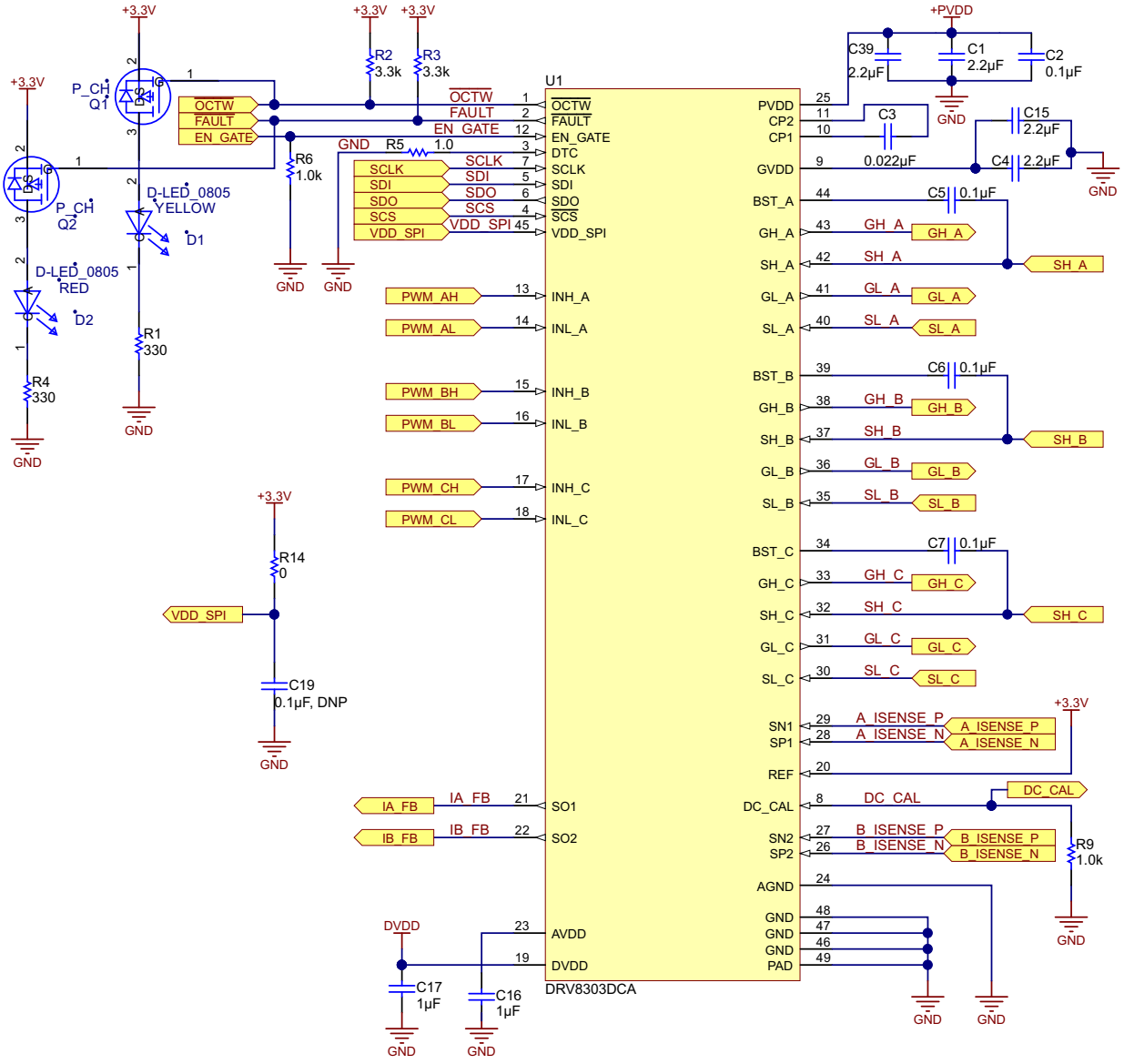


Figure 7. DRV8303 Schematic

The gate driver has following features:

- Internal handshake between high-side and low-side FETs during switching transition to prevent current shoot through
- Programmable slew rate or current driving capability through SPI
- Supports up to 200-kHz switching frequency with Qg(TOT) = 25 nC or total 30-mA gate drive average current
- Provide cycle-by-cycle (CBC) current limiting and latch overcurrent shut down of external FETs. Current is sensed through FET V_{DS} and the overcurrent level is programmable through SPI. V_{DS} sensing range is programmable from 0.060 to 2.4 V with 5-bit resolution
- High-side gate drive will survive negative output from half bridge up to –10 V for 10 ns
- During EN_GATE pin low and fault conditions, the gate driver keeps external FETs in high impedance mode
- Programmable dead time through DTC pin. Dead time control range: 50 to 500 ns. Shorting DTC pin to ground will provide minimum dead time of 50 ns. External dead time will override internal dead time as long as the time is longer than the dead time setting
- Bootstraps circuits are used to drive high-side FETs of three-phase inverter. Trickle charge circuitry is used to replenish current leakage from bootstrap cap and support 100% duty cycle operation

In Figure 7, C1, C2, and C39 are the PVDD decoupling capacitors. PVDD decoupling capacitors should be placed close to their corresponding pins with a low impedance path to device GND (PowerPAD) (See Section 10.3 for more details). PVDD is the power supply pin for gate driver. The DRV8303 provides power stage undervoltage protection by driving its outputs low whenever PVDD is below 6 V (PVDD_UV). The PVDD undervoltage will be reported through $\overline{\text{FAULT}}$ pin and SPI status register. C5, C6, and C7 are the bootstrap capacitors. The detailed design and features of the DRV8303 are explained in the following sections.

6.3.1 Internal Regulator Voltages of DRV8303

AVDD

AVDD is the internal 6-V supply voltage. Connect the AVDD capacitor to the AGND. AVDD is an output, but not specified to drive external circuitry. In the schematic, C16 is used as the AVDD capacitor with a recommended value of 1 uF. Typical AVDD voltage is 6.5 V. The minimum specified value is 6 V and a maximum of 7 V.

DVDD

Internal 3.3-V supply voltage. Connect the DVDD capacitor to the AGND. DVDD is an output, but not specified to drive external circuitry. In the schematic, C17 is used as the DVDD capacitor with a recommended value of 1 uF. Place AVDD and DVDD capacitors close to their corresponding pins with a low impedance path to the AGND pin (see Section 10.3 for more details). Make this connection on the same layer. Tie AGND to device GND (PowerPAD) through a low-impedance trace or copper fill. Typical DVDD voltage is 3.3 V. The minimum specified value is 3 V and maximum is 3.6 V. If DVDD goes to undervoltage, the external FETs go to high-impedance state by means of weak pull down of all gate driver output. On recovering from undervoltage, the DRV8303 resets the SPI registers. The DVDD undervoltage will be reported through $\overline{\text{FAULT}}$ pin.

GVDD

GVDD is the voltage output from internal gate driver voltage regulator. The capacitor C15 is connected to the GVDD pin. Connect the GVDD capacitor to GND. Typically, use a 2.2-uF ceramic capacitor as the GVDD capacitor. Place the GVDD capacitor close to its corresponding pin with a low-impedance path to device GND (PowerPAD) (See Section 10.3 for more details). GVDD pin is protected from undervoltage and overvoltage. The undervoltage protection limit is 7.5 V and overvoltage protection limit is 16 V. When undervoltage protection is triggered, the DRV8303 outputs are driven low and the external MOSFETs will go to a high-impedance state. The GVDD undervoltage will be reported through $\overline{\text{FAULT}}$ pin and SPI status register. The GVDD overvoltage fault is a latched fault and can only be reset through a transition on EN_GATE pin. The GVDD overvoltage will be reported through $\overline{\text{FAULT}}$ pin and SPI status register.

6.3.2 Current Shunt Amplifiers in DRV8303

The DRV8303 includes two high performance current shunt amplifiers for accurate current measurement. The current amplifiers provide output offset up to 3 V to support bi-directional current sensing. The current shunt amplifier has following features:

- Programmable gain: Four gain settings (10, 20, 40, 80) are possible through SPI command
- Programmable output offset through reference pin (half of the V_{ref})
- Minimize DC offset and drift over temperature with DC calibration through SPI command or DC_CAL pin. When DC calibration is enabled, the device will short input of current shunt amplifier and disconnect the load. DC calibrating can be done at any time even when FET is switching because the load is disconnected. For best results, perform the DC calibrating during the switching off period when no load is present to reduce the potential noise impact to the amplifier

The output of current shunt amplifier can be calculated as:

$$V_O = \frac{V_{ref}}{2} - G \times (SN_X - SP_X) \quad (3)$$

where

- V_{ref} is the reference voltage
- G is the gain of the amplifier
- SN_x and SP_x are the inputs of channel X

SP_x should connect to resistor ground for the best common mode rejection. The selection of the gain of the amplifier is explained in Section 6.4.

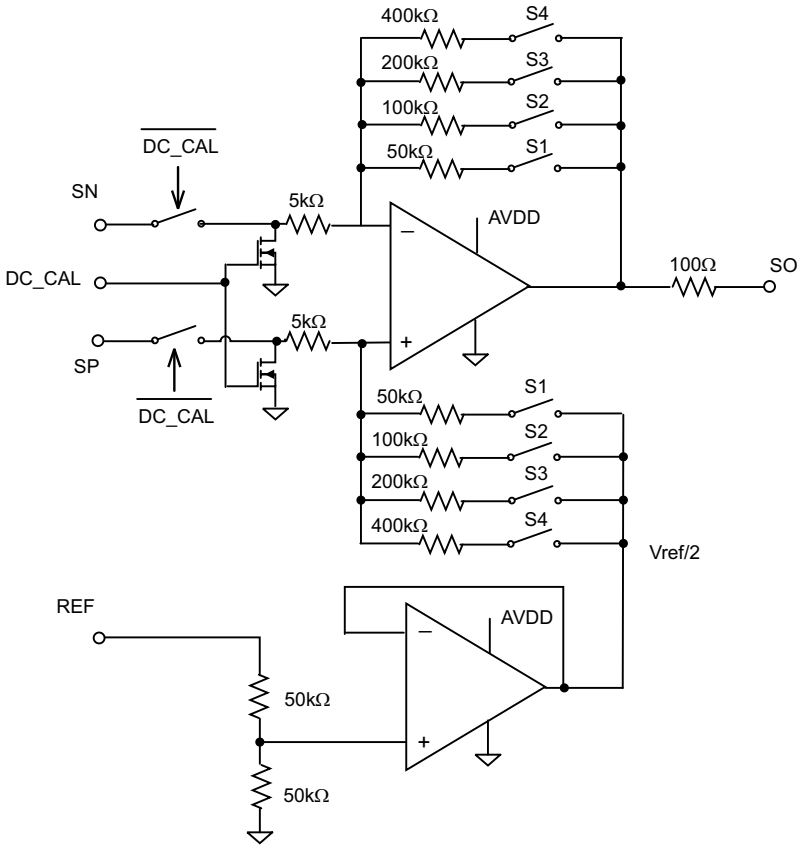


Figure 8. Simplified Block Diagram of Current Shunt Amplifier in DRV8303

6.3.3 Protection Features in DRV8303

Overcurrent Protection and Reporting

To protect the power stage from damage due to high currents, a V_{DS} sensing circuitry is implemented in the DRV8303. Based on the R_{DS_ON} of the power MOSFETs and the maximum allowed drain current, a voltage threshold can be calculated which, when exceeded, triggers the overcurrent protection feature. This voltage threshold level is programmable through SPI command.

There are total four OC_MODE settings in SPI:

1. Current limit mode
   When current limit mode is enabled, the DRV8303 limits the MOSFET current instead of shutting down during the overcurrent event. The overcurrent event is reported through the overcurrent temperature warning ($\overline{OCTW}$) pin. $\overline{OCTW}$ reporting will hold low during same PWM cycle or for a max 64-µs period (internal timer) so that the external controller has enough time to sample the warning signal. If in the middle of reporting other FETs get overcurrent, then $\overline{OCTW}$ reporting will hold low and recount another 64 µs unless PWM cycles on both FETs are ended.

   There are two current control settings in current limit mode (selected by one bit in SPI and default is CBC mode):

   - Setting 1 (CBC mode): during overcurrent event, the FET that detected overcurrent will turn off until next PWM cycle.
   - Setting 2 (off-time control mode):
     - During overcurrent event, the FET that detected overcurrent will turn off for 64 µs as off time and back to normal after that (so same FET will be on again) if PWM signal is still holding high. Since all three phases or six FETs share a single timer, if more than one FET get overcurrent, the FETs will not be back to normal until the all FETs that have overcurrent event pass 64 µs.
     - If PWM signal is toggled for this FET during timer running period, device will resume normal operation for this toggled FET. So real off-time could be less than 64 µs in this case.
     - If two FETs get overcurrent and one FET's PWM signal gets toggled during timer running period, this FET will be back to normal, and the other FET will be off until the timer ends (unless its PWM is also toggled).
2. Overcurrent latch shutdown mode
   When overcurrent occurs, the device will turn off both high-side and low-side FETs in the same phase if any of the FETs in that phase have overcurrent.
3. Report only mode
   No protection action will be performed in this mode. Overcurrent detection will be reported through the $\overline{OCTW}$ pin and SPI status register. External MCU takes actions based on its own control algorithm. A pulse stretching of 64 µs will be implemented on $\overline{OCTW}$ pin so the controller can have enough time to sense the overcurrent signal.
4. Overcurrent disable mode
   The device will ignore all the overcurrent detections and will not report them either.

Undervoltage Protection

To protect the power stage during undervoltage conditions, the DRV8303 provides power stage undervoltage protection by driving its outputs low whenever PVDD is below 6 V (PVDD_UV) or GVDD is below 7.5 V (GVDD_UV). When undervoltage protection is triggered, the DRV8303 outputs are driven low and the external MOSFETs will go to a high impedance state.

Overvoltage Protection (GVDD_OV)

The DRV8303 will shut down both the gate driver and charge pump if GVDD voltage exceeds 16 V to prevent potential issue related to the GVDD or charge pump (for example, short of external GVDD cap or charge pump). The fault is a latched fault and can only be reset through a transition on EN_GATE pin.

Over Temperature Protection

A two-level over temperature detection circuit is implemented in the DRV8303:

- Level 1: over temperature warning (OTW). OTW is reported through $\overline{\text{OCTW}}$ pin for default setting. The $\overline{\text{OCTW}}$ pin can be set to report OTW or overcurrent warning only through SPI command.
- Level 2: over temperature latched shut down of gate driver and charge pump (OTSD_GATE). The fault will be reported to the $\overline{\text{FAULT}}$ pin. This pin is a latched shut down, so the gate driver will not be recovered automatically—even over temperature condition is not present anymore. An EN_GATE reset through pin or SPI (RESET_GATE) is required to recover gate driver to normal operation after temperature goes below a preset value, t_{OTSD_CLR}. SPI operation is still available and register settings will be remaining in the device during OTSD operation as long as PVDD is still within defined operation range.

Junction temperature for resetting over temperature warning (OTW_CLR) is 115°C. Junction temperature for the over temperature warning and resetting over temperature shutdown (OTW_SET/OTSD_CLR) is 130°C.

Fault and Protection Handling

The $\overline{\text{FAULT}}$ pin indicates an error event (with shutdown) has occurred such as overcurrent, over temperature, overvoltage, or undervoltage. Note that $\overline{\text{FAULT}}$ is an open-drain signal. $\overline{\text{FAULT}}$ will go high when gate driver is ready for PWM signal (internal EN_GATE goes high) during start up. The $\overline{\text{OCTW}}$ pin indicates overcurrent event and over temperature event that not necessary related to shut down. $\overline{\text{OCTW}}$ is an open-drain signal.

EN_GATE

EN_GATE low is used to put the gate driver, charge pump, current shunt amplifier, and internal regulator blocks into a low-power consumption mode to save energy. SPI communication is not supported during this state. The device will put the MOSFET output stage to a high-impedance mode as long as PVDD is still present. When EN_GATE pin goes high, it will go through a power-up sequence, and enable gate driver, current amplifiers, charge pump, internal regulator, and so on and reset all latched faults related to the gate driver block. The pin will also reset status registers in the SPI table. All latched faults can be reset when EN_GATE is toggled after an error event unless the fault is still present. When EN_GATE goes from high to low, it will shut down gate driver block immediately, so the gate output can put external FETs in high impedance mode. It will then wait for 10 µs before completely shutting down the rest of the blocks.

A quick fault reset mode can be done by toggling EN_GATE pin for a very short period (less than 10 µs). This will prevent device to shut down other function blocks such as charge pump and internal regulators and bring a quicker and simple fault recovery. SPI will still function with such a quick EN_GATE reset mode. The other way to reset all the faults is to use SPI command (RESET_GATE), which will only reset gate driver block and all the SPI status registers without shutting down other function blocks. One exception is to reset a GVDD_OV fault. A quick EN_GATE quick fault reset or SPI command reset will not work with GVDD_OV fault. A complete EN_GATE with low level holding longer than 10 µs is required to reset GVDD_OV fault. Inspect the system and board when GVDD_OV occurs.

DTC

Dead time can be programmed through DTC pin. Connect a resistor from DTC to ground to control the dead time. Dead time control range is from 50 to 500 ns. A short DTC pin to ground will provide the minimum dead time (50 ns). The resistor range is 0 to 150 kΩ. Dead time is linearly set over this resistor range. Current shoot through prevention protection is constantly enabled in the device, independent of dead time setting and input mode setting. In the reference design, a 1-Ω resistor is connected to the DTC pin.

6.3.4 SPI Communication

VDD_SPI
VDD_SPI is the power supply to power SDO pin. It has to be connected to the same power supply (3.3 V or 5 V) that the MCU uses for its SPI operation. During power up or down transient, VDD_SPI pin could be zero voltage shortly. During this period, no SDO signal should be present at the SDO pin from any other devices in the system because it causes a parasitic diode in the DRV8303 conducting from SDO to VDD_SPI pin as a short. This should be considered and prevented from system power sequence design.

DC_CAL
When DC_CAL is enabled, the device will short inputs of the shunt amplifier and disconnect from the load, so the external microcontroller (or SPI command) can calibrate the DC offset. Using the SPI exclusively for DC calibration, the DC_CAL pin can be connected to GND.

SPI Pins
The SDO pin has to be 3-state, so a data bus line can be connected to multiple SPI slave devices. The SCS pin is active low. When SCS is high, SDO is at high impendence mode.

SPI
SPI is used to set device configuration, operating parameters and read out diagnostic information. The DRV8303 SPI operates in the slave mode. The SPI input data (SDI) word consists of 16-bit word, with 11-bit data and 5-bit (MSB) command. The SPI output data (SDO) word consists of 16-bit word, with 11-bit register data and 4-bit MSB address data and one frame fault bit (active 1). When a frame is not valid, frame fault bit will set to 1, and rest of SDO bit will shift out zeroes.

A valid frame has to meet following conditions:

1. Clock must be low when /SCS goes low.
2. Clock must have 16 full cycles.
3. Clock must be low when /SCS goes high.

When SCS is asserted high, any signals at the SCLK and SDI pins are ignored, and SDO is forced into a high impedance state. When SCS transitions from high to low, SDO is enabled and the SPI response word loads into the shift register based on 5-bit command in SPI at the previous clock cycle. The SCLK pin must be low when SCS transitions low. While SCS is low, at each rising edge of the clock, the response bit is serially shifted out on the SDO pin with MSB shifted out first. While SCS is low, at each falling edge of the clock, the new control bit is sampled on the SDI pin. The SPI command bits are decoded to determine the register address and access type (read or write). The MSB will be shifted in first. If the word sent to SDI is less than 16 bits or more than 16 bits, it is considered a frame error. If it is a write command, the data will be ignored. The fault bit in SDO (MSB) will report 1 at next 16-bit word cycle. After the 16^{th} clock cycle or when SCS transitions from low to high, in case of write access type, the SPI receive shift register data is transferred into the latch where address matches decoded SPI command address value. Any amount of time may pass between bits as long as SCS stays active low, which allows two 8-bit words to be used.

For a read command (N^{th} cycle) in SPI, SPO will send out data in the register with address in read command in next cycle (N+1). For a write command in SPI, SPO will send out data in the status register 0x00h in next 16-bit word cycle (N+1). For most of the time, this feature will maximize SPI communication efficiency when having a write command, but still get fault status values back without sending extra read command.

SPI Format
An SPI input data control word is 16 bits long, consisting of:

- 1 read or write bit W [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

An SPI output data response word is 16 bits long, and its content depends on the given SPI command (SPI Control Word) in the previous cycle. When an SPI Control Word is shifted in, the SPI Response Word (that is shifted out during the same transition time) is the response to the previous SPI Command (shift in SPI Control Word 'N' and shift out SPI Response Word "N-1"). Therefore, each SPI Control / Response pair requires two full 16-bit shift cycles to complete. The definitions of all SPI registers are given in the datasheet of DRV8303 (SLOS846).

6.4 External Current Shunt Amplifier (OPA2374)

The DRV8303 includes two current shunt amplifiers for accurate current measurement, which are used to measure the two leg currents in the three-phase inverter. The third leg current is measured using external current shunt amplifier. In the reference design, phase A and phase B leg currents are measured using the DRV8303 current shunt amplifiers. The phase C current is measured using the external amplifier. The schematic of the external current amplifier is shown in Figure 9.

To measure bidirectional currents, the circuit require a reference voltage of 1.65 V. This voltage is generally not available in 3.3-V systems, but it can be created very easily by a voltage follower. In Figure 9, U3B is a voltage follower that generates a 1.65-V reference from a 3.3-V input.

The phase C leg current is measured across the shunt resistor and amplified by the differential amplifier U3A. The output of U3A is unidirectional with an offset voltage of 1.65 V added from the U3B. The gain of the differential amplifier has to be matched with the DRV8303 gain. The DRV8303 can provide four gains (10, 20, 40 and 80) through SPI command. The gain of the circuit has to be designed along with the shunt resistor value to get the full swing of 3.3 V. In the reference design, the maximum value of the peak winding current is set at 80 A.

The shunt resistor value is designed to 1 mΩ and the gain of the amplifier (AMPLIFIER_GAIN) is selected as 20, to get full swing at the input of the ADC of MCU at the peak current.

Selecting R43 = R47 and R44 = R45, Gain of the amplifier = R43/R44

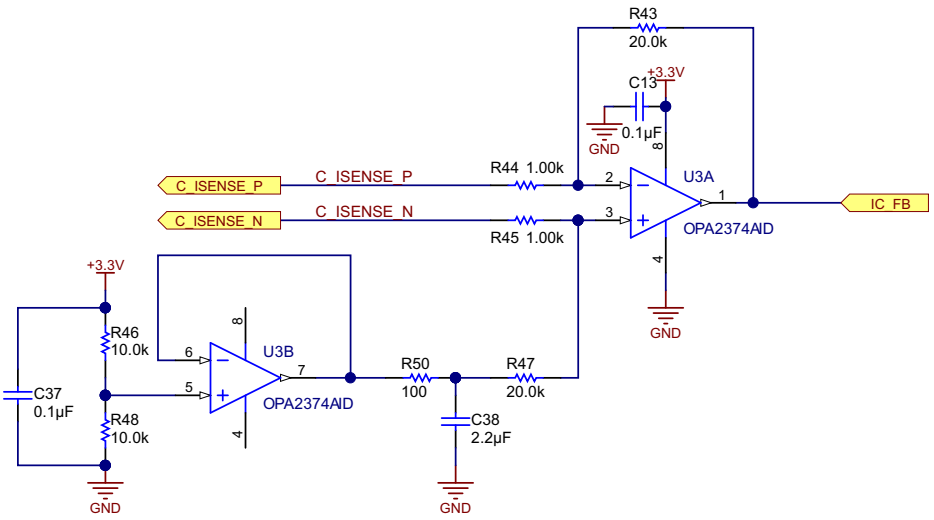


Figure 9. External Current Shunt Amplifier for Phase C Current Sense

6.5 Motor Current Sensing — Settings

The motor current sensing amplifier gain has to be designed to get maximum resolution from the ADC of the MCU. Considering the external shunt amplifier, the output of the current shunt amplifier can be written as in Equation 4:

$$\text{Output of the current shunt amplifier} = 1.65 + \left(I_C \times R_{SENSE} \times \text{AMPLIFIER\_GAIN}\right) \quad (4)$$

Here, I_C is the phase C leg current. Equation 4 is also valid for the current shunt amplifiers in the DRV8303 used for phase A and phase B leg current sensing. The maximum leg current feedback measurable by the MCU can be calculated as follows, considering the maximum voltage for the ADC input is 3.3 V:

If I_a^{max} is the peak value of the phase A leg current measurable by the ADC, then

$$1.65 + (I_a^{max} \times R_{SENSE} \times \text{AMPLIFIER\_GAIN}) = V_{ADC\_Ia}^{max} \quad (5)$$

$$I_a^{max} = \frac{\left(V_{ADC_{Ia}}^{max} - 1.65\right)}{R_{SENSE} \times \text{AMPLIFIER\_GAIN}} = \frac{(3.3 - 1.65)}{0.001 \times 20} = 82.5 \quad (6)$$

Therefore, the peak-to-peak maximum current measurable by the ADC is 165 A. With this current feedback circuit, the following setting is done in user.h (see Section 7 for the details about user.h).

```
//! \brief Hardware dependent, this should be based on the current sensing and
scaling to the ADC input
#define USER_ADC_FULL_SCALE_CURRENT_A       (165)
```

NOTE: USER_IQ_FULL_SCALE_CURRENT_A is a parameter used in user.h, which defines the full scale current for the I_Q variables. This value must be larger than the maximum current readings that you are expecting from the motor. If the measured current is greater than the USER_IQ_FULL_SCALE_CURRENT_A at any point, there might be a numerical overflow condition in the software. Make sure the measurable current is less than this value to avoid an undesirable software behavior.

To avoid this issue, make sure that (USER_IQ_FULL_SCALE_CURRENT_A × 2) is always greater than the measurable current by the ADC. The "multiply by 2" factor is because the USER_IQ_FULL_SCALE_CURRENT_A parameter ranges from zero to maximum amplitude (peak), while the USER_ADC_FULL_SCALE_ CURRENT_A is from peak to peak.

See the INSTA-FOC user's guide for more details (SPRUHJ1).

6.6 Motor Winding Voltage Sensing

The voltage divider circuit shown in the Figure 10 is used to measure the winding voltages. Voltage feedback is needed in the FAST estimator of the InstaSPIN-FOC to allow the best performance at the widest speed range. In FAST, phase voltages are measured directly from the motor phases instead of a software estimate. This software value (USER_ADC_FULL_SCALE_VOLTAGE_V) depends on the circuit that senses the voltage feedback from the motor phases.

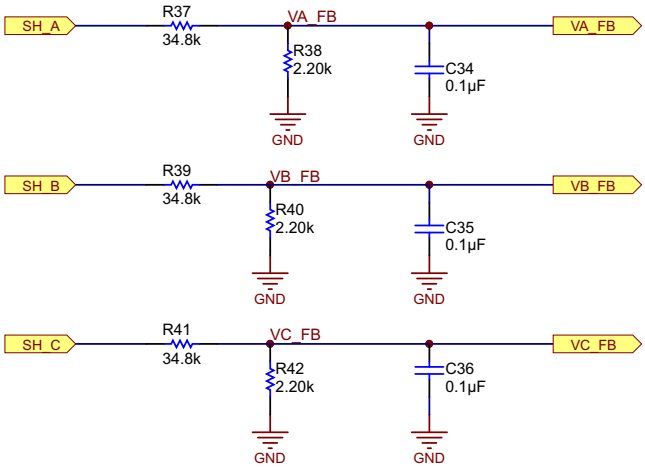


Figure 10. Motor Winding Voltage Sense Circuit

In Figure 10, SH_A, SH_B, and SH_C are the phase voltages. These voltages are properly scaled and fed to the MCU through VA_FB, VB_FB, and VC_FB. The maximum phase voltage feedback measurable by the MCU can be calculated as follows, considering the maximum voltage for the ADC input is 3.3 V:

$$V_a^{max} = V_{ADC\_a}^{max} \times \frac{(2.20\ k\Omega + 34.8\ k\Omega)}{2.20\ k\Omega} = 3.3 \times \frac{(2.20\ k\Omega + 34.8\ k\Omega)}{2.20\ k\Omega} = 55.5\ V \quad (7)$$

With that voltage feedback circuit, the following setting is done in user.h:

```
//! \brief Defines the maximum voltage at the input to the AD converter
#define USER_ADC_FULL_SCALE_VOLTAGE_V (55.5)
```

Considering a 20% headroom for this value, the maximum voltage input to the system is recommended to be 55.5 × 0.8 = 44.4; for a motor with maximum operating voltage of 42 V, this voltage feedback resistor divider is ideal. This divider makes sure that the ADC resolution is maximum for a motor working from 36 to 42 V.

The voltage filter pole is needed by the FAST estimator to allow an accurate detection of the voltage feedback. The filter cut off frequency should be low enough to filter out the PWM signals. As a general guideline, a cutoff frequency of a few hundred Hertz is enough to filter out a PWM frequency of 10 to 20 kHz. The hardware filter should only be changed when ultra-high speed motors are run, which generate phase voltage frequencies of a few kHz. In this reference design, consider the PMSM with a maximum speed of about 3,000 RPM with eight pole pairs. This motor gives a voltage frequency of 3000 × 8 / 60 = 400 Hz. The voltage filter of around this frequency of 400 Hz should be enough cutoff frequency for this motor and speed. The filter pole setting can be calculated as follows:

$$F_{filter\_pole} = \frac{1}{2 \times \pi \times R_{parallel} \times C} = \frac{1}{2 \times \pi \times \left(\frac{34.8\ k\Omega \times 2.2\ k\Omega}{34.8\ k\Omega + 2.2\ k\Omega} \right) \times 0.1\ \mu F} = 769.16\ Hz \quad (8)$$

The following code example shows how this is defined in user.h:

```
//! \brief Defines the analog voltage filter pole location, Hz
#define USER_VOLTAGE_FILTER_POLE_Hz (769.16)
```

NOTE: The parameter USER_IQ_FULL_SCALE_VOLTAGE_V defines the full-scale value for the IQ30 variable of voltage inside the system. All voltages are converted into per unit based on the ratio to this value. This value must be larger than the maximum value of any voltage calculated inside the control system otherwise the value can saturate and roll over, causing an inaccurate value. This value is often greater than the maximum measured ADC value, especially with high BEMF motors operating at higher than rated speeds. If the value of your BEMF constant is known and the design is operating at a speed higher than its rated speed due to field weakening, set this value higher than the expected BEMF voltage.

See the InstaSPIN-FOC user's guide for more details (SPRUHJ1).

6.7 Design of 36-V to 3.3-V Step-Down DC-DC Converter

The 3.3-V regulated power supply for the board is derived using the switching converter TPS54061. The TPS54061 device is a 60-V, 200-mA, step-down (buck) regulator with an integrated high-side and low-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current mode control, which reduces output capacitance and simplifies external frequency compensation design. The design specifications of the step-down converter are given in Table 2. The schematic of the step-down converter is shown in Figure 11.

Table 2. Design Specifications of Step-Down Converter

PARAMETER	VALUE
Conduction mode	Continuous conduction mode (CCM)
Output voltage	3.3 V
Maximum output current	150 mA
Input voltage	36 V nominal (36 to 42 V)
Output voltage ripple	0.5% of V_{OUT}
Start input voltage (rising V_{IN})	33 V
Stop input voltage (falling V_{IN})	30 V

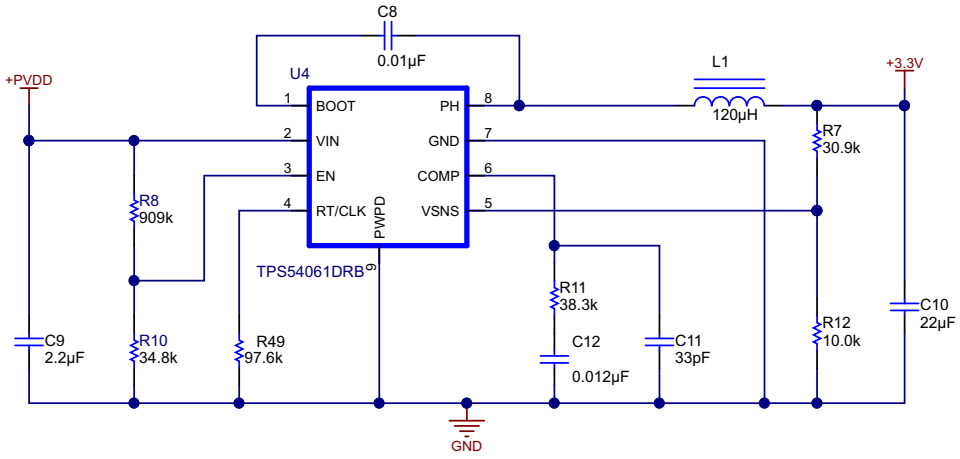


Figure 11. 36-V to 3.3-V Step-Down Converter

The following parameters symbols are used for the further analysis of the buck converter:

- $L_{O,min}$ — Minimum value of output inductor
- L_O — Output inductor
- $V_{IN,max}$ — Maximum value of input voltage
- $V_{IN,min}$ — Minimum value of input voltage
- V_{OUT} — Output voltage
- I_{OUT} — Average output current
- f_{sw} — Switching frequency

6.7.1 Selecting the Switching Frequency

The switching frequency of the TPS54061 is adjustable over a wide range, from 50 kHz to 1100 kHz, by varying the resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.53 V and must have a resistor to ground to set the switching frequency. To reduce the solution size, set the switching frequency as high as possible; however, consider the tradeoffs of the supply efficiency, maximum input voltage, and minimum controllable on time. The minimum controllable on time is typically 120 ns and limits the operating frequency for high input voltages. To determine the timing resistance (R_T) for a given switching frequency, use Equation 9.

$$R_T\,(k\Omega) = \frac{71657}{f_{sw}\,(kHz)^{1.039}} \tag{9}$$

The switching frequency is set by resistor R49 shown in Figure 11. The reference design uses a switching frequency of 573 kHz.

6.7.2 Output Inductor Selection (L_o)

To calculate the minimum value of the output inductor, use Equation 10:

$$L_{O,min} \geq \frac{V_{IN,max} - V_{OUT}}{K_{IND} \times I_O} \times \frac{V_{OUT}}{V_{IN,max} \times f_{sw}} = \frac{42 - 3.3}{0.4 \times 0.15} \times \frac{3.3}{42 \times 573 \times 10^3} = 89\,\mu H \tag{10}$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. This design uses a K_{IND} of 0.4. The minimum inductor value is calculated to be greater than 89 µH. For this design, a standard 120-µH value was chosen as the L_O. The inductor current ripple (I_{RIPPLE}), RMS inductor current ($I_L$rms), and peak inductor current ($I_L$peak) can be calculated using Equation 11 through Equation 13.

$$I_{RIPPLE} \geq \frac{V_{OUT} \times (V_{IN}\,max - V_{OUT})}{V_{IN}\,max \times L_O \times f_{sw}} = \frac{3.3 \times (42 - 3.3)}{42 \times 120 \times 10^{-6} \times 573 \times 10^3} = 44.22\,mA \tag{11}$$

$$I_L rms = \sqrt{I_O{}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN}\,max - V_{OUT})}{V_{IN}\,max \times L_O \times f_{sw}} \right)^2}$$

$$I_L rms = \sqrt{0.15^2 + \frac{1}{12} \times \left(\frac{3.3 \times (42 - 3.3)}{42 \times 120 \times 10^{-6} \times 573 \times 10^3} \right)^2} = 0.15\,A \tag{12}$$

$$I_L peak = I_{OUT} + \frac{I_{RIPPLE}}{2} = 0.15 + \frac{0.04422}{2} = 0.172\,A \tag{13}$$

For this design, the RMS inductor current is 150 mA and the peak inductor current is 172 mA. The chosen inductor has a saturation current rating of 250 mA and an RMS current rating of 220 mA. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the calculated peak inductor current.

6.7.3 Output Capacitor

Consider these three aspects when selecting the value of the output capacitor: the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria. Equation 14 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where f_{sw} is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current.

$$C_{out} \geq \frac{I_{RIPPLE}}{V_{RIPPLE}} \times \left(\frac{1}{8 \times f_{sw}} \right) \tag{14}$$

Refer to the datasheet of TPS54061 for the detailed description of the capacitor selection (SLVSBB7). The reference design uses a 22-µF, 4-V X5R ceramic capacitor.

6.7.4 Bootstrap Capacitor Selection

Connect a 0.01-µF ceramic capacitor between the BOOT and PH pins for proper operation. Use a ceramic capacitor with X5R or better grade dielectric with a voltage rating of 10 V or higher.

6.7.5 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the V_{SENSE} pin. Use 1% tolerance or better divider resistors. Start with 10 kΩ for the R_{LS} resistor and use the Equation 15 to calculate R_{HS}.

$$R_{HS} = R_{LS} \times \left(\frac{V_{OUT} - 0.8\ V}{0.8\ V} \right) \tag{15}$$

Selecting R_{LS} = R12 = 10 k; To get V_{OUT} = 3.3 V

R_{HS} = R7 = 30.9 k (Selecting the standard value)

6.7.6 Undervoltage Lockout Set Point

The undervoltage lock out (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54061. The UVLO has two thresholds: one for power up when the input voltage is rising, and one for power down or brown outs when the input voltage is falling. The programmable UVLO and enable voltages are set by connecting the resistor divider between +PVDD and ground to the EN pin. Equation 16 and Equation 17 can be used to calculate the resistance values necessary.

$$R8 = R_{UVLO}1 = \frac{V_{START}\left(\frac{V_{ENAFALLING}}{V_{ENARISING}} \right) - V_{STOP}}{I_1 \times \left(1 - \frac{V_{ENAFALLING}}{V_{ENARISING}} \right) + I_{HYS}} \tag{16}$$

$$R10 = R_{UVLO}2 = \frac{R_{UVLO}1 \times V_{ENAFALLING}}{V_{STOP} - V_{ENAFALLING} + R_{UVLO}1 \times \left(I_1 + I_{HYS} \right)} \tag{17}$$

From the datasheet of TPS54061:

- The EN pin rising threshold, $V_{ENARISING}$ = 1.23 V
- The EN pin falling threshold, $V_{ENAFALLING}$ = 1.18 V
- The EN pin internal pull up current, I_1 = 1.2 µA
- The hysteresis current, I_{HYS} = 3.5 µA

The UVLO feature can be used to protect the Lithium-ion batteries from discharging below the safe voltage level. Generally, 3.6 V per cell is considered a safe voltage to operate the batteries safely. General standard of discharge protection voltage is 2.75 V. Sometimes, 3.0 V is a safer setting. Considering 3.0 V per cell as the protection voltage on discharge for the 10-cell unit, disconnect the battery when the battery unit voltage reaches 30 V to avoid further discharge. Considering these values, the UVLO thresholds for the reference design are:

- The power up threshold, V_{START} = 33 V
- The power down threshold, V_{STOP} = 30 V

Using the above design vales, a 909-kΩ resistor between +PVDD and EN and a 34.8-kΩ resistor between EN and ground are required to produce the 33-V and 30-V start and stop voltages, respectively.

6.8 Heat Sink Temperature Sensor

Figure 12 shows the temperature sensor circuit used to measure the heat sink temperature. The LMT84 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage, thus providing a low-impedance output source. The average output sensor gain is –5.5 mV/°C.

Although the LMT84 is very linear, its response does have a slight parabolic shape. The output voltages at different temperatures are given in the datasheet of LMT84 in tabular form (SNIS167). For an even less accurate linear approximation, a line can easily be calculated over the desired temperature range using the two-point equation of a line. Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

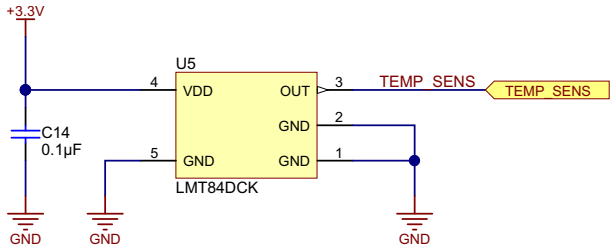


Figure 12. Heat Sink Temperature Sensor

6.9 LaunchPad Connections

Figure 13 shows the LaunchPad connections. The C2000 InstaSPIN-FOC LaunchPad is used in the testing. The TPD4S009 provides system level electrostatic discharge (ESD) protection in the voltage feedback signal lines. The current sense feedback signals from the current shunt amplifiers are filtered and fed to the LaunchPad. The TEMP_SENS is the signal from the temperature sensor, $\overline{\text{FAULT}}$ and $\overline{\text{OCTW}}$ signals from the DRV8303 are also connected to the LaunchPad so that the MCU can be programmed to take necessary action during these fault events. The signal connections SCLK, SCS, SDI, and SDO are required for the SPI programming of the DRV8303. The DC offset calibration of the shunt amplifiers in the DRV8303 are controlled through DC_CAL signal. EN_gate is used to enable gate driver and current shunt amplifiers of the DRV8303.

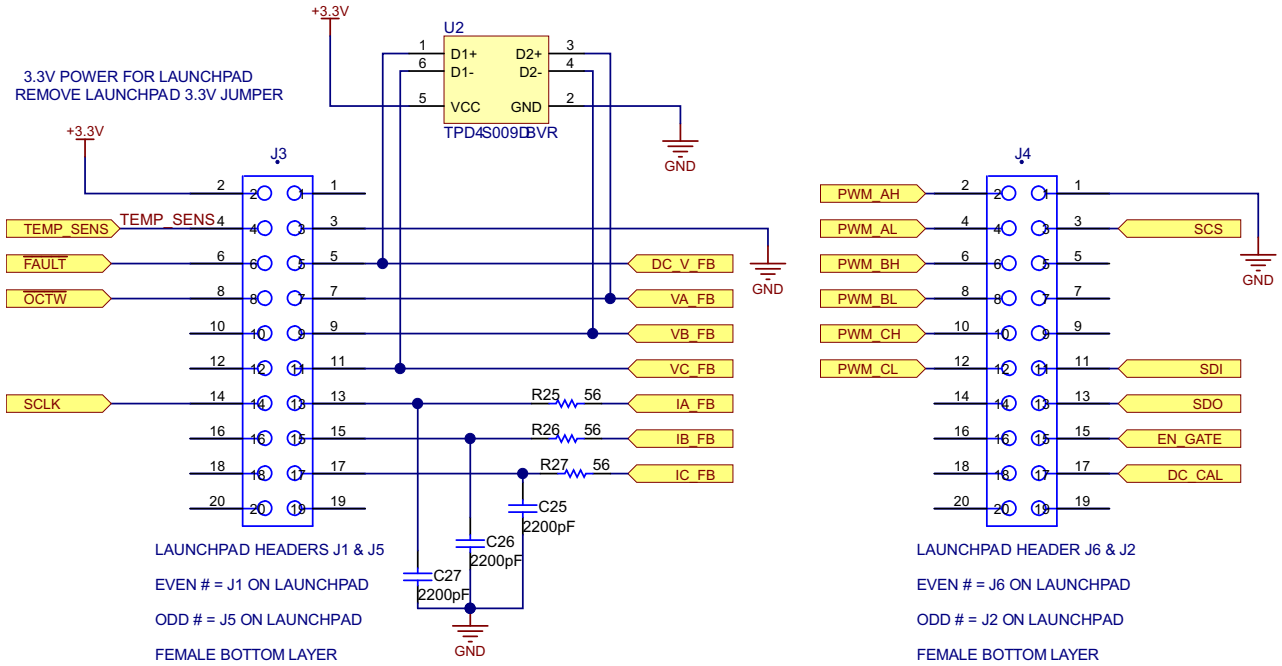


Figure 13. LaunchPad Connections for C2000 InstaSPIN-FOC Controller

6.10 Fault Indications

The DRV8303 fault indication outputs $\overline{\text{OCTW}}$ and $\overline{\text{FAULT}}$ are pulled up and connected to two LED indications as shown in Figure 14. Table 3 shows the faults in the DRV8303 indicated through the two fault reporting output pins.

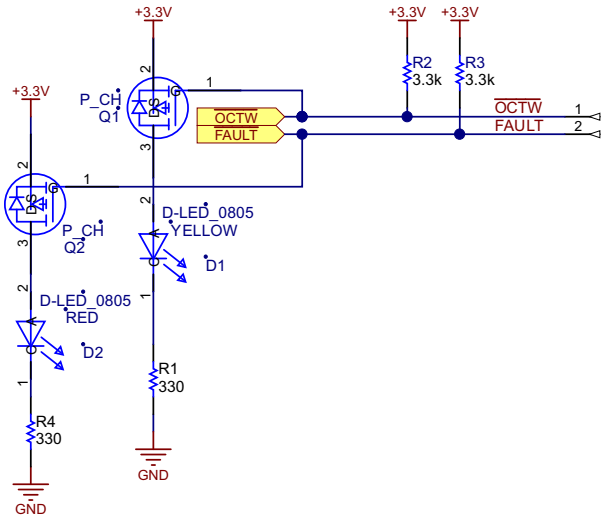


Figure 14. Fault Indication Through LED

Table 3. Fault Events Reporting from DRV8303

REPORTING PIN	FAULT EVENTS
$\overline{\text{FAULT}}$	PVDD Undervoltage
	DVDD undervoltage
	GVDD undervoltage
	GVDD overvoltage
	OTSD_GATE — Gate driver latched shut down
	External FET Overload — Latch mode
$\overline{\text{OCTW}}$	OTW — Over temperature
	OTSD_GATE — Gate driver latched shut down
	External FET Overload — Current limit mode
	External FET Overload — Latch mode
	External FET Overload — Reporting only mode

7 Getting Started Firmware

The InstaSPIN-FOC is selected as it is easy to work with motors with unknown parameters. The MCU firmware for C2000 Piccolo LaunchPad is taken from MotorWare™ software. MotorWare contains the required projects and libraries to use TI's InstaSPIN-FOC technology. MotorWare can be downloaded from http://www.ti.com/tool/motorware.

This design is compatible with "boostxldrv8301_revB" hardware and has the same pin configurations. Therefore, for Code Composer Studio™ (CCS) projects, use the projects under "boostxldrv8301_revB". After installing MotorWare, the projects can be located in this folder location: \motorware\motorware_1_01_00_13\sw\solutions\InstaSPIN_foc\boards\boostxldrv8301_revB\f28x\f2802xF\projects\ccs5

The projects are arranged in a series of labs. Lab9 implements a speed controller to perform the load test of the board. However, as a perquisite to this, Lab2c and Lab5a are run to tune the firmware for the reference design board and the motor. The following mentions the flow used to setup the firmware:

- Lab2c is used to obtain the motor resistance, inductance and board offsets.
- Lab5a is used to tune the PI controller of the current loop.
- Lab9 is used for the load test.

The detailed procedure to build and run the lab is given in *InstaSPIN Projects and Labs User's Guide* provided inside MotorWare.

7.1 Modifying user.h

InstaSPIN-FOC libraries use a global header file user.h, which contains many important parameters used in InstaSPIN-FOC. Some of these parameters values are dependent on the board and motor. Table 4 lists the parameters that need to be changed to make the firmware compatible with the reference design.

Table 4. Parameters in user.h to Tune Based on Motor and Board

PARAMETER	VALUE	COMMENT
USER_IQ_FULL_SCALE_FREQ_Hz	800	> (Maximum RPM × Poles) / 120
USER_IQ_FULL_SCALE_VOLTAGE_V	48	See Section 6.6
USER_ADC_FULL_SCALE_VOLTAGE_V	55.5	See Section 6.6
USER_IQ_FULL_SCALE_CURRENT_A	85	See Section 6.5
USER_ADC_FULL_SCALE_CURRENT_A	165	See Section 6.5
USER_NUM_CURRENT_SENSORS	3	Number of current sensors
I_A_offset I_B_offset I_C_offset	0.521301746 0.523253679 0.50654459	In Lab2c, the offset is computed and stored in user.h for use in other labs.
V_A_offset	0.44593966	In Lab2c, the offset is computed and stored in user.h for use in other labs.
V_B_offset	0.447788179	
V_C_offset	0.442513049	
USER_PWM_FREQ_kHz	60.0	For Lab2c, identification is done using higher PWM frequency of 60 kHz as it helps identifying low inductance motors.
USER_VOLTAGE_FILTER_POLE_Hz	769.164	See Section 6.5
USER_MOTOR_TYPE	MOTOR_Type_Pm	Motor type — Permanent magnet motors
USER_MOTOR_NUM_POLE_PAIRS	8	Number of pole pairs in the motor
USER_MOTOR_Rr	NULL	Not applicable for PMSM
USER_MOTOR_Rs	0.006022509	Values obtained from Lab2c identification.
USER_MOTOR_Ls_d	3.79984E-05	Identified motor phase to neutral resistance is 60 mΩ and average stator inductance is 38 µH.
USER_MOTOR_Ls_q	3.79984E-05	
USER_MOTOR_RATED_FLUX	0.05358878	
USER_MOTOR_MAGNETIZING_CURRENT	NULL	Not applicable for PMSM
USER_MOTOR_RES_EST_CURRENT	5	Maximum current used for Rs estimation in motor identification. Use 10 to 20% of rated current.
USER_MOTOR_IND_EST	–5	Maximum current (negative Amperes, float) used for Ls estimation, use just enough to enable rotation.
USER_MOTOR_MAX_CURRENT	80	Sets a limit on the maximum current command output of the provided speed PI controller to the I_Q controller, used during identification and run-time.
USER_MOTOR_FLUX_EST_FREQ_Hz	20	Default value is 20 Hz, but this can be increased to get a better estimation values in Lab2c.

7.2 Configuring DRV8303 Registers

The InstaSPIN-FOC project sets up registers in the DRV8303 using the SPI peripheral TMS320F2027. The InstaSPIN-FOC projects use two source files by name drv8301.h and drv8301.c for configuring DRV8303. These files contains the DRV8303 register details and function to read and write to DRV8303 using the SPI peripheral. Project uses DRV8301_setupSpi function to initialize the DRV8303 at start up. The control register configuration for DRV8303 is given below.

```
// Update Control Register 1
drvRegName  =     DRV8301_RegName_Control_1;
drvDataNew  =     (DRV8301_PeakCurrent_0p70_A       | \
                  DRV8301_Reset_Normal              | \
                  DRV8301_PwmMode_Six_Inputs        | \
                  DRV8301_OcMode_CurrentLimit       | \
                  DRV8301_VdsLevel_1p043_V);
// Update Control Register 2
drvRegName  =     DRV8301_RegName_Control_2;
drvDataNew  =     (DRV8301_OcTwMode_Both            | \
                  DRV8301_ShuntAmpGain_20VpV        | \
                  DRV8301_DcCalMode_Ch1_Load        | \
                  DRV8301_DcCalMode_Ch2_Load        | \
                  DRV8301_OcOffTimeMode_Normal);
```

Refer to the DRV8303 datasheet to see the full list of the setup options available (SLOS846).

8 Test Results

Figure 15 and Figure 16 show the top and bottom view of the assembled board. Note from the bottom view that a copper wire is soldered into the mask opening to carry the high current. The test results are divided in two sections that cover the functional test results and load test results.

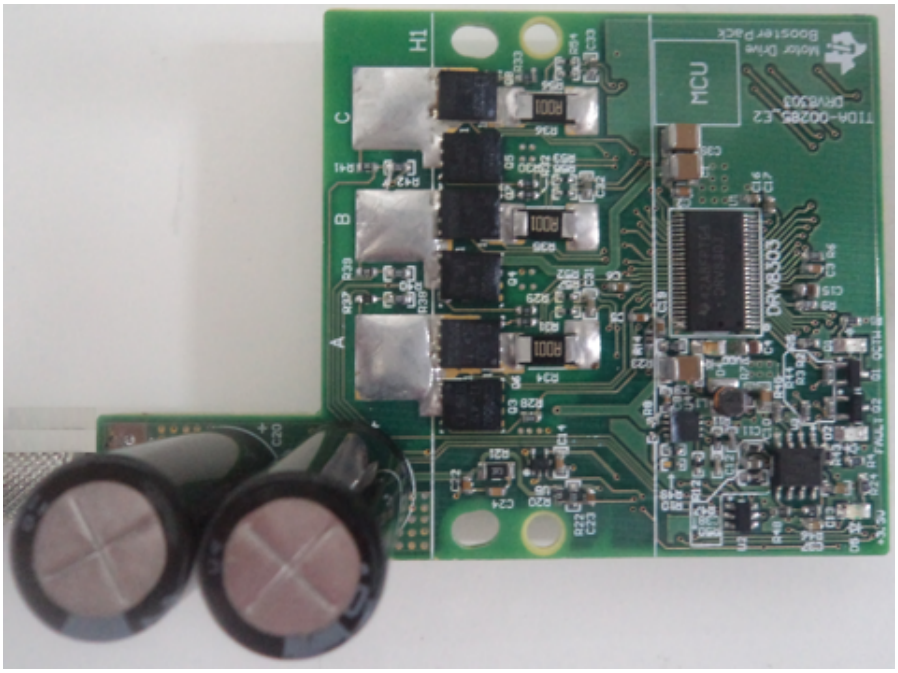


Figure 15. Assembled Power Stage — Top View

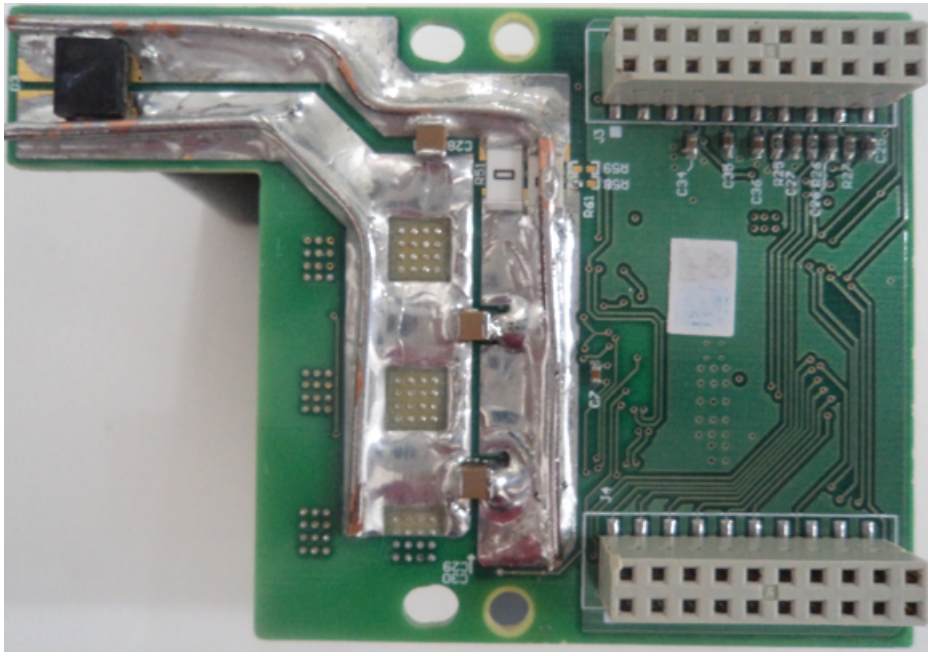


Figure 16. Assembled Power Stage — Bottom View

8.1 Functional Tests

Figure 17 shows the 3.3 V generated from the TPS54061 step-down converter. The ripple in the 3.3-V rail is shown in Figure 18.

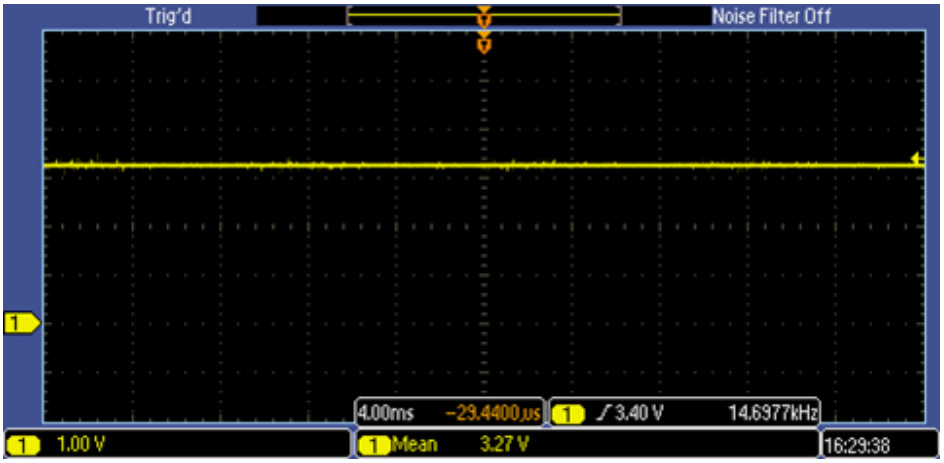


Figure 17. Output Voltage of 3.3 V from Step-Down Converter

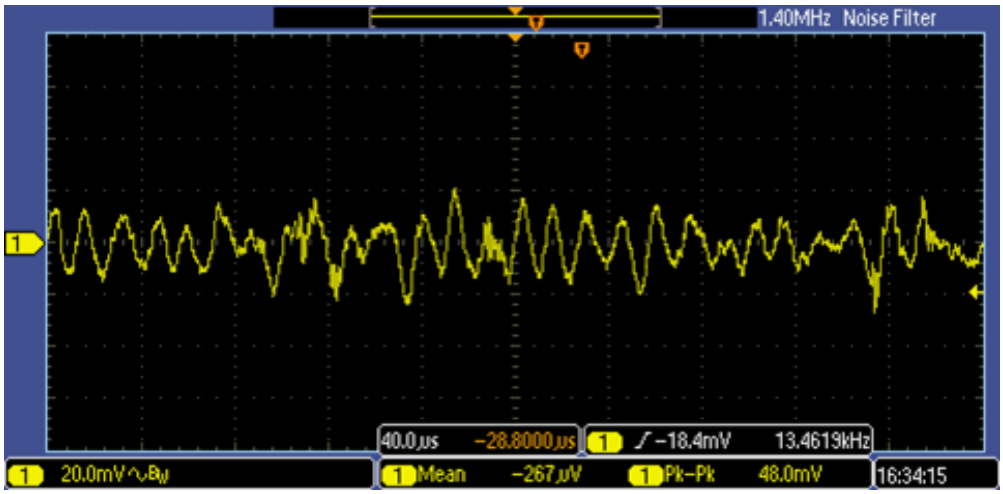


Figure 18. Ripple in 3.3-V Output from Step-Down Converter

The internal voltage regulator of the DRV8303 produces different regulated voltages. The DRV8303 generates GVDD, AVDD, and DVDD for the operation of the internal circuits of the DRV8303. Figure 19 shows the GVDD voltage of DRV8303 and the voltage ripple in GVDD is shown in Figure 20. The mean voltage at the GVDD is observed to be 10.8 V, well above the undervoltage rating (7.5 V). The GVDD ripple is like a saw tooth wave for a FOC algorithm. This ripple waveform is expected as GVDD supplies the bootstrap capacitor for high side and also gate charge for bottom side.

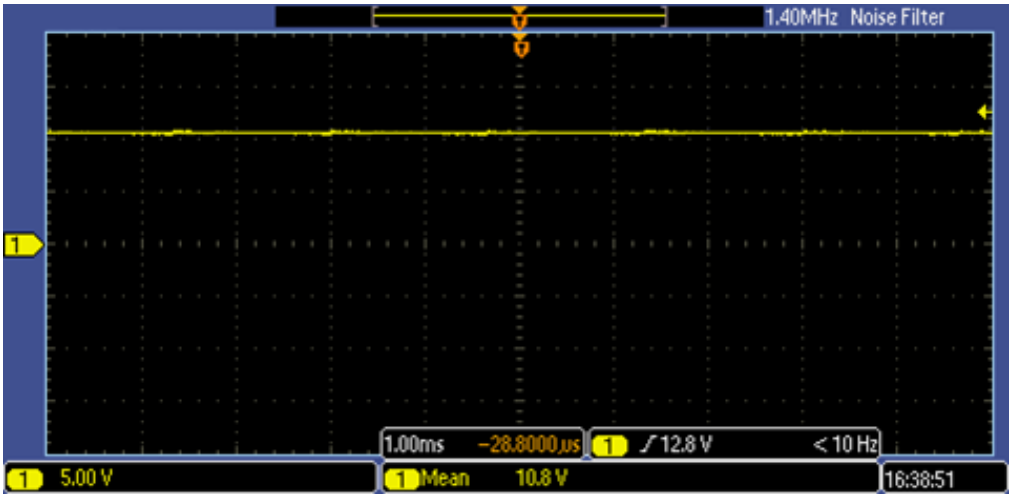


Figure 19. Voltage at GVDD Pin of DRV8303

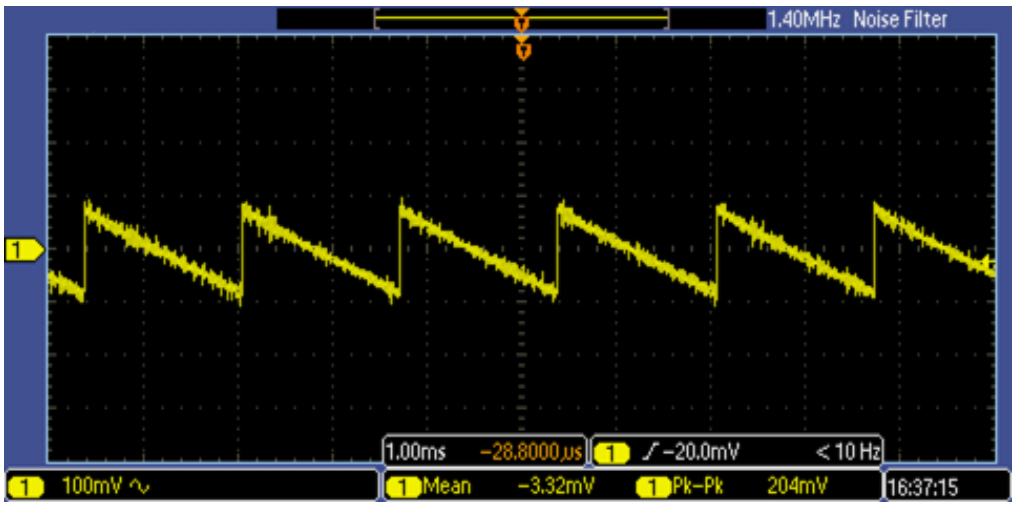


Figure 20. Ripple at GVDD Pin Voltage of DRV8303

Figure 21 shows the voltage output at the DVDD pin of the DRV8303, and the ripple in DVDD rail is shown in Figure 22.

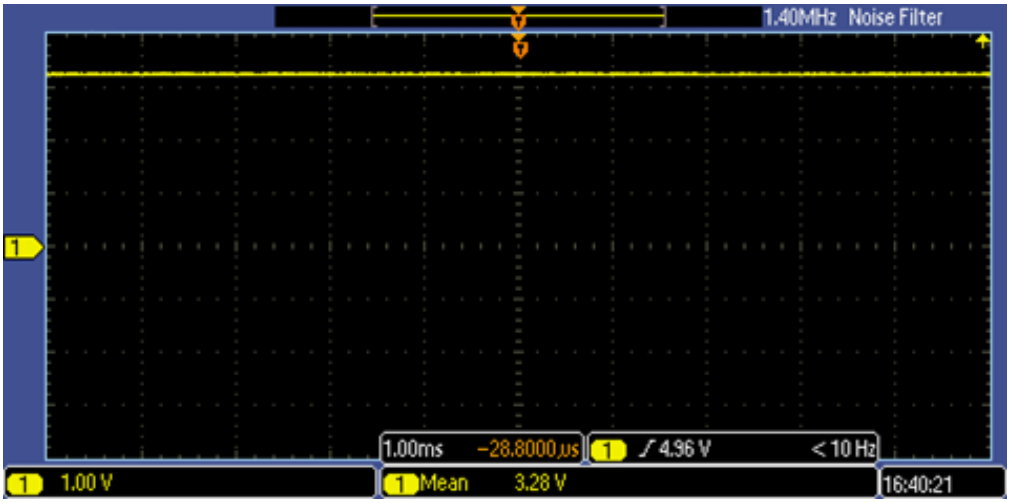


Figure 21. Voltage at DVDD Pin of DRV8303

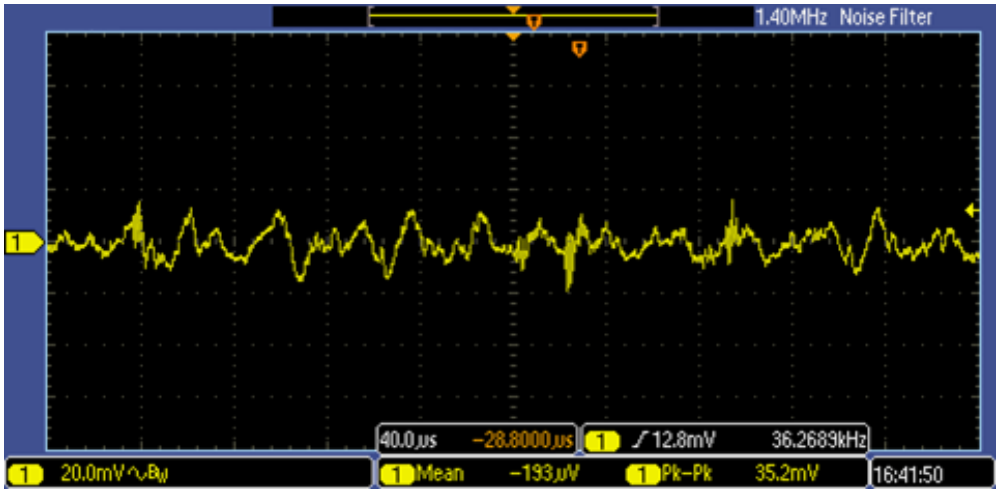


Figure 22. Ripple at DVDD Pin Voltage of DRV8303

Figure 23 shows the voltage output at the AVDD pin of DRV8303, and Figure 24 shows the ripple in AVDD voltage rail. The mean voltage available at the AVDD pin is 6.64 V.

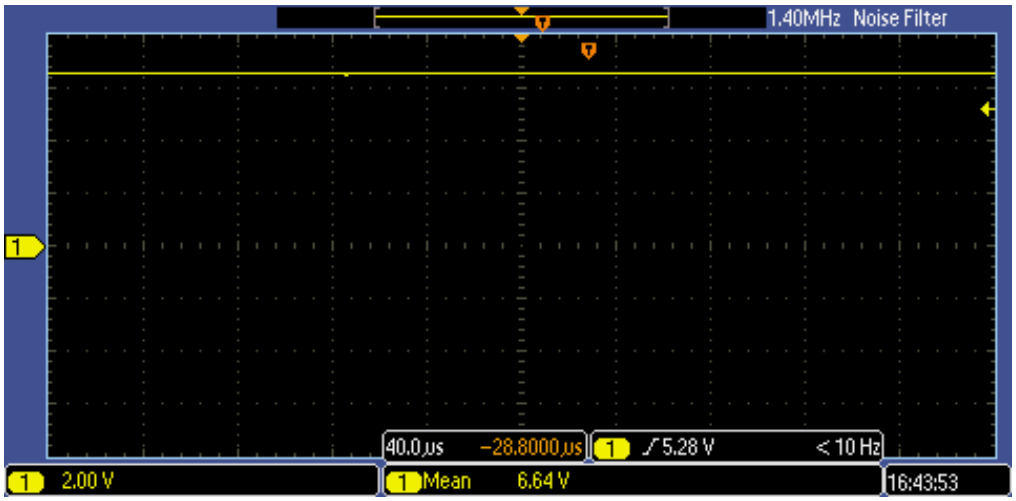


Figure 23. Voltage at AVDD Pin of DRV8303

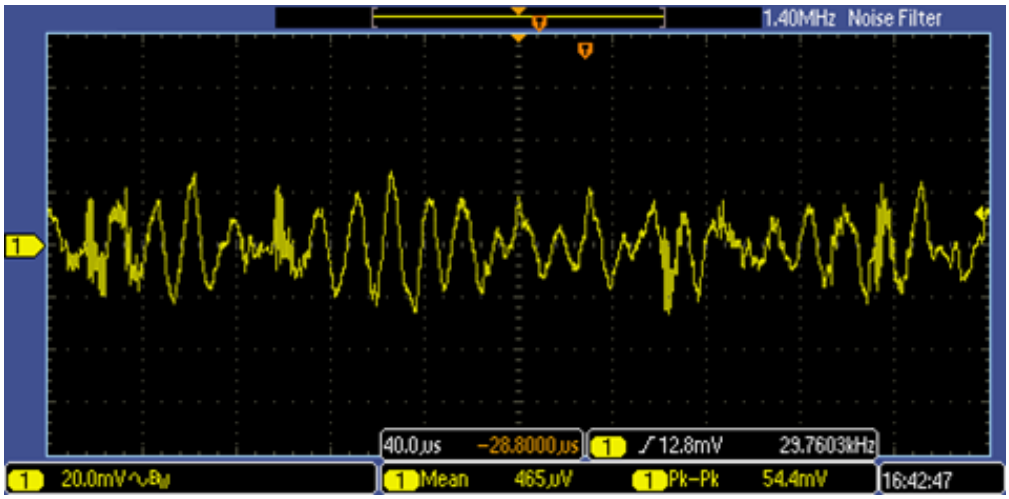


Figure 24. Ripple at AVDD Pin Voltage of DRV8303

The PWM signals generated from the C2000 controller LaunchPad are fed to the DRV8303 gate driver. A switching frequency of 60 kHz is used in the power stage inverter. Figure 25 shows the gate-source voltage for one of the lower MOSFET from the output of the DRV8303 and the corresponding input of DRV8303 coming from the C2000 LaunchPad.

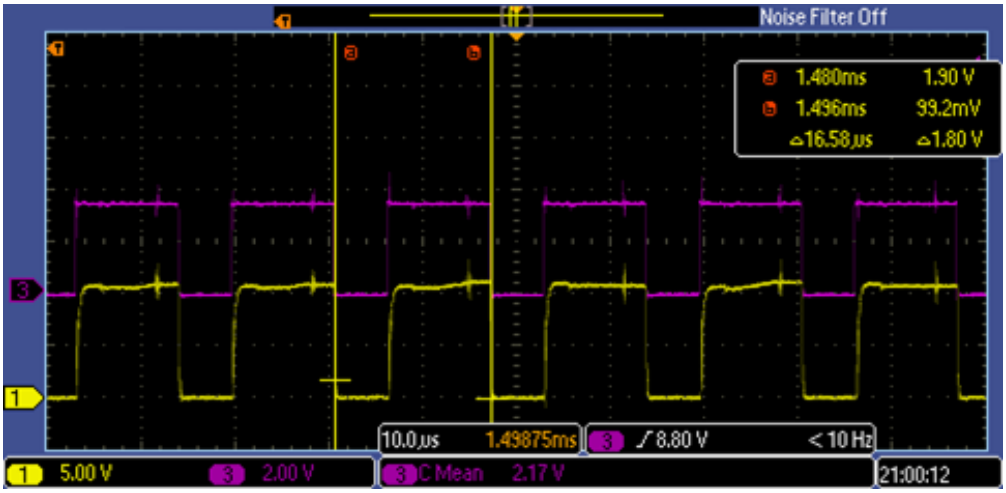


Figure 25. Low-Side PWM Input and Output of DRV8303

Figure 26 shows the complimentary PWM gate signal from the DRV8303 for one leg of the inverter. (Both the top side bottom side waveforms are measured with same ground reference.) Figure 27 and Figure 28 show the dead time inserted by the DRV8303 at the falling edge and rising edge of the PWMs.

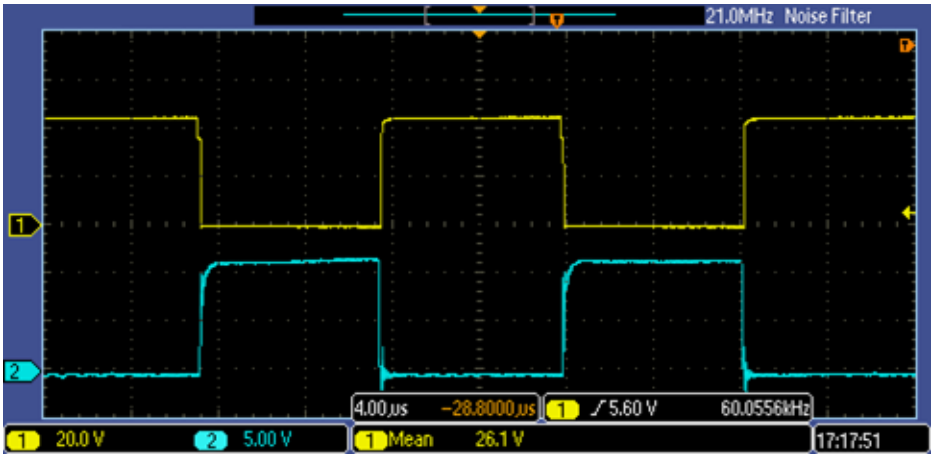


Figure 26. Complimentary PWM Gate Signal from DRV8303

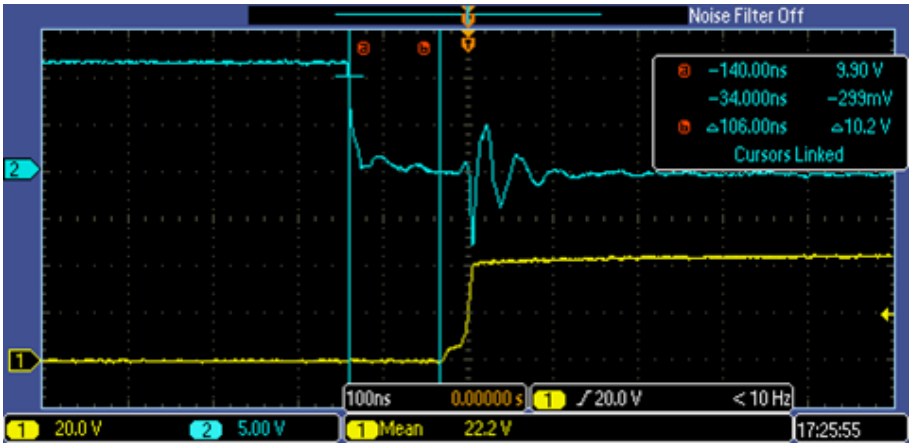


Figure 27. Dead Time Inserted by DRV8303 Measured at Falling Edge of Lower FET PWM

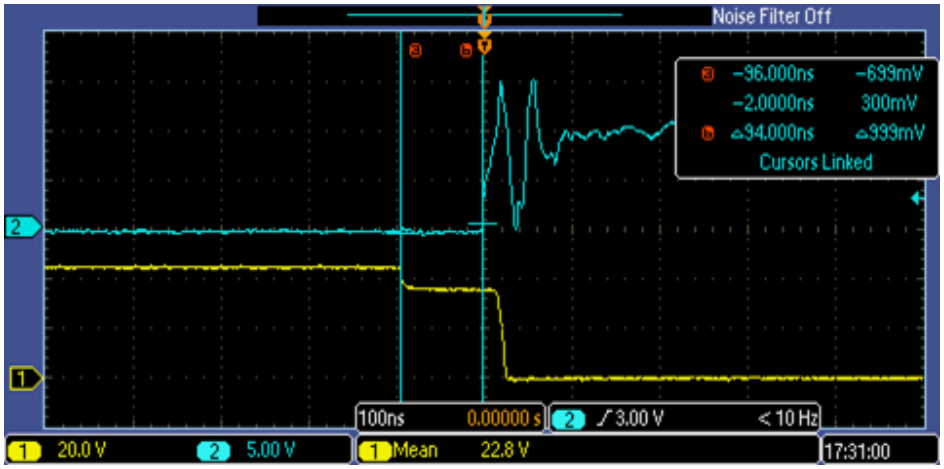


Figure 28. Dead Time Inserted by DRV8303 Measured at Rising Edge of Lower FET PWM

Figure 29 shows the phase-to-phase voltage at motor winding terminals, which is the switching voltage as per the space vector PWM from the C2000 LaunchPad. Figure 30 shows the motor line-to-line voltage filtered by the oscilloscope.

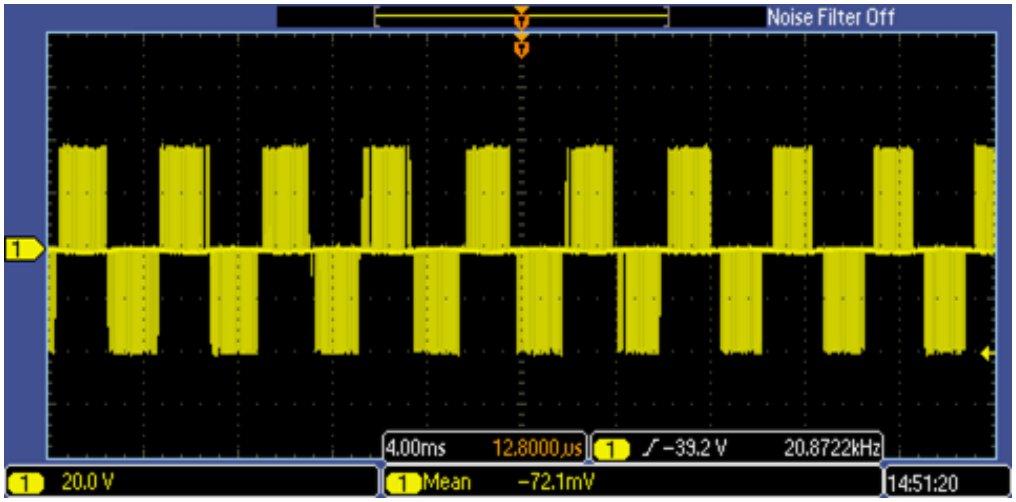


Figure 29. Phase-to-Phase Voltage at Motor Winding Terminals

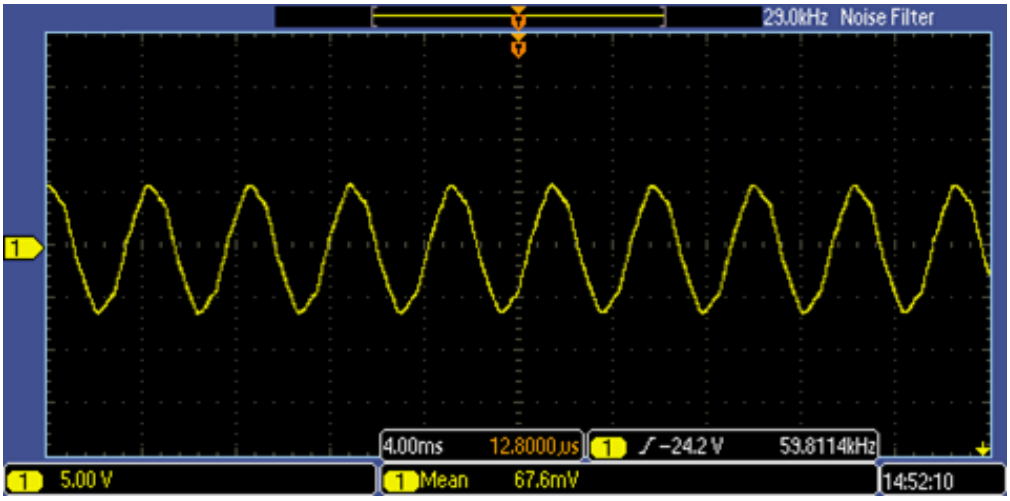


Figure 30. Phase-to-Phase Voltage at Motor Winding Terminals (Filtered View from Oscilloscope)

8.2 Load Tests

The load test determines the thermal characteristics and the current handling capability of the power stage. Figure 31 shows the block diagram of the test setup used for load testing.

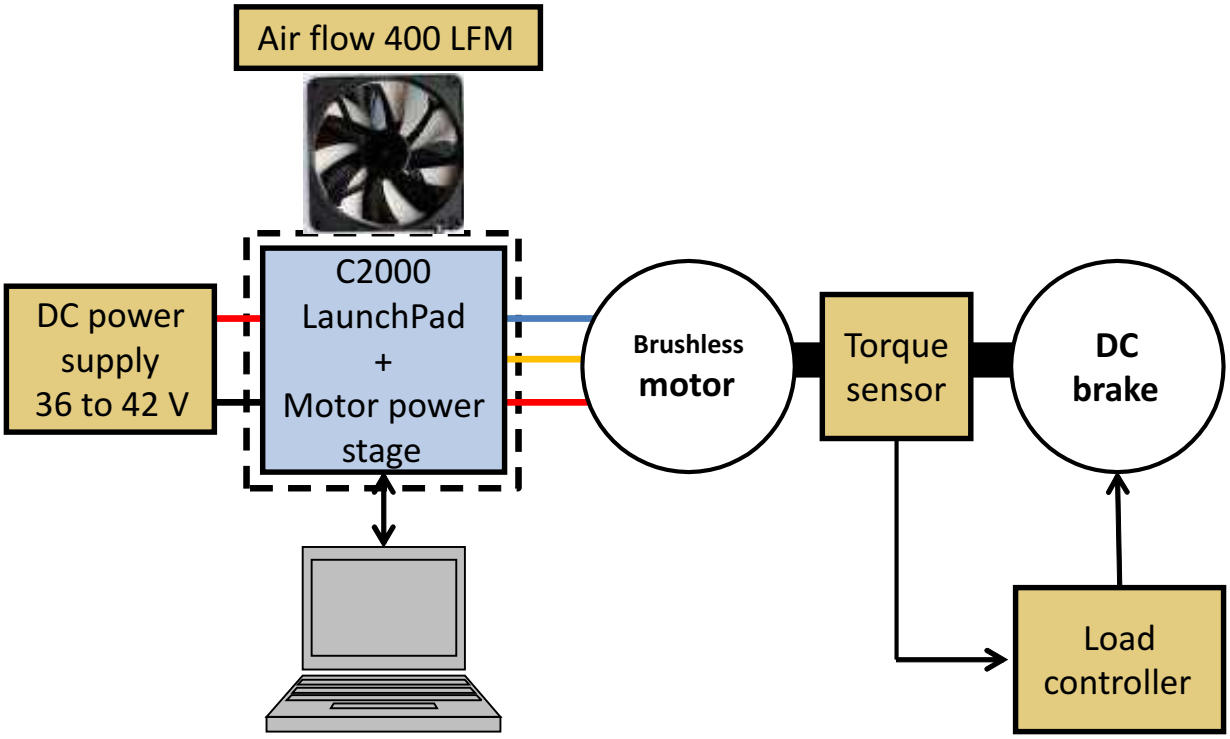


Figure 31. Block Diagram of Load Test Setup

The motor shaft is connected to a DC brake. A motor rated to deliver a shaft torque of 6 Nm at 3000 RPM is used for testing. The loading on the brushless motor is done by means of the DC brake controlled by the load controller. The torque sensor provides the shaft torque feedback to the load controller so that the shaft torque can be adjusted by the torque controller. The load setup measures torque and speed of the motor. The load testing was done by running the motor at a constant speed. The firmware on the C2000 LaunchPad is running Lab9 of the InstaSPIN-FOC projects, which is a closed loop speed control. The speed can be commanded while CCS is connected to the C2000 LaunchPad. A constant torque is applied on the motor shaft using the load controller. The measured values are motor speed, motor shaft torque, RMS and peak value of motor winding current, DC link voltage, and DC link current. The board temperature was measured using a thermal imager.

Figure 32 shows the top view and Figure 33 shows the bottom view of the assembled board with the input DC connection leads and three-phase motor connections. To enable the PCB to carry currents of 40 A, follow these PCB fabrication and assembly processes:

- The power stage is made of a four-layer PCB with 2-Oz copper thickness in all layers. There are wide power and ground return tracks provided in all layers (Refer to the PCB fabrication images in Section 10.3).
- The power tracks on the bottom side of the PCB have external copper filling to enable high current carrying capacity.

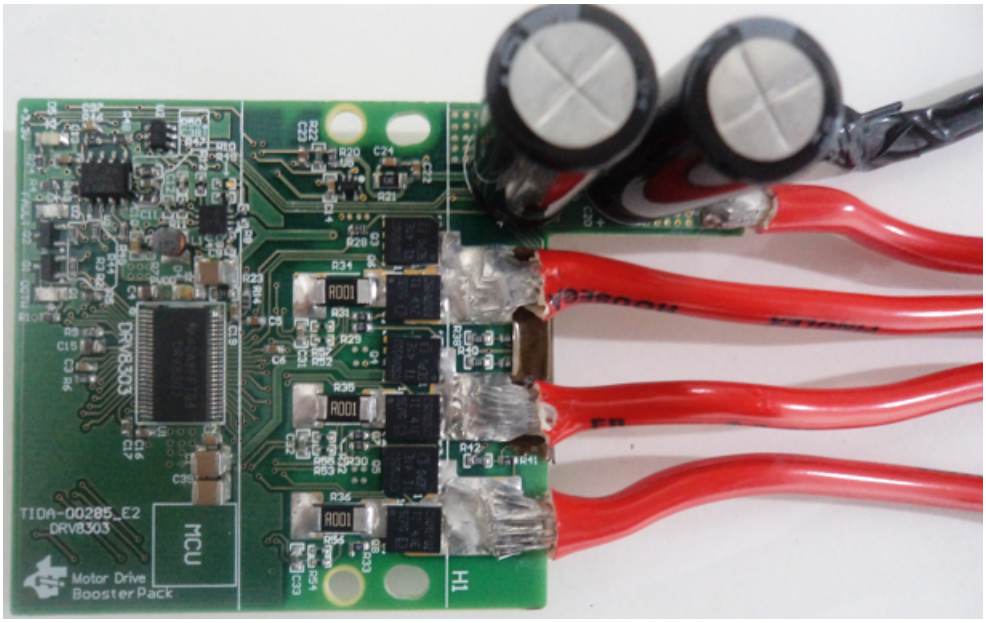


Figure 32. Assembled Power Stage With Power Connections — Top View

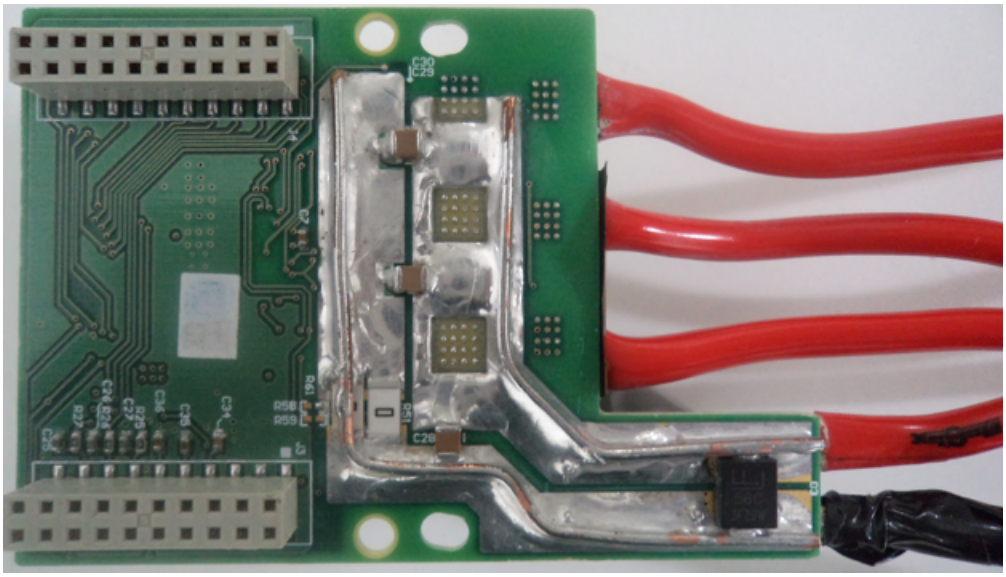


Figure 33. Assembled Power Stage With Power Connections — Bottom View

Figure 34 shows the heat sink mounting on the PCB. The heat sink is mounted on the top side of the MOSFETs. The thermally conductive pad is used between the PCB and the heat sink flat surface to provide electrical insulation. It is important to select a thermal pad with high thermal conductivity. The selected heat sink has a thermal resistance of 1.74°C/W at airflow of 2 m/s.

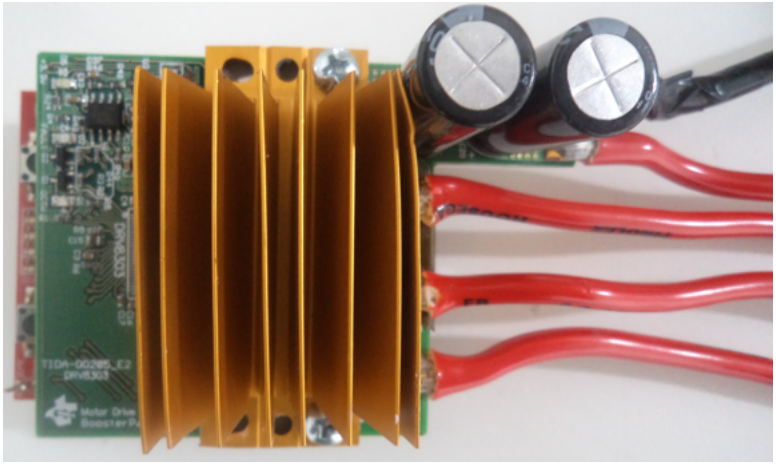


Figure 34. Assembled Power Stage With Heat Sink Mounting

Figure 35 shows the enclosure setup to provide airflow to the power stage. The cooling fan is selected to provide a 400-LFM airflow to the board. The airflow is measured using an anemometer.

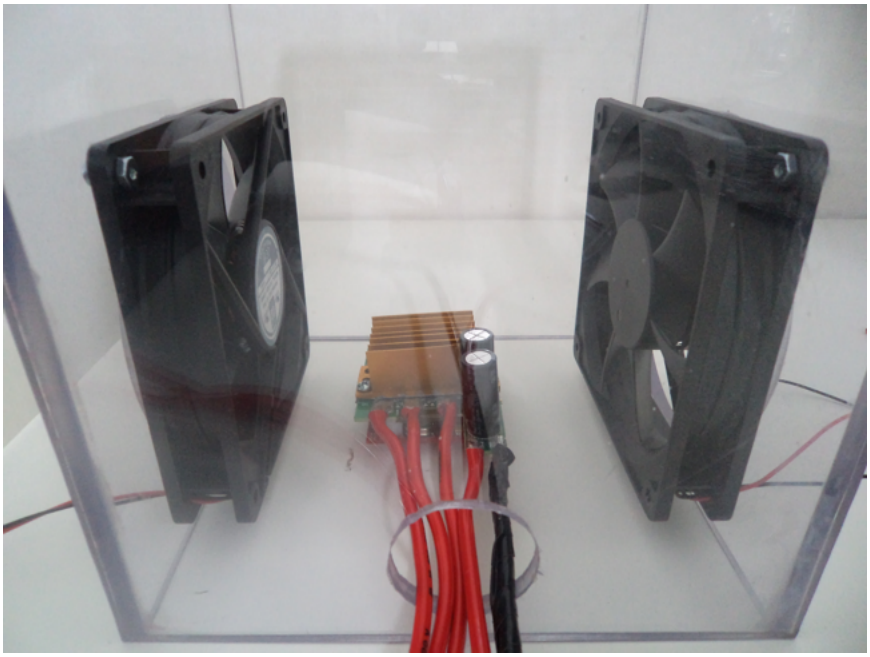


Figure 35. Test Setup to Provide Airflow to Power Stage

The results of the load test conducted at an input DC voltage of 36 V and winding current of 29.2 A_{RMS} is given in Table 5. The input power to the board is 1080 kW.

Table 5. Load Test Results at 36-V Input Voltage and 29.2-A_{RMS} Winding Current

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	PEAK WINDING CURRENT (A)	HEAT SINK TEMPERATURE (°C)	MAXIMUM PCB TEMPERATURE (°C)
36	30	29.2	42.4	46	63.6

Figure 36 shows the motor winding current and Figure 37 shows the thermal image of the board at this load of 29.2 A_{RMS}. Note that the heat sink temperature at this power level is 46°C. The maximum temperature captured by the thermal imager is 63.6°C and is observed on the copper pad near the MOSFET. The MOSFET temperature, which was not visible in the thermal imager, would be slightly more than the PCB copper pad temperature.

NOTE: All the temperature mentioned in the document is absolute temperature. All the tests are done at an ambient temperature of 25°C.

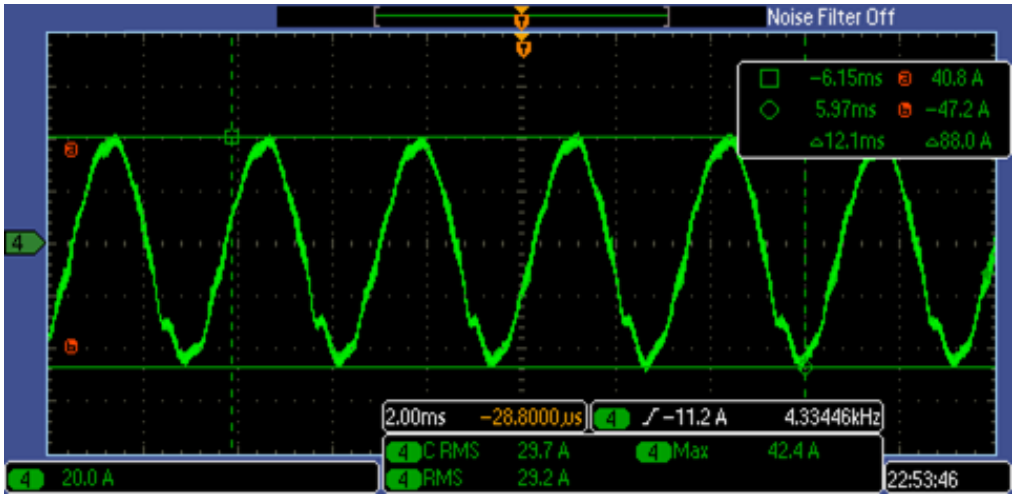


Figure 36. Load Test at 36 V — Winding Current Waveform (29.2 A_{RMS})

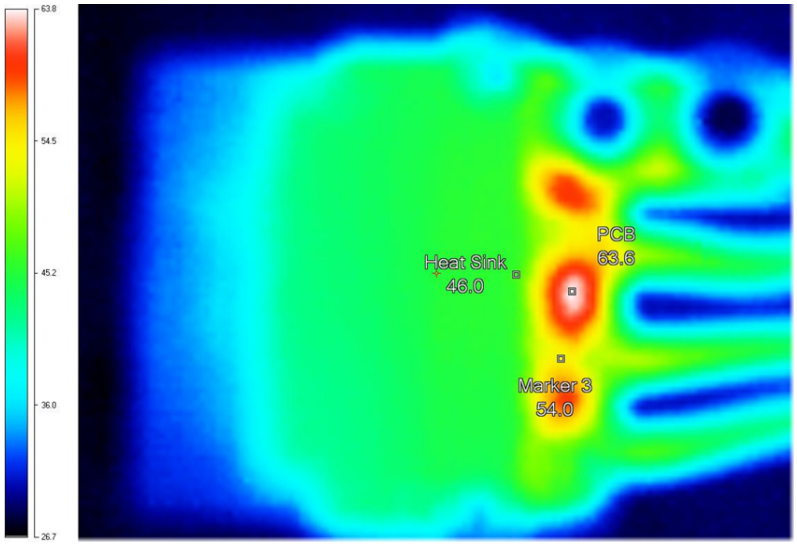


Figure 37. Load Test at 36 V — Thermal Image of Board at Winding Current of 29.2 A_{RMS}

The load test results at an input voltage of 36 V and winding current of 37.3 A_{RMS} is given in Table 6.

Table 6. Load Test Results at Input Voltage of 36 V and Winding Current of 37.3 A_{RMS}

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	PEAK WINDING CURRENT (A)	HEAT SINK TEMPERATURE (°C)	MAXIMUM PCB TEMPERATURE (°C)
36	38	37.3	54.4	60.8	88.3

Figure 38 shows the motor winding current and Figure 39 shows the thermal image of the board at this load of 37.3 A_{RMS}. The measured heat sink temperature at this power level is 60.8°C. The maximum PCB temperature of 88.3°C is observed on the on the copper pad near the MOSFET.

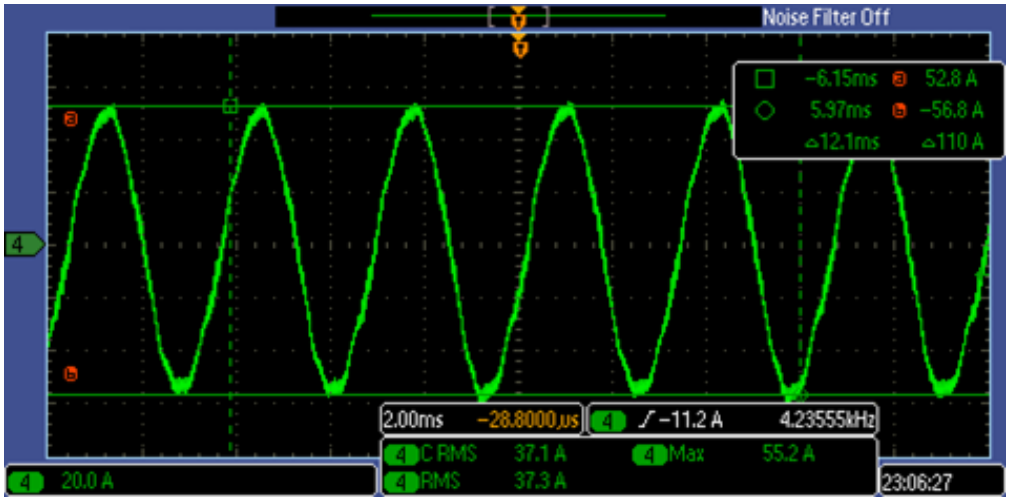


Figure 38. of Load Test at 36 V — Winding Current Waveform (37.3 A_{RMS})

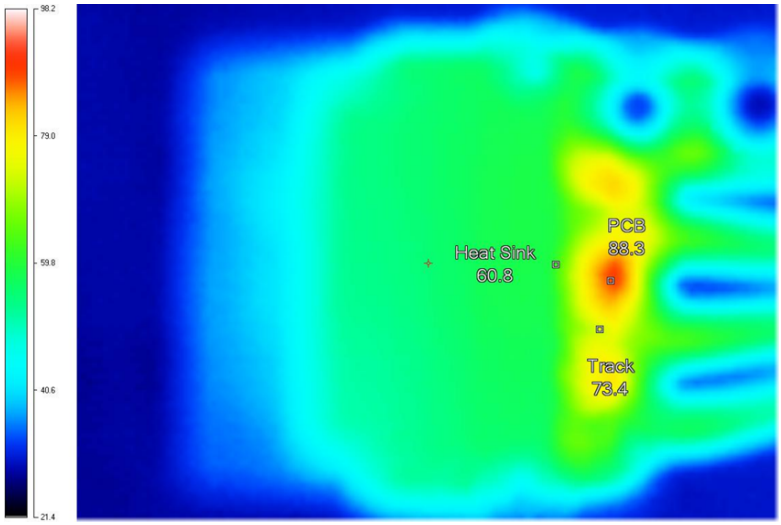


Figure 39. Load Test at 36 V — Thermal Image of Board at Winding Current of 37.3 A_{RMS}

The power stage is tested at an input DC voltage of 42 V and one set of observations at a winding current of 23.4 A_{RMS} is given in Table 7.

Table 7. Load Test Results at Input Voltage of 42 V and Winding Current of 23.4 A_{RMS}

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	PEAK WINDING CURRENT (A)	HEAT SINK TEMPERATURE (°C)	MAXIMUM PCB TEMPERATURE (°C)
42	22	23.4	36	37.5	53.4

Figure 40 shows the motor winding current and Figure 41 shows the thermal image of the board. The heat sink temperature is 37.5°C. The maximum PCB temperature of 53.4°C is observed on the on the copper pad near the MOSFET.

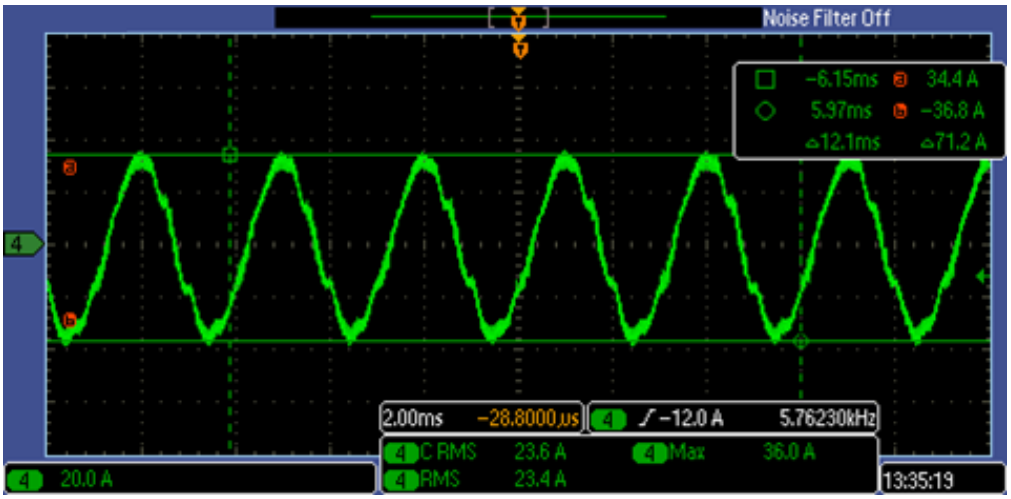


Figure 40. Load Test at 42 V — Winding Current Waveform (23.4 A_{RMS})

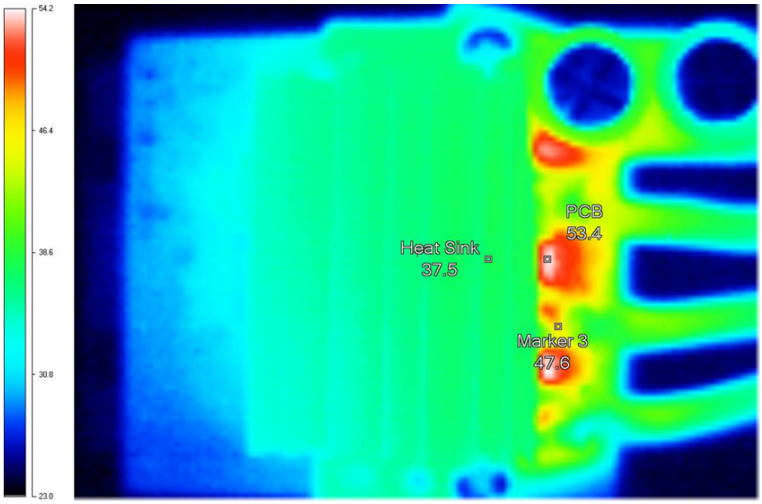


Figure 41. Load Test at 42 V — Thermal Image of Board at Winding Current of 23.4 A_{RMS}

The complete load test results at 36 V and at a motor speed of 2300 RPM is given in Table 8. The load test results at 42 V and at a motor speed of 2500 RPM is tabulated in Table 9.

Table 8. Load Test Results at Input Voltage of 36-V DC and 2300 RPM

INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	PEAK WINDING CURRENT (A)	MOTOR SHAFT TORQUE (Nm)	MOTOR OUTPUT POWER (W)	DC INPUT POWER (W)	MAXIMUM PCB TEMPERATURE (°C)
6.4	6.26	11.6	0	0	230.4	32
10	9.75	16.4	0.55	132.99	360	33
12	11.8	18.8	0.85	205.52	432	35
14.1	13.7	21.6	1.15	277.96	507.6	37
16	15.7	24	1.43	345.68	576	39
18	17.6	26.4	1.72	415.85	648	41
20.1	19.7	28.8	2.02	488.25	723.6	44
22	21.7	32.2	2.3	556.27	792	47
24	23.9	33.6	2.573	621.47	864	51
26	25.9	36	2.86	691.45	936	55
28	27.8	39.2	3.15	761.68	1008	59
30	29.2	42.4	3.4	822.27	1080	64
32	31.2	44.8	3.66	885.12	1152	69
34	33.3	48	3.94	952.88	1224	74
36	35.6	52	4.22	1020.21	1296	81
38	37.3	54.4	4.48	1083.8	1368	89

Table 9. Load Test Results at Input Voltage of 42-V DC and 2500 RPM

INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	PEAK WINDING CURRENT (A)	MOTOR SHAFT TORQUE (Nm)	MOTOR OUTPUT POWER (W)	DC INPUT POWER (W)	MAXIMUM PCB TEMPERATURE (°C)
7.7	7.74	15.2	0	0	323.4	32
10	10.2	18	0.4	104.61	420	33
12.1	12.4	21.2	0.76	198.65	508.2	36
14.1	14.6	24	1.12	293.84	592.2	39
16	16.7	27.2	1.45	379.31	672	42
18.1	18.8	29.6	1.77	469.86	760.2	46
20	21.1	32.8	2.09	546.83	840	50
22	23.4	36	2.42	633.05	924	57
24	25.32	38.6	2.56	726.98	1008	64
26	27.5	41.5	2.87	816.34	1092	74

Figure 42 shows the variation of the maximum temperature observed on the board (by the thermal imager) with the winding current. The maximum temperature is observed on the PCB copper pad near the MOSFET. The MOSFET temperature will be slightly more than the maximum observed temperature (MOSFETs are not visible in the thermal imager due to the heat sink).

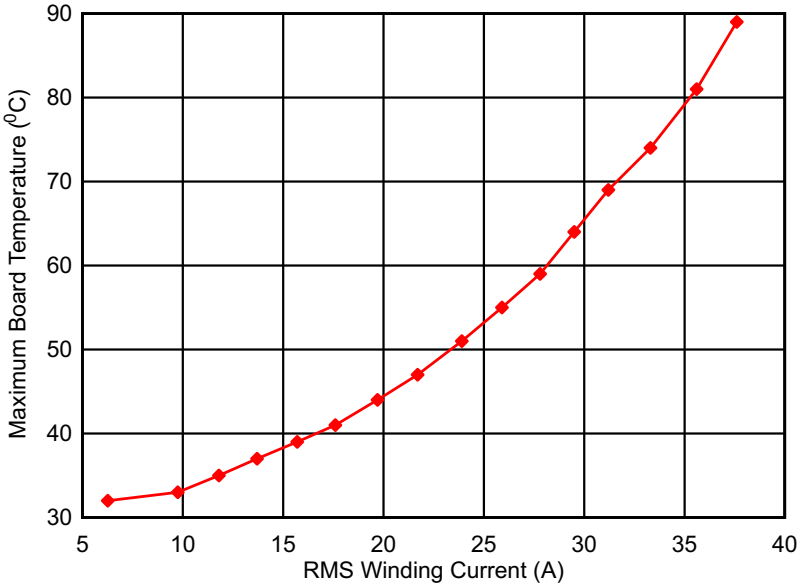


Figure 42. Winding Current versus Maximum Temperature Observed on Board

The design uses CSD18540Q5B rated for 60 V with a R_{DS_ON} of 1.8 mΩ. Alternatively, the thermal performance of the power stage also evaluated with CSD19502Q5B NEXFETs with higher voltage rating and consequently a higher R_{DS_ON}. The FET CSD19502Q5B is rated for 80 V with a R_{DS_ON} of 3.4 mΩ. Both the MOSFETs are available in the SON5x6 package. Figure 43 shows the variation of the maximum temperature observed on the board with the winding current for the two evaluated FETs. The maximum temperature is observed on the PCB copper pad near the MOSFET.

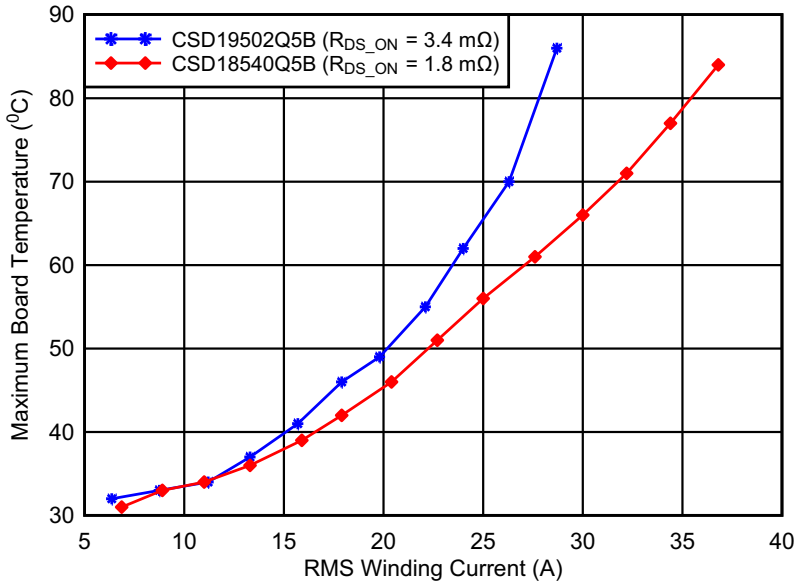


Figure 43. Comparison of Temperature Rise in Power Stage Tested With Two Different MOSFETs

8.3 Overcurrent Protection Test

The current through the motor power stage can exceed the rated value due to motor overload or motor stall condition. The DRV8303 implements an overcurrent protection using the MOSFET V_{DS} sensing. The overload and stall conditions are simulated by using a electronic resistive load. Alternatively, the overload and stall conditions could have been applied mechanically to the motor; in this case, the brake rating should not be exceeded. Therefore, a more practical approach is taken to inject an overload current in the power stage.

A single leg of the power stage is connected to an electronic load and the return current is routed through the power supply negative terminal. The current path during an overload is indicated as the red line in Figure 44. The current flows in the top MOSFET during the test. The C2000 LaunchPad is setup to generate a PWM with a constant duty period of 50% at 60 kHz and the overcurrent and fault response feature of the C2000 LaunchPad is not used.

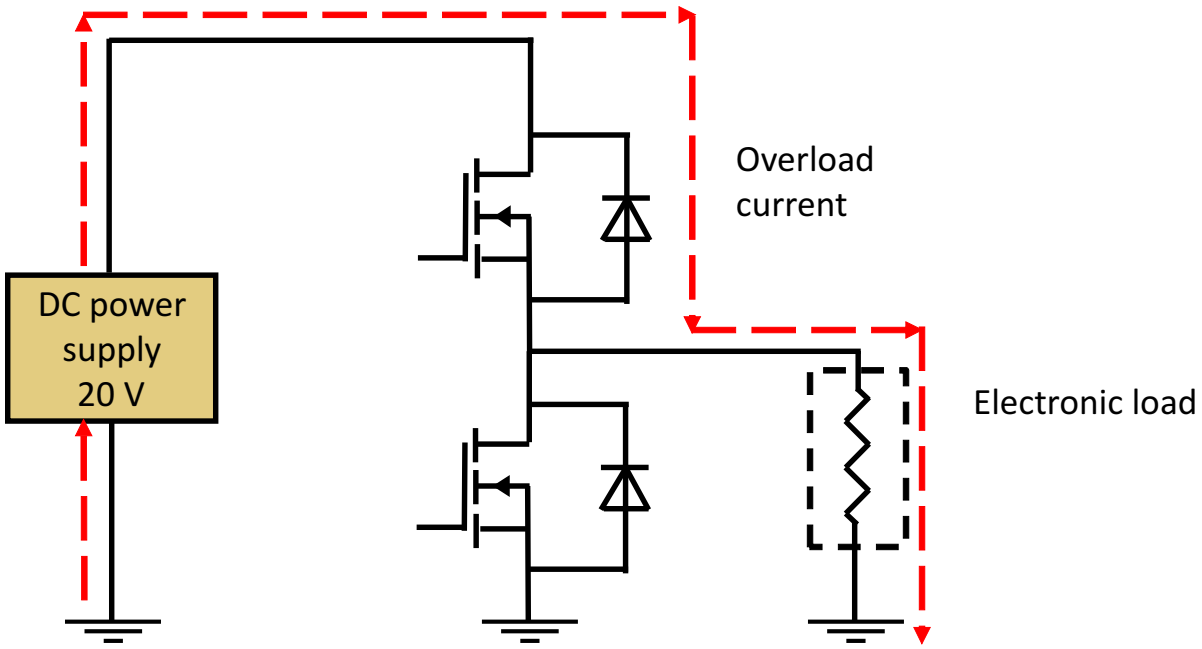


Figure 44. Circuit for Testing Overcurrent Shutdown Feature of DRV8303

The DRV8303 on detecting an overcurrent pulls $\overline{\text{OCTW}}$ pin low. If the DRV8303 is set up to latch mode on overcurrent event, it will hold $\overline{\text{OCTW}}$ pin low until the DRV8303 is reset, and in current limiting mode, the DRV8303 will release the pin from low state in the next PWM toggle or for a period of 64 µs. In the schematic, the transistor Q3 is controlled by $\overline{\text{OCTW}}$, which drives the indicator LED. During the testing, to show the transition of $\overline{\text{OCTW}}$ during fault condition, the transistor Q3 is removed to reduce the transient time from low state to high state. However, this is not a requirement for normal working condition. The on-state V_{DS} of the MOSFET can be calculated by multiplying the drain current by the R_{DS_ON} of the MOSFET. The R_{DS_ON} of the MOSFET is specified in the datasheet. Figure 45 shows the V_{DS} of the MOSFET at a continuous drain current of 10 A.

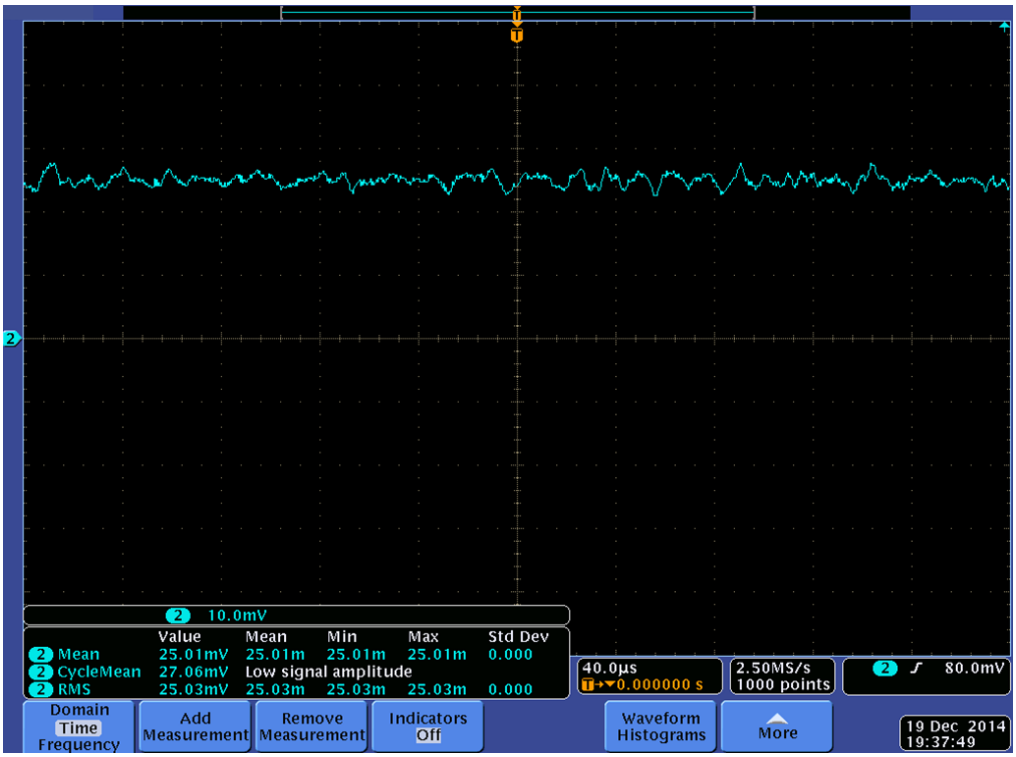


Figure 45. Drain-to-Source Voltage at a Continuous Drain Current of 10 A

The threshold value for V_{DS} sensing is set to 0.175 V. The R_{DS_ON} of the MOSFET is 1.8 mΩ at 25°C. The maximum value of R_{DS_ON} is 2.2 mΩ. The temperature of the MOSFET will cause increase in R_{DS_ON}. The R_{DS_ON} of 2.2 mΩ corresponds to an overcurrent limit of 79.5 A (0.175 / 2.2 = 79.5). The signal monitored on the oscilloscope are $\overline{\text{OCTW}}$ from the DRV8303, the high-side gate output signal from the DRV8303, and the MOSFET current. Figure 46 shows the signals during normal operation of the DRV8303 when load is turned off. Figure 47 shows the CBC overcurrent limit operation of the DRV8303. The $\overline{\text{OCTW}}$ goes low when the MOSFET current touches 76 A. The PWM pulled down immediately and $\overline{\text{OCTW}}$ is holding low during same PWM cycle. The $\overline{\text{OCTW}}$ signal is coming to high state when the PWM input of the DRV8303 for the overcurrent detected MOSFET is toggled.

Figure 46. $\overline{\text{OCTW}}$ Pin Output of DRV8303 During Normal Operation

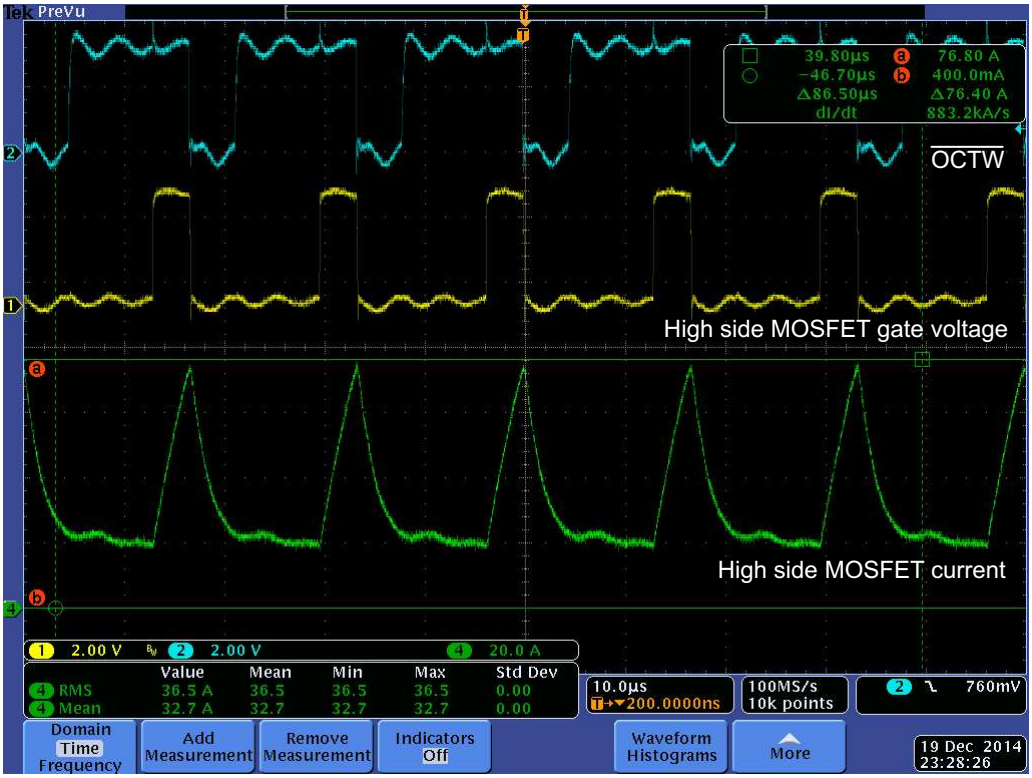


Figure 47. Overcurrent Response of DRV8303 in Current Limiting CBC Mode

Figure 48 shows the overcurrent response of the DRV8303 in latch mode. The open drain output $\overline{\text{OCTW}}$ is held low after the overcurrent detection and resetting the DRV8303 is required for normal operation.

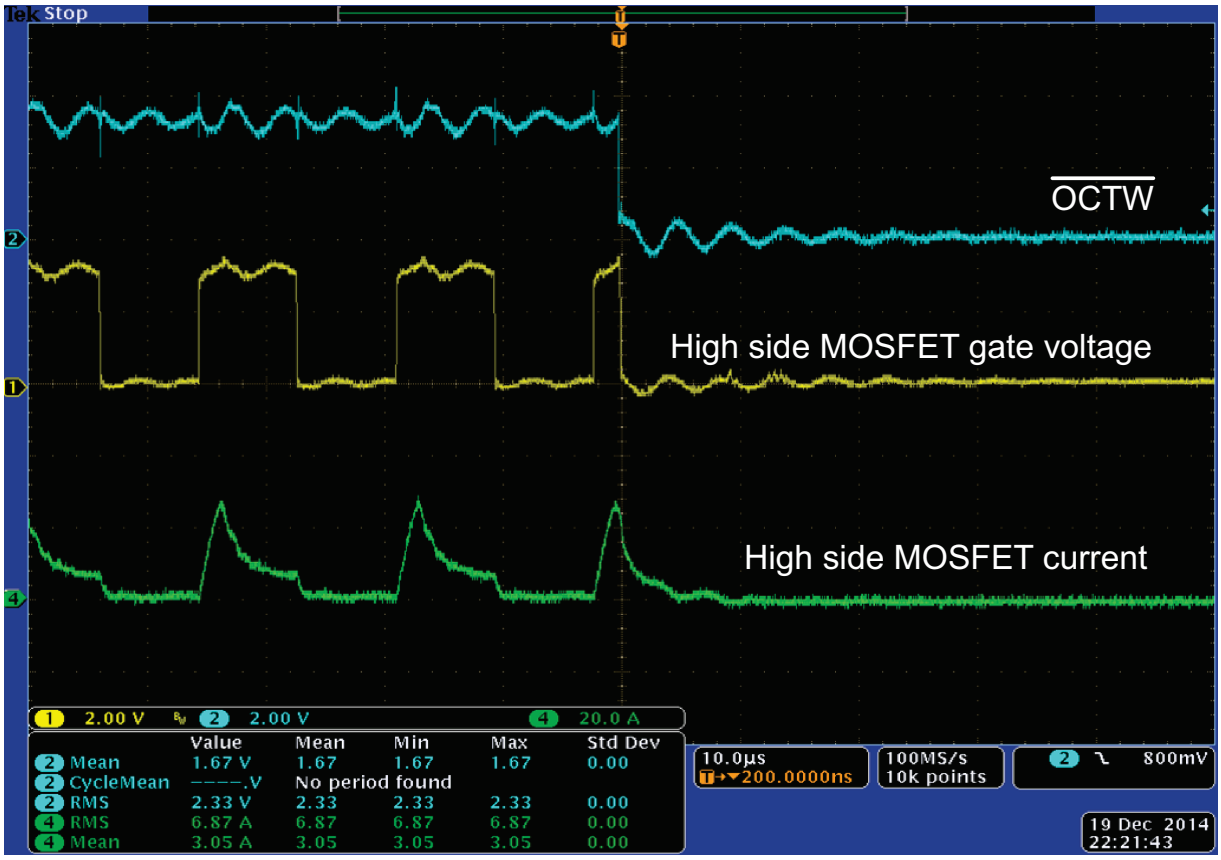


Figure 48. Overcurrent Protection Response by DRV8303 in Latch Mode

9 Using the Power Stage for Trapezoidal Control of BLDC Motors

The BLDC motor is conventionally defined as a permanent magnet motors with a trapezoidal BEMF waveform shape and a PMSM is having a sinusoidal BEMF. Both motor types are synchronous machines. The only difference between them is the shape of the induced voltage.

In BLDC motors, trapezoidal control is used where only two phases are ON at a time and the third phase is open. The phase windings are energized by square wave currents. In PMSM, sinusoidal control is used where all the three phase winding of the motor is ON at a time and the windings are energized by sinusoidal currents. BLDC machines could be driven with sinusoidal currents and PMSM with square wave currents, but for better performance, PMSM should be excited by sinusoidal currents and BLDC machines by square wave currents.

The trapezoidal control is simple and has less switching losses compared to sinusoidal control. The control structure (hardware and software) of a sinusoidal motor requires several current sensors and sinusoidal phase currents, which are hard to achieve with analog techniques. Trapezoidal control has the disadvantage of commutation torque ripple.

To get the best performance out of the permanent magnet motor, identify the type of motor to apply the most appropriate type of control. In this reference design, sinusoidal control (InstaSPIN-FOC) is used to validate the performance of the power stage as the motor used for testing had a sinusoidal BEMF. However, the same power stage can be used to drive a BLDC motor with trapezoidal control using a C2000 controller. The power stage can also support a 30-A_{RMS} phase winding current in trapezoidal control.

9.1 Hardware Modifications Required for Trapezoidal Control

Figure 49 shows the modified block diagram of the power stage for trapezoidal control of three-phase BLDC motors. The hardware modifications required in the board are listed in the Table 10.

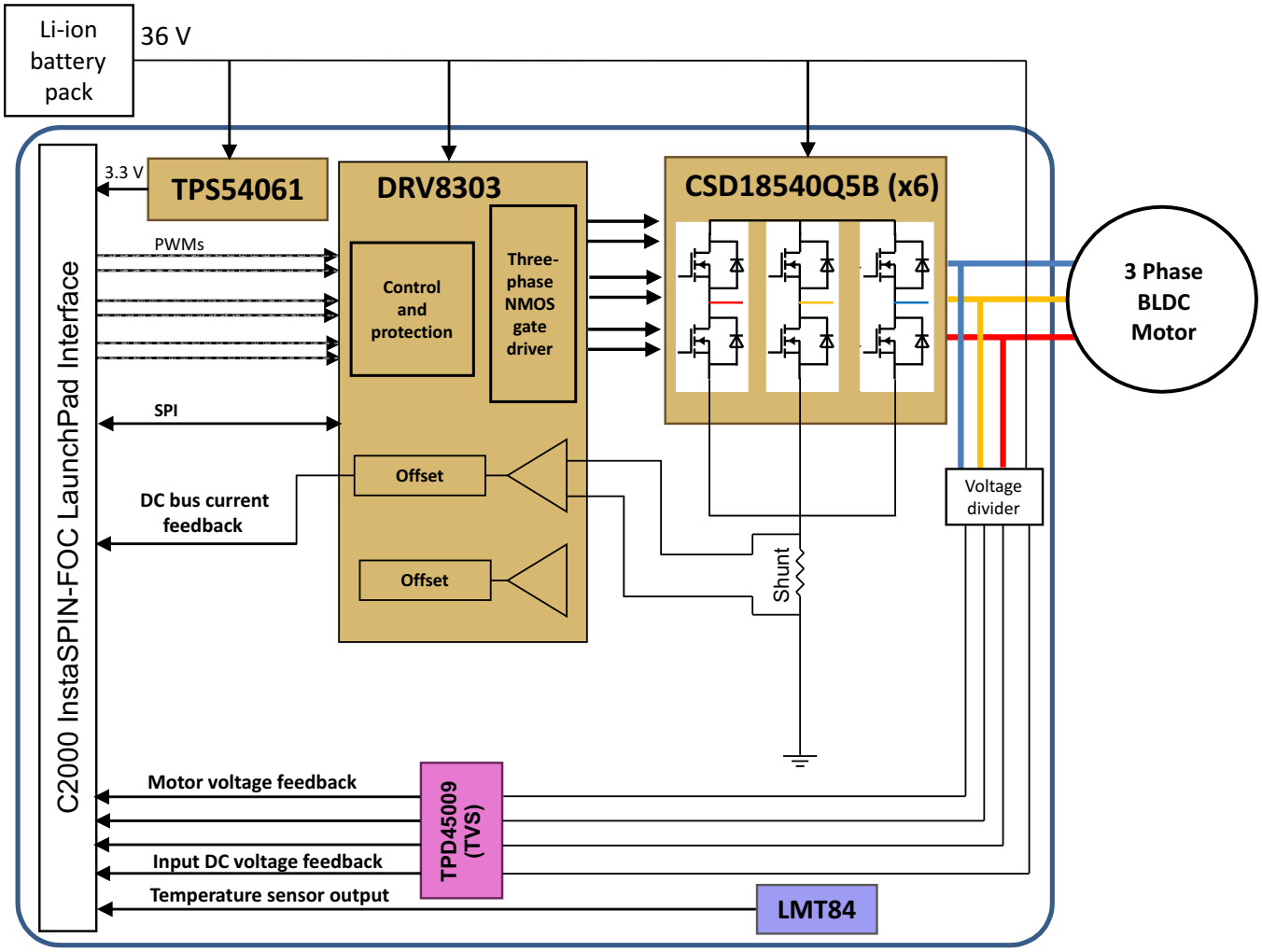


Figure 49. Block Diagram of Power Stage for Trapezoidal Control of Three-Phase BLDC Motors

Table 10. Hardware Modifications Required for Trapezoidal Control

COMPONENTS	MODIFICATION REQUIRED	REMARKS
R34, R35 , R36	Remove and short the pad using 0-Ω resistor.	Shunt resistors in the inverter legs
R52, R53, R54, R55, R56, R57, C32, C33	Do not populate	Filters used in the inverter leg current sensing
R51, R61	• Populate with suitable resistor value (user can start with 1 mΩ) and adjust the gain in DRV8303 current amplifier appropriately. • A shunt resistor of 2-W / 2512 package and 1% tolerance can be selected.	Current sensing resistors in the negative DC bus. The sense resistor and the amplifier gain values can be set such that it activates the integrated overcurrent protection when the maximum current permitted by the power board has been reached.
R58, R59	Populate	Used as a filter with C31

9.2 Software — Trapezoidal Control

The user can use sensor-based or sensorless trapezoidal control. A simplified block diagram of the common control strategy is shown in Figure 50. The control loop has an outer speed loop with an inner current control loop. Also, the control can be a simple speed control loop where the DC bus current sensing is not required.

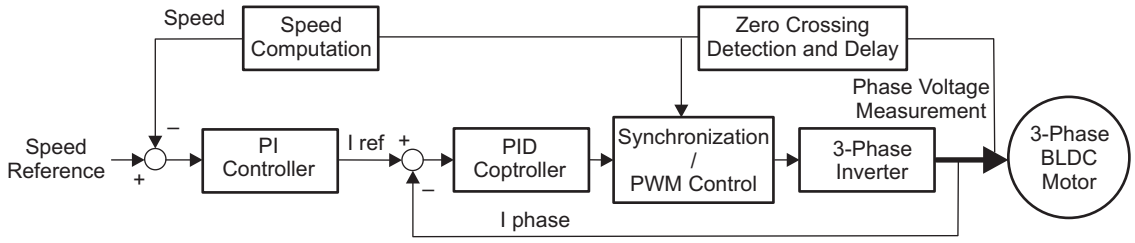


Figure 50. Simplified Block Diagram of Power Stage for Trapezoidal Control of Three-Phase BLDC Motors

In sinusoidal control, all phase currents need to be measured and the control algorithm is complex. A characteristic of the BLDC motor control is to have only one current at a time in the motor (two phases ON). Consequently, it is not necessary to put a current sensor on each phase of the motor; one sensor placed in the line inverter input makes it possible to control the current of each phase. Moreover, using this sensor on the ground line (negative DC bus), insulated systems are not necessary, and a low-cost resistor can be used. Its value is set such that it activates the integrated overcurrent protection when the maximum current permitted by the power board has been reached.

The BLDC motor control consists of generating square wave currents in the motor phases. This control requires stator and rotor flux synchronization and control of the winding current. Both operations are realized through the three-phase inverter depicted in Figure 49. The flux synchronization is derived from the position information coming from sensors, or from sensorless techniques. From the position, the controller determines the appropriate pair of transistors that must be driven. The regulation of the current to a fixed 60° reference can be realized using the PWM. For more details, refer to the BLDC motor application report (SPRABQ7).

NOTE: The placement of the decoupling capacitors is important for the proper functioning of the V_{DS} sensing protection of the DRV8303. Place these capacitors near each MOSFET leg. When the sense resistor is used in the negative DC rail, make sure that the return path of the decoupling capacitors are through a thick track and return path length is as short as possible to improve the decoupling. See Section 10.3 for more details.

10 Design Files

10.1 Schematics

To download the schematics, see the design files at TIDA-00285.

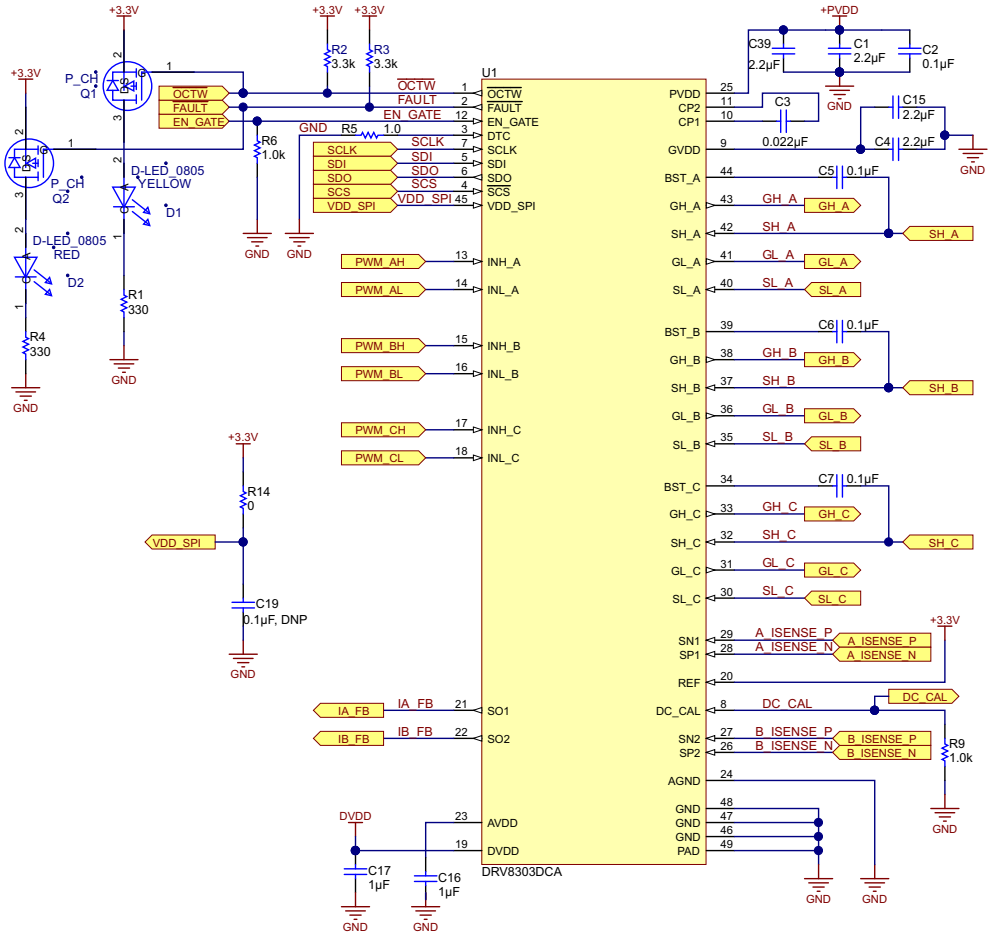


Figure 51. TIDA-00285 Schematic Page 1

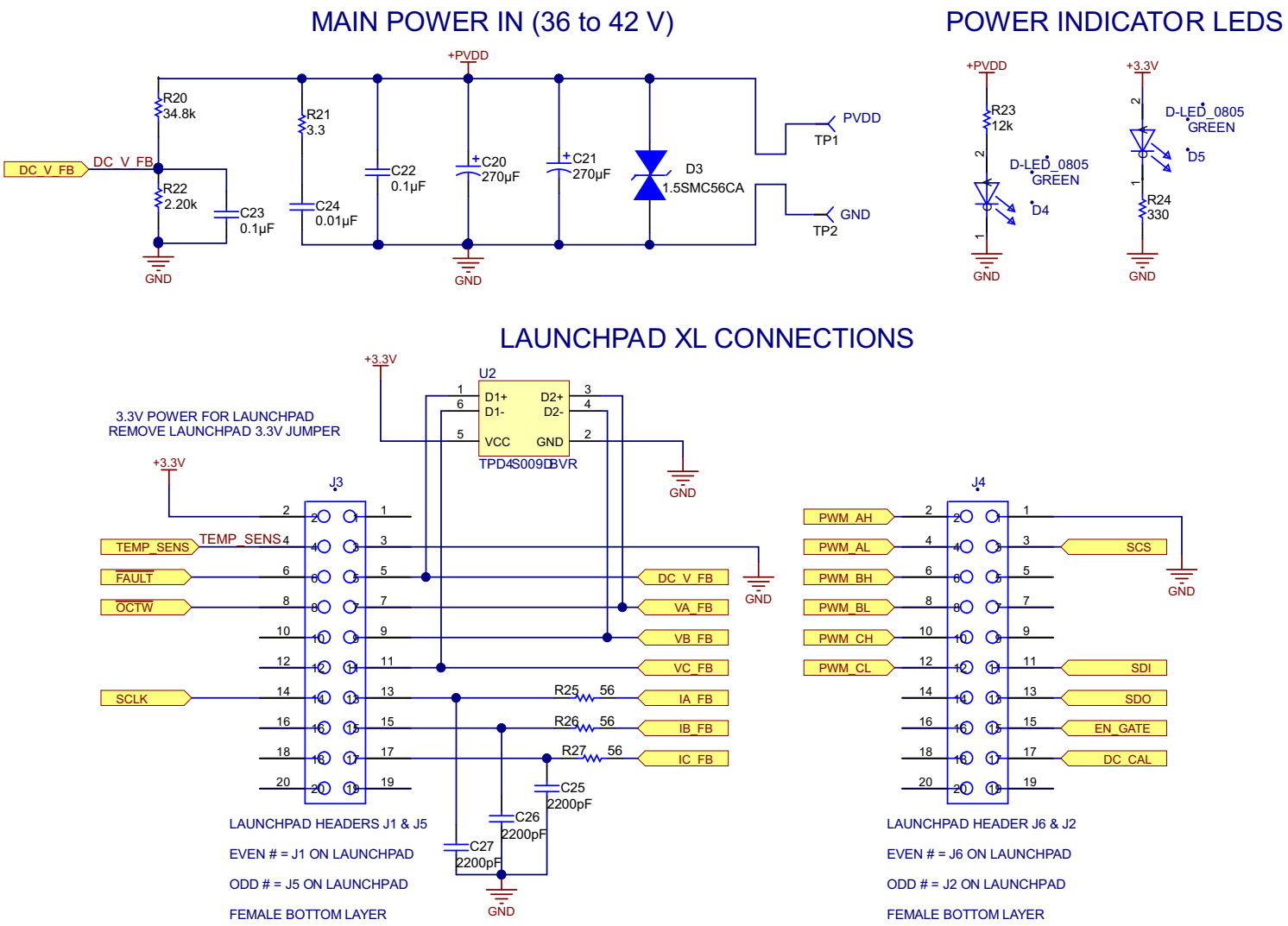


Figure 52. TIDA-00285 Schematic Page 2

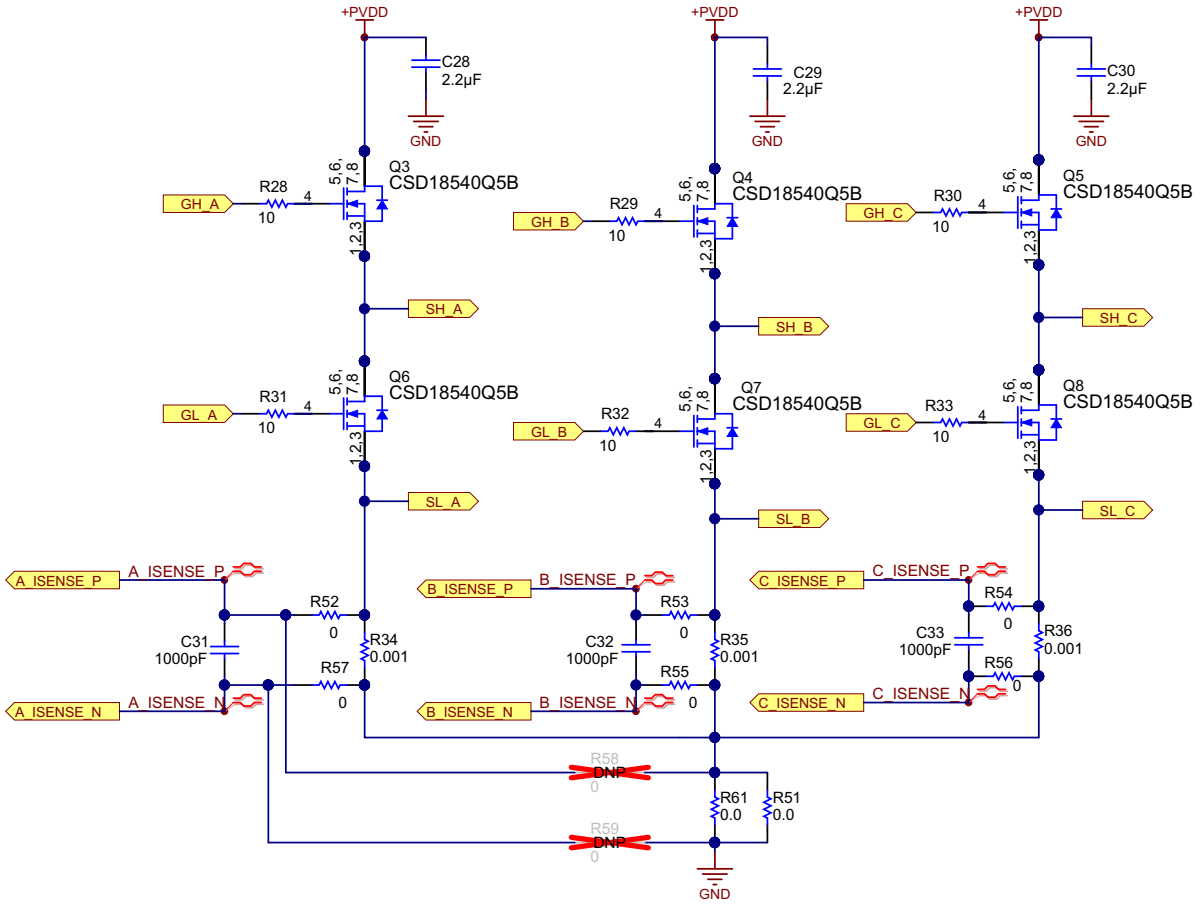


Figure 53. TIDA-00285 Schematic Page 3

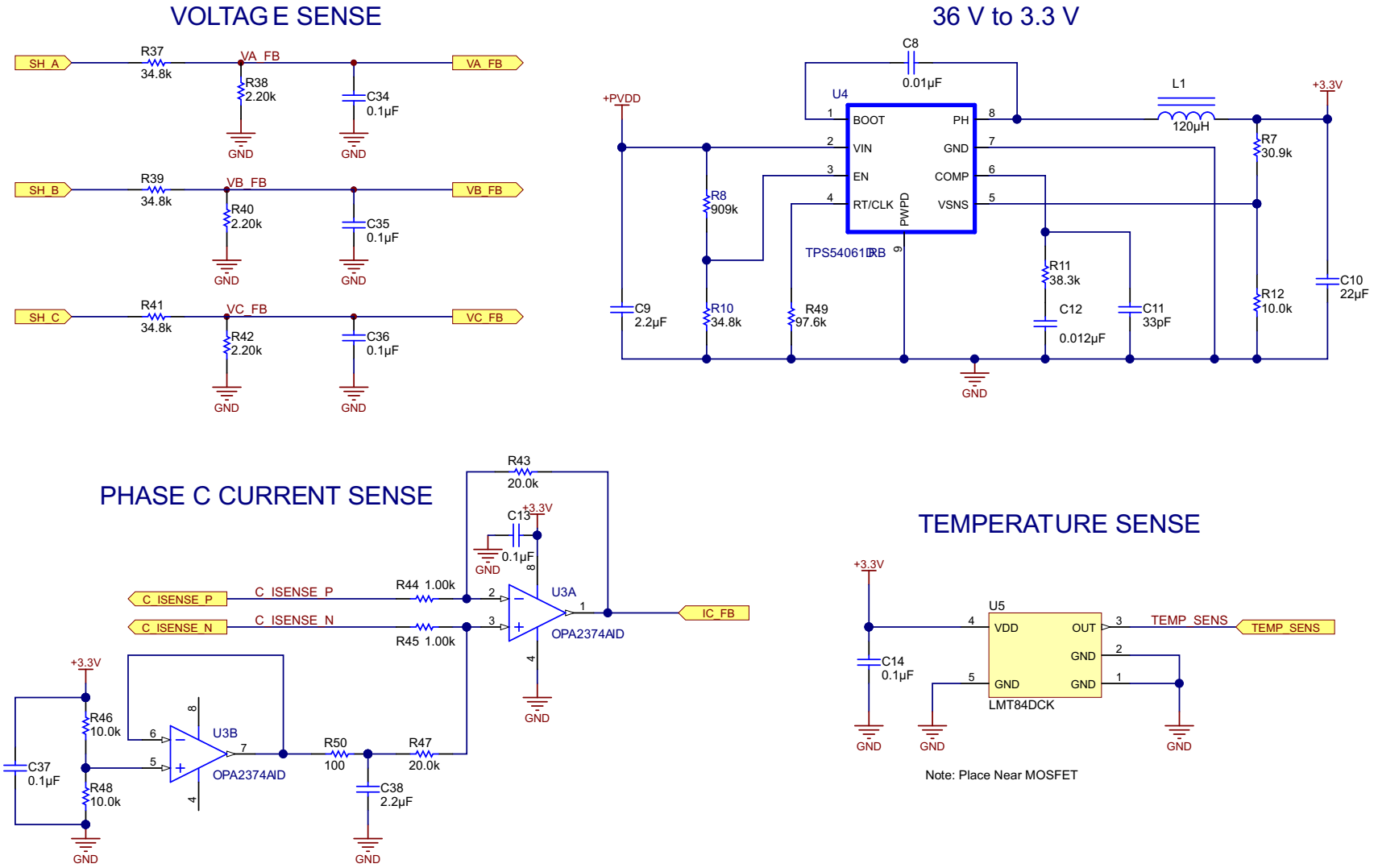


Figure 54. TIDA-00285 Schematic Page 4

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00285.

Table 11. BOM

QTY	REFERENCE	DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
6	C1, C9, C28, C29, C30, C39	CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210	MuRata	GRM32ER72A225KA35L	1210	Fitted
1	C10	CAP, CERM, 22uF, 4V, +/-20%, X5R, 0603	TDK	C1608X5R0G226M080AA	0603	Fitted
1	C11	CAP, CERM, 33pF, 50V, +/-5%, C0G/NP0, 0402	Kemet	C0402C330J5GAC	0402	Fitted
1	C12	CAP, CERM, 0.012uF, 16V, +/-10%, X7R, 0402	MuRata	GRM155R71C123KA01D	0402	Fitted
1	C13	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E104KA01D	0603	Fitted
1	C14	CAP, CERM, 0.1uF, 25V, +/-20%, Y5V, 0603	Kemet	C0603C104M3VACTU	0603	Fitted
2	C16, C17	CAP, CERM, 1uF, 25V, +/-10%, X5R, 0603	MuRata	GRM188R61E105KA12D	0603	Fitted
1	C19	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	TDK	C1608X7R1E104K	0603	Fitted
2	C2, C22	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0603	MuRata	GRM188R72A104KA35D	0603	Fitted
2	C20, C21	CAP 270UF 80V RADIAL	United Chemi-Con	EKYB800ELL271MK20S	Through Hole Radial G	Fitted
5	C23, C34, C35, C36, C37	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	Kemet	C0603C104J4RACTU	0603	Fitted
1	C24	CAP, CERM, 0.01uF, 100V, +/-10%, X7R, 0603	TDK	C1608X7R2A103K	0603	Fitted
3	C25, C26, C27	CAP, CERM, 2200pF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C222KA01D	0603	Fitted
1	C3	CAP, CERM, 0.022uF, 50V, +/-10%, X7R, 0603	TDK	C1608X7R1H223K	0603	Fitted
3	C31, C32, C33	CAP, CERM, 1000pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C102J5GAC	0603	Fitted
1	C38	CAP, CERM, 2.2uF, 10V, +/-20%, X5R, 0603	Kemet	C0603C225M8PACTU	0603	Fitted
2	C4, C15	CAP, CERM, 2.2uF, 25V, +/-10%, X5R, 0805	MuRata	GRM219R61E225KA12D	0805	Fitted
3	C5, C6, C7	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	TDK	C1608X7R1H104K	0603	Fitted

Table 11. BOM (continued)

QTY	REFERENCE	DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	C8	CAP, CERM, 0.01 µF, 25 V, +/- 10%, X7R, 0402	TDK	C1005X7R1E103K	0402	Fitted
1	D1	LED THIN 585NM YEL DIFF 0805 SMD	Lumex Opto/Components Inc	SML-LXT0805YW-TR	0805	Fitted
1	D2	LED THIN660NM SUPRED DIFF0805SMD	Lumex Opto/Components Inc	SML-LXT0805SRW-TR	0805	Fitted
1	D3	Diode, Superfast Rectifier, 400V, 1A, SMA	Littelfuse	1.5SMC56CA	SMA	Fitted
2	D4, D5	LED THIN 565NM GRN DIFF 0805 SMD	Lumex Opto/Components Inc	SML-LXT0805GW-TR	0805	Fitted
1	H1	1/8 BRICK HEATSINK 58X23X22.9MM	Advanced Thermal Solutions Inc	ATS-1181-C1-R0	Rectangular, Angled Fins	Fitted
2	J3, J4	CONN RCPT 20POS .100 DL STR SMD	FCI	89898-310ALF		Fitted
1	L1	Inductor, Drum Core, Ferrite, 120uH, 0.22A, 3.2 ohm, SMD	Bourns	SDR0302-121KL	3x2.5x2.8mm	Fitted
2	Q1, Q2	MOSFET P-CH 8V 5.4A SOT23-3	Vishey Siliconix	SI2325DS-T1-E3	SOT-23-3	Fitted
6	Q3, Q4, Q5, Q6, Q7, Q8	MOSFET, N-CH, 60V, 100A, SON 5x6mm	Texas Instruments	CSD18540Q5B	SON 5x6mm	Fitted
3	R1, R4, R24	RES, 330 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603330RJNEA	0603	Fitted
1	R10	RES, 34.8 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040234K8FKED	0402	Fitted
1	R11	RES, 38.3k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040238K3FKED	0402	Fitted
1	R12	RES, 10.0k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040210K0FKED	0402	Fitted
1	R14	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Fitted
2	R2, R3	RES, 3.3 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06033K30JNEA	0603	Fitted
4	R20, R37, R39, R41	RES, 34.8k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060334K8FKEA	0603	Fitted
1	R21	RES, 3.3 ohm, 5%, 0.25W, 1206	Vishay-Dale	CRCW12063R30JNEA	1206	Fitted
4	R22, R38, R40, R42	RES, 2.20k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-072K2L	0603	Fitted
1	R23	RES, 12k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060312K0JNEA	0603	Fitted
3	R25, R26, R27	RES, 56 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060356R0JNEA	0603	Fitted
6	R28, R29, R30, R31, R32, R33	RES, 10 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060310R0JNEA	0603	Fitted
3	R34, R35, R36	RES, 0.001 ohm, 1%, 2W, 2512	Panasonic, Panasonic, Stackpole	CSNL2512FT1L00	2512	Fitted
2	R43, R47	RES, 20.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060320K0FKEA	0603	Fitted
2	R44, R45	RES, 1.00k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031K00FKEA	0603	Fitted
2	R46, R48	RES, 10.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-103-B-T5	0603	Fitted

Table 11. BOM (continued)

QTY	REFERENCE	DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	R49	RES, 97.6k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040297K6FKED	0402	Fitted
1	R5	RES, 1.0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031R00JNEA	0603	Fitted
1	R50	RES, 100, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100RFKEA	0603	Fitted
2	R51, R61	RES, 0.0 ohm, 63.2A JUMP, 2512	Panasonic	HCJ2512ZT0R00	2512	Fitted
6	R52, R53, R54, R55, R56, R57	RES, 0, 5%, 0.063 W, 0402	Yageo America	RC0402JR-070RL	0402	Fitted
2	R6, R9	RES, 1.0k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K00JNEA	0603	Fitted
1	R7	RES, 30.9k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040230K9FKED	0402	Fitted
1	R8	RES, 909 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402909KFKED	0402	Fitted
2	TP1, TP2	Test Point, O.040 Hole	STD	STD		Fitted
1	U1	THREE PHASE PRE-DRIVER WITH DUAL CURRENT SHUNT AMPLIFIERS, DCA0048A	Texas Instruments	DRV8303DCA	DCA0048A	Fitted
1	U2	ESD Solution for High-Speed Differential Interface, 4 Channels, -40 to +85 degC, 6-pin SOT-32 (DBV), Green (RoHS and no Sb/Br)	Texas Instruments	TPD4S009DBVR	DBV0006A	Fitted
1	U3	Dual 6.5 MHz, 585 uA, Rail-to-Rail I/O CMOS Operational Amplifier, 2.3 to 5.5 V, -40 to 125 degC, 8-pin SOIC (D0008A), Green (RoHS and no Sb/Br)	Texas Instruments	OPA2374AID	D0008A	Fitted
1	U4	IC, 60V/0.2A Synchronous Buck Regulator	Texas Instruments	TPS54061DRB	QFN	Fitted
1	U5	Analog Temperature Sensors with Class-AB Output, DCK0005A	Texas Instruments	LMT84DCK	DCK0005A	Fitted
1	Thermal Pad	THERMALLY CONDUCTIVE FILLER PAD, 5W/m.K, 0.5MM	AMEC THERMASOL	W8TR500G-0.5	60 mm X 24 mm Rectangular	Fitted
2	Machine Screw	MACHINE SCREW PAN PHILLIPS 6-32	B&F Fastener Supply	PMS 632 0050 PH	6-32 Thread	Fitted
2	Hex Nut	HEX NUT 5/16" 6-32	B&F Fastener Supply	HNZ 632	Hex, 6-32 Thread	Fitted
2	R58, R59	RES, 0, 5%, 0.063 W, 0402	Yageo America	RC0402JR-070RL	0402	Not Fitted

10.3 PCB Layout Recommendations

Consider the following points during the PCB layout design and assembly:

1. The DRV8303 makes an electrical connection to GND through the PowerPAD. Always check to ensure that the PowerPAD has been properly soldered. See the PowerPAD application report (SLMA002).
2. C1/C2/C39: Place PVDD decoupling capacitors close to their corresponding pins with a low impedance path to device GND (PowerPAD).
3. C4/C15: Place GVDD capacitor close its corresponding pin with a low-impedance path-to-device GND (PowerPAD).
4. C16/C17: Place AVDD and DVDD capacitors close to their corresponding pins with a low-impedance path to the AGND pin. If possible, make this connection on the same layer.
5. Tie AGND to GND (PowerPAD) through a low-impedance trace/copper fill.
6. Add stitching vias to reduce the impedance of the GND path from the top to bottom side.

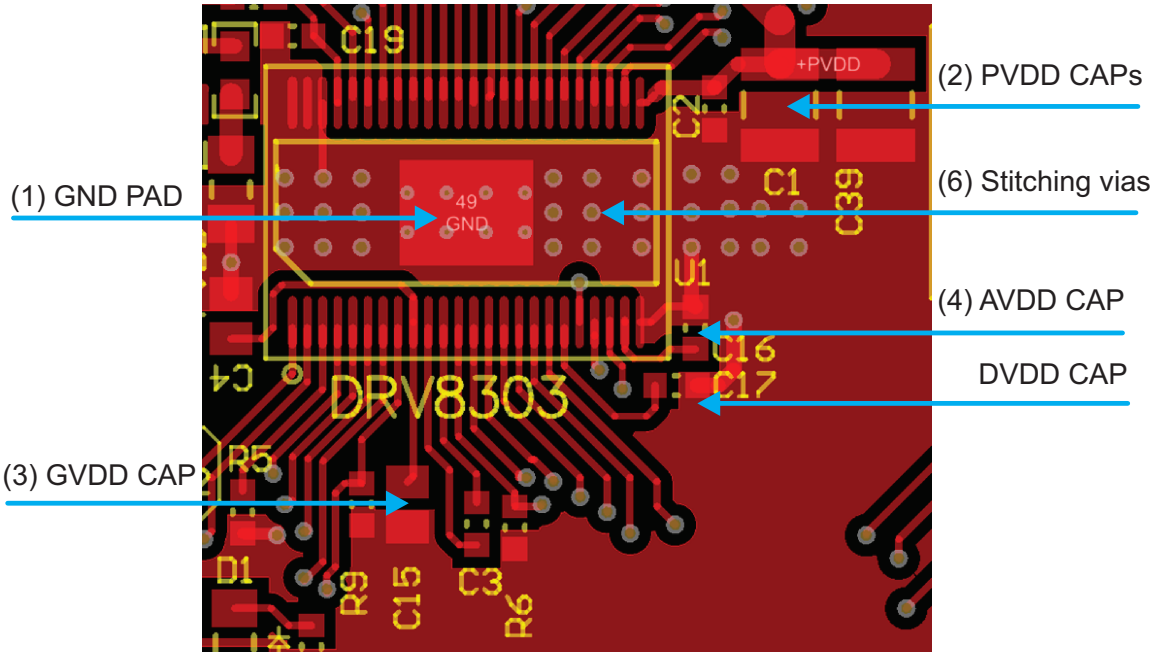


Figure 55. Layout Consideration for DRV8303

7. Clear the space around and underneath the DRV8303 to allow for better heat spreading from the PowerPAD.

8. Route the track for sensing the V_{DS} of the MOSFET as a differential track as shown in Figure 56.

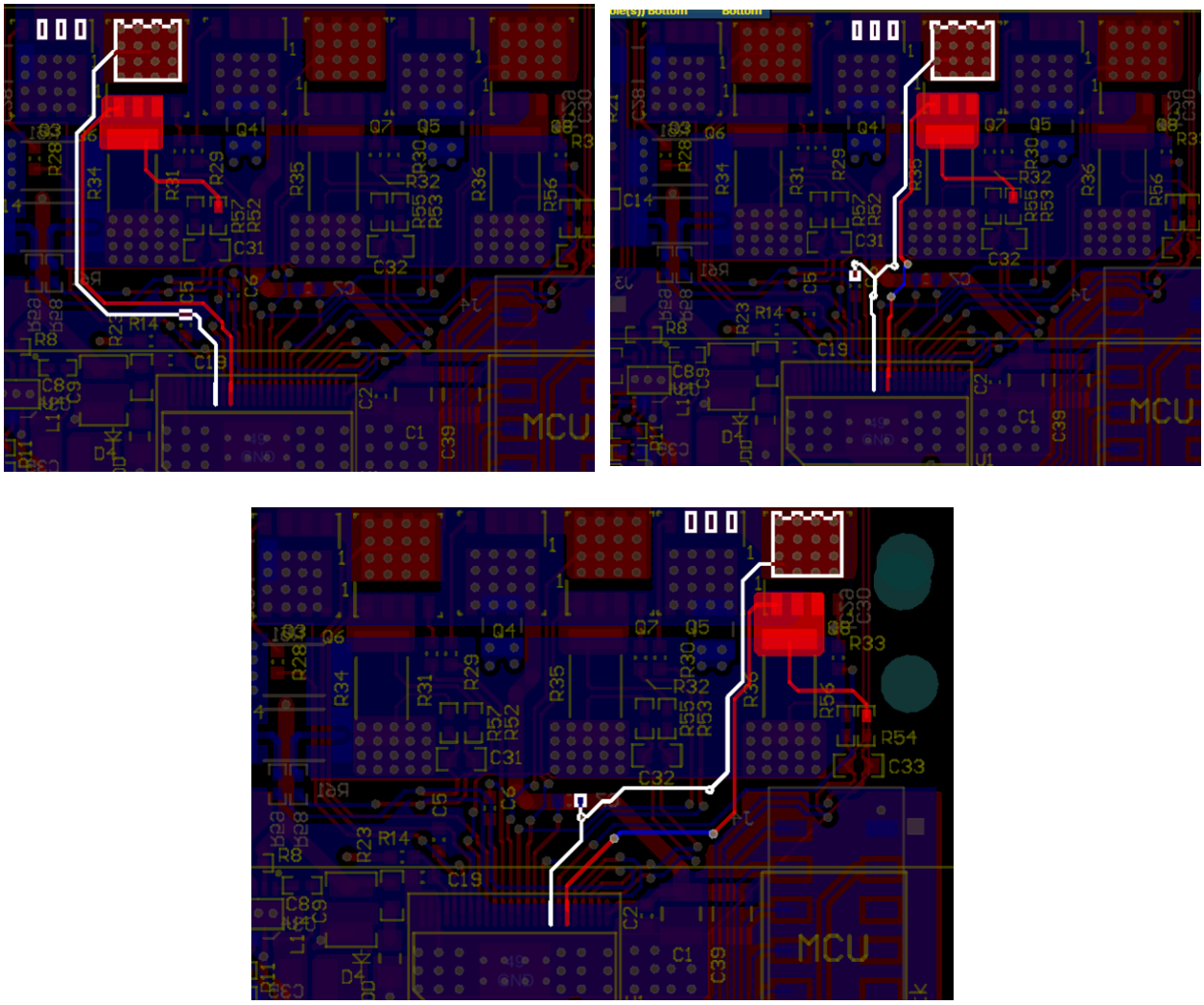


Figure 56. Differential Line for V_{DS} Sensing of MOSFETs

9. In the reference design, the PCB is made in four layer with 2-Oz (70 micron) copper thickness in every layer. The power tracks are made wide to carry a high current. Figure 57 shows the current carrying track from the power input point. The tracks in different layers are connected by arrays of stitching vias.

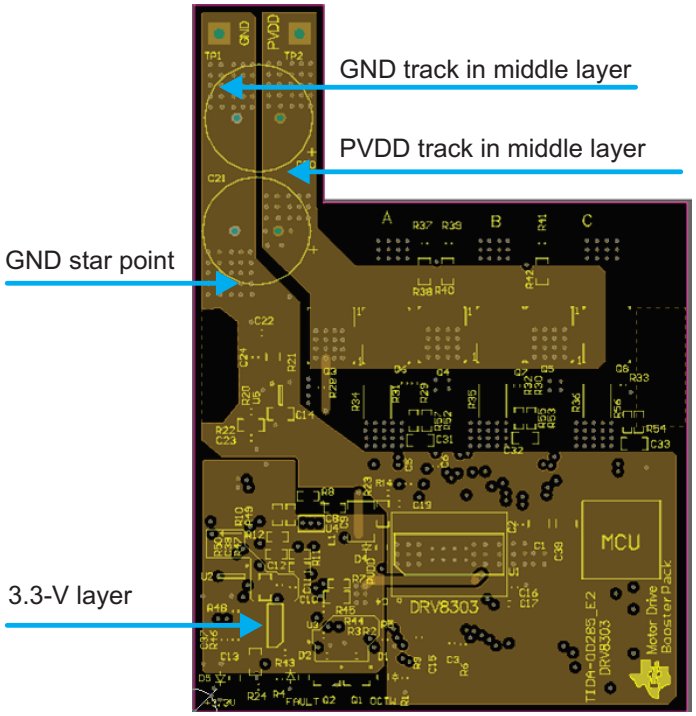


Figure 57. Layout Considerations for Power Handling and GND Tracks

10. A GND star point is defined in the PCB from where the GND path for the DRV8303 and other signal circuits in the board is tapped.
11. For better thermal dissipation from the MOSFET to the PCB, increase the copper area around the MOSFET pad as much as possible. Use arrays of vias under the drain pad of the MOSFET, which will help in better heat dissipation through the bottom surface copper area. Add a small heat sink or copper bars to the bottom surface of PCB to aid heat dissipation.

12. The placement of the decoupling capacitors is important for the proper functioning of the V_{DS} sensing protection of the DRV8303. Place these capacitors near to each MOSFET leg. The return path of the decoupling capacitors should be through a thick track, and the return path length should be as short as possible to improve the decoupling.

NOTE: In the reference design, shunt resistors are provided at the ground (battery negative) rail. Therefore, the return path of the decoupling capacitors across the phase B and phase C legs (C29 and C30) are taken through wide tracks in one of the middle layer to the star point of GND.

However, during testing using InstaSPIN-FOC, the shunt resistors are not used and thus populated with 0-Ω resistors. To decouple properly, shorten the return of the capacitors C29 and C30 to the thick GND track near to these capacitors using external soldering as shown in Figure 59.

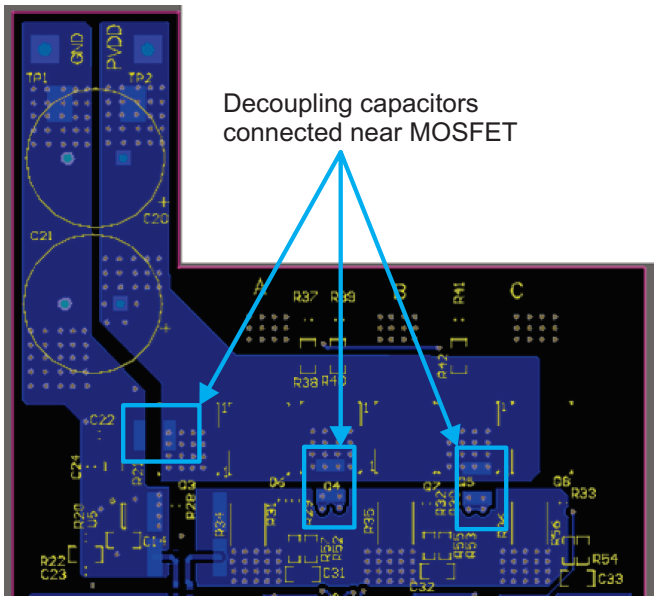


Figure 58. Mounting of Decoupling Capacitors for Inverter Legs

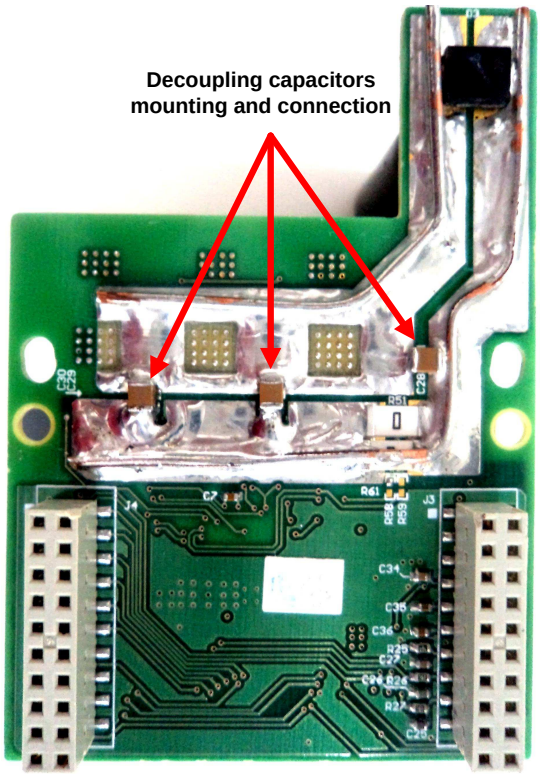


Figure 59. Mounting of Decoupling Capacitors for Inverter Legs

10.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00285.

10.4 Altium Project

To download the Altium project files, see the design files at TIDA-00285.

10.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00285.

10.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00285.

11 References

1. Texas Instruments Datasheet, *Three Phase Pre-Driver with Dual Current Shunt Amplifiers*, DRV8303 (SLOS846)
2. Texas Instruments Application Report, *Trapezoidal Control of BLDC Motors Using Hall Effect Sensor*, (SPRABQ6)
3. Texas Instruments Technical Reference Manual, *TMS320F28026F, TMS320F28027F InstaSPIN™-FOC Software*, (SPRUHP4)
4. Texas Instruments User's Guide, *InstaSPIN-FOC™ and InstaSPIN-MOTION™*, (SPRUHJ1)
5. Texas Instruments Application Report, *PowerPAD™ Thermally Enhanced Package*, (SLMA002)
6. Texas Instruments Application Report, *Semiconductor and IC Package Thermal Metrics*, (SPRA953)
7. Texas Instruments Application Report, *AN-2026 The Effect of PCB Design on the Thermal Performance of SIMPLE SWITCHER® Power Modules*, (SNVA424)
8. Texas Instruments Application Report, *PCB Layout Guidelines for Power Controllers*, (SLUA366)

12 Terminology

BLDC— Brushless DC motor

ESD— Electrostatic discharge

FETs, MOSFETs—The metal-oxide-semiconductor field-effect transistor

FOC— Field oriented control

LaunchPad— All reference to LaunchPad refers to InstaSPIN-FOC enabled C2000 LaunchPads

LFM— Linear feet per minute; 1 LFM = 0.005 m/s

MCU— Microcontroller unit

PMSM— Permanent magnet synchronous motor

PWM— Pulse width modulation

RMS— Root mean square

RPM— Rotation per minute

SPI— Serial peripheral interface

TVS— Transient voltage suppressors

13 About the Author

NELSON ALEXANDER is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Nelson has been with TI since 2011 and has been involved in designing products related to smart grid and embedded systems based on microcontrollers. Nelson earned his bachelor of technology in electrical engineering at MSRIT, Bangalore.

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