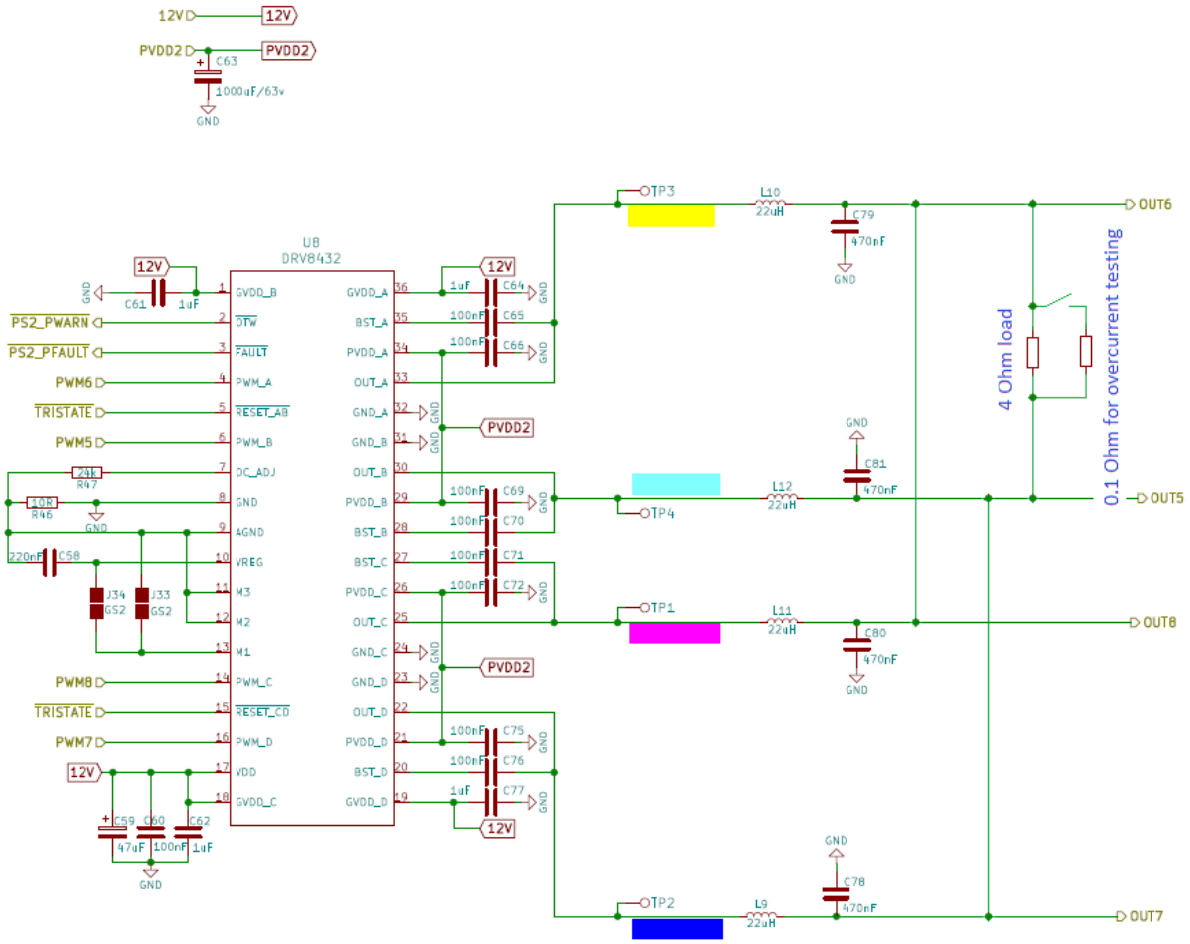
I would like to apologize for the error in my previous diagram. I forgot to draw two connections, which make load being shared between two bridges (PBTL).

The circuit diagram of DRV8432 PBTL stage with scope traces colors:

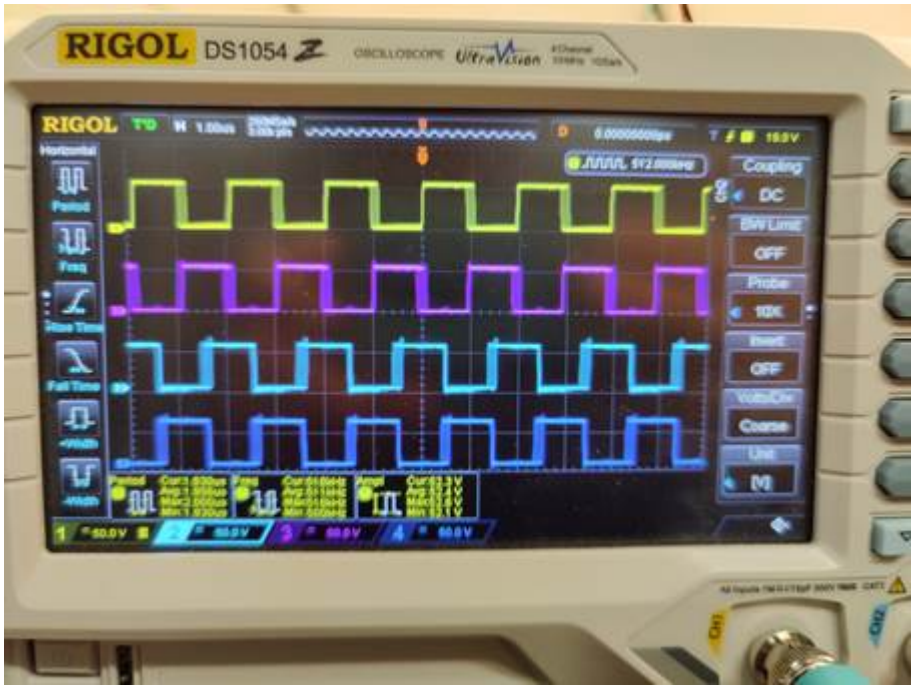


The ~FAULT is asserted LOW when one or more half-bridges are detecting OCP. The other half-bridges in the same IC will still operate normally; the ones which had an OCP will be in High-Z.

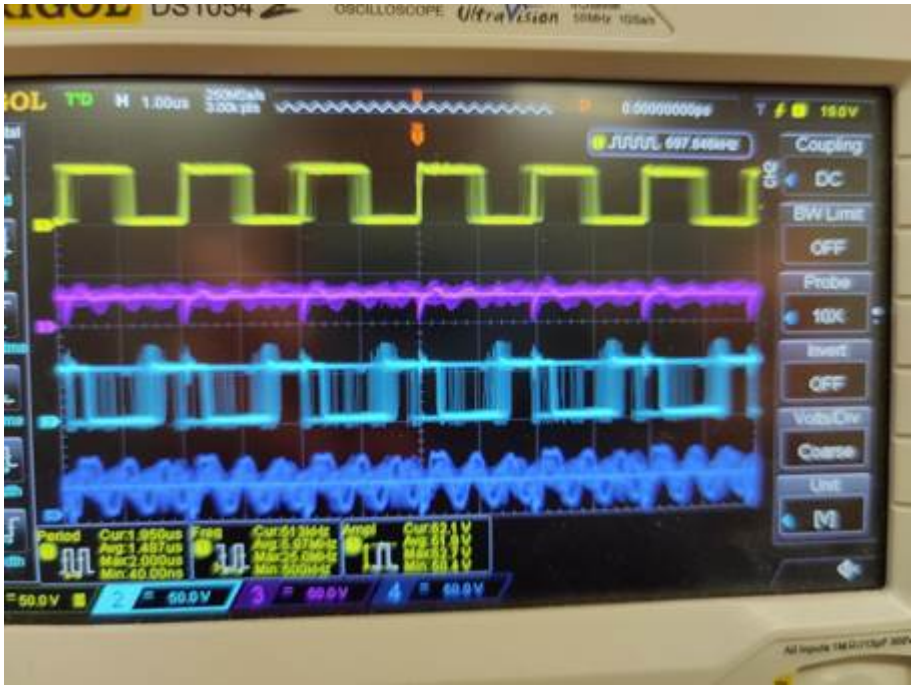
The ~FAULT pin stays low during and after an OCP to indicate a fault has happened. The TI FAE also says that it can only be reset by restarting the power stage.

I have captured the PWM outputs of the bridges for three cases:

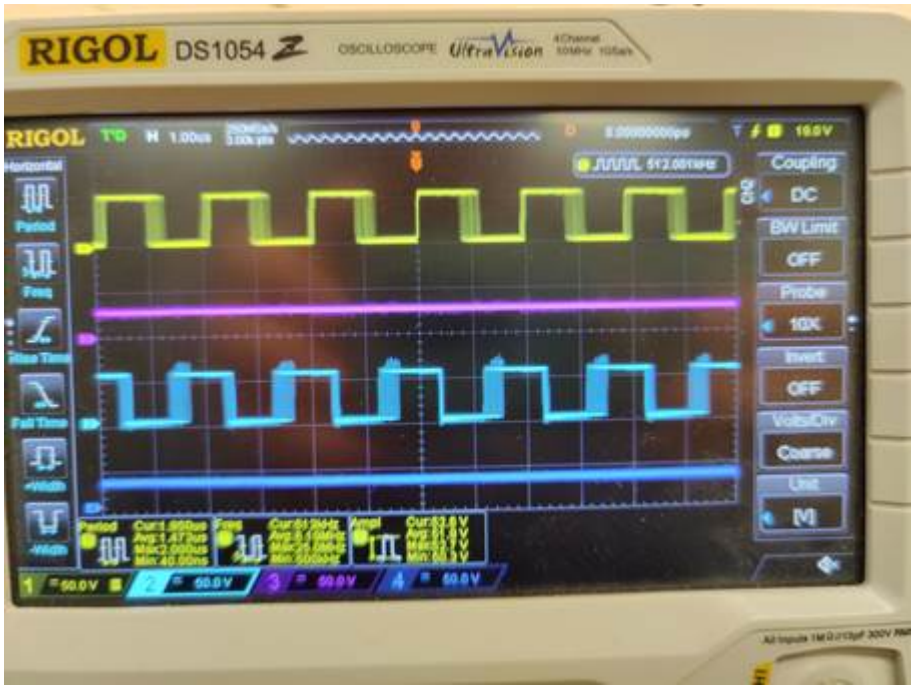
Normal operation:



During short circuit:



After short circuit is removed:



The yellow and magenta traces are signals on the first bridge PWM outputs. The cyan and blue traces are signals on the second bridge PWM outputs. Load is connected after the filter inductors.

During the short circuit, the OCP event was detected for magenta and blue outputs and these outputs turn into high-Z state. The other two PWM outputs keep switching.
It seems to be random whether the first bridge (magenta and blue) or the second one (yellow and cyan) goes into high-Z, but regardless the other two PWM outputs keep switching with ~FAULT low.

This means that after an OCP event, the system has lost 2 phases out of 4.

The question still remains – why there is the output signal with ~FAULT asserted? Why another two phases do not go to high-Z? Driver is set to dual full bridge mode with CBC M1=M2=M3=0. Should we set M2=1 as per attached table?

Mode Selection Pins

MODE PINS			OUTPUT CONFIGURATION	DESCRIPTION
M3	M2	M1		
0	0	0	2 FB or 4 HB	Dual full bridges (two PWM inputs each full bridge) or four half bridges with cycle-by-cycle current limit
0	0	1	2 FB or 4 HB	Dual full bridges (two PWM inputs each full bridge) or four half bridges with OC latching shutdown (no cycle-by-cycle current limit)
0	1	0	1 PFB	Parallel full bridge with cycle-by-cycle current limit
0	1	1	2 FB	Dual full bridges (one PWM input each full bridge with complementary PWM on second half bridge) with cycle-by-cycle current limit
1	x	x	Reserved	