DATA BOOK
PACKAGE OUTLINE

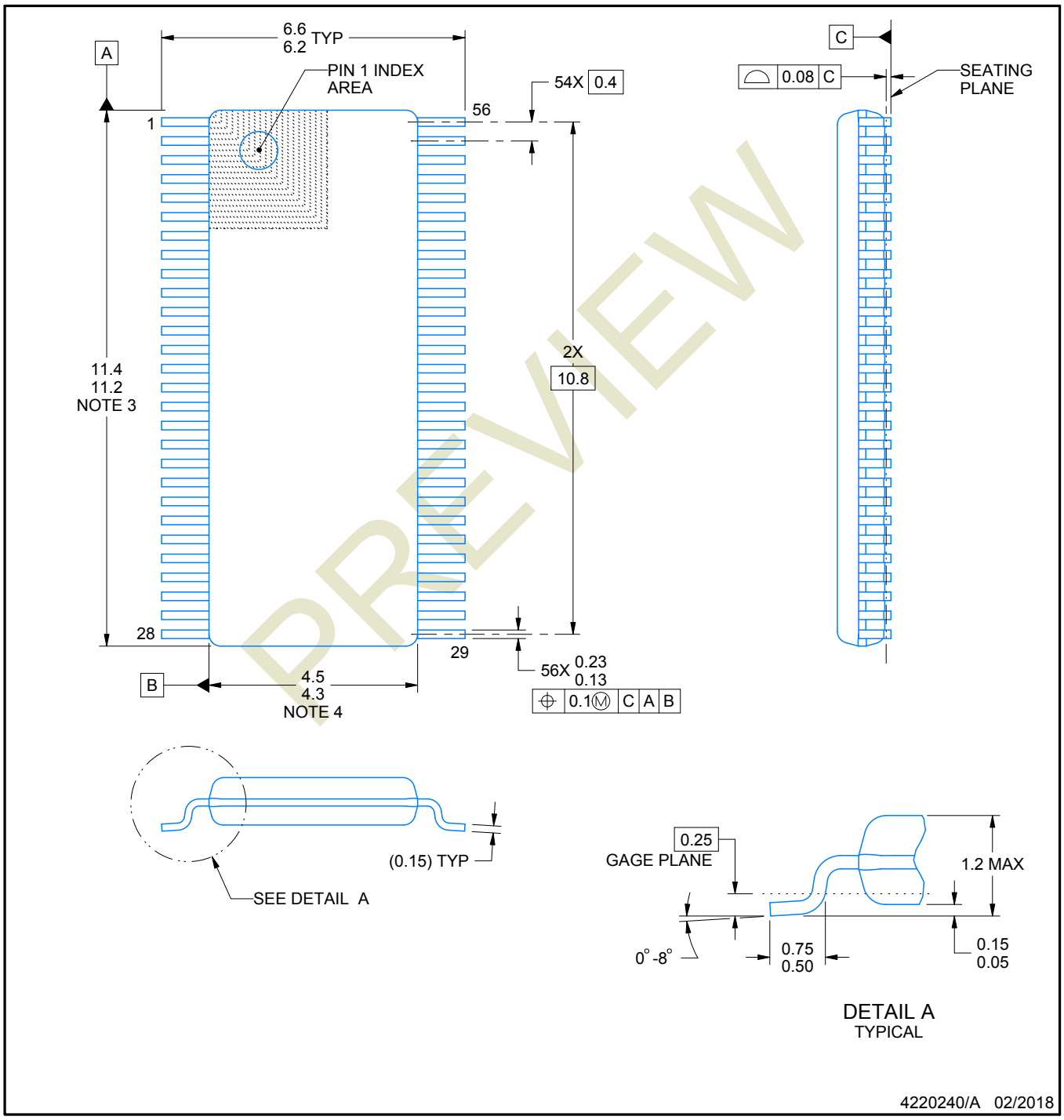
DRAFTER: K. SINCERBOX	DATE: 2018		DIMENSIONS IN MILLIMETERS
DESIGNER:	DATE:	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
CHECKER: K. SINCERBOX	DATE: 2018		
ENGINEER: A. TORMA	DATE: 2018	ePOD, DGV0056A / TVSOP 56 PIN, 0.4 MM PITCH	
APPROVED: D. CHIN & E. LEE	DATE: 2018		
RELEASED: WDM	DATE: 2018		
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016	SCALE NTS / SIZE A / 4220240 / REV A / PAGE 1 OF 5	

PACKAGE OUTLINE

DGV0056A

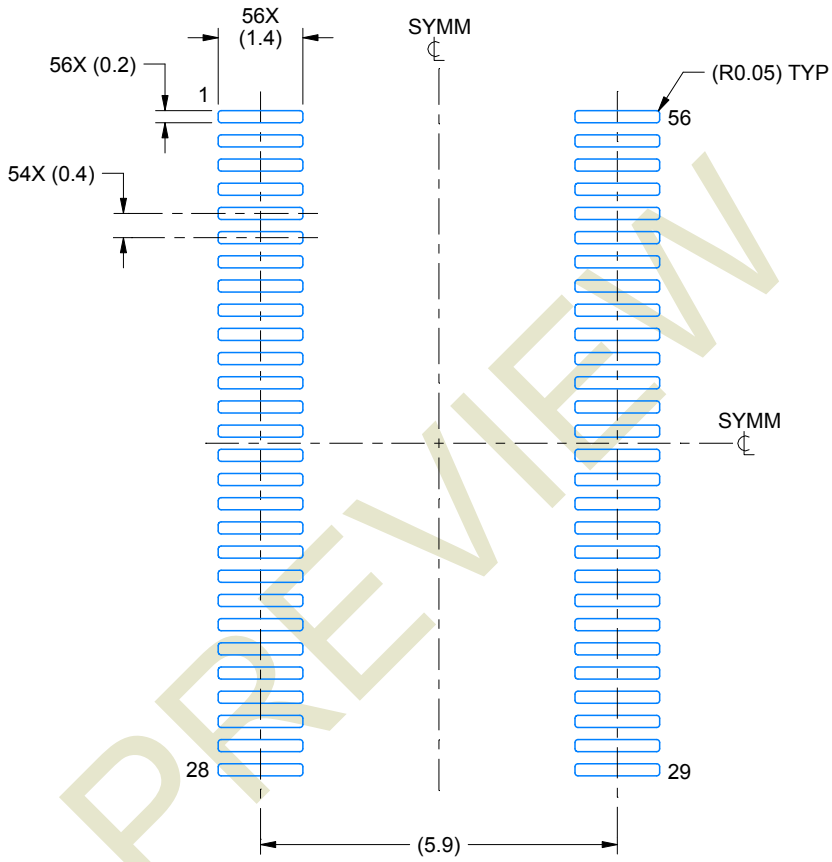
TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

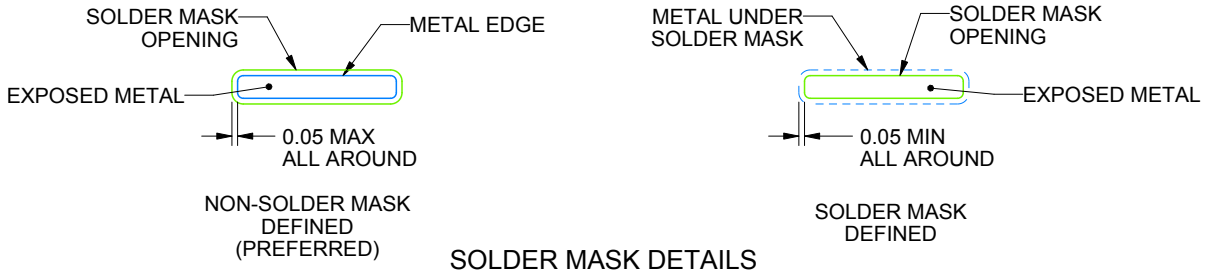


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

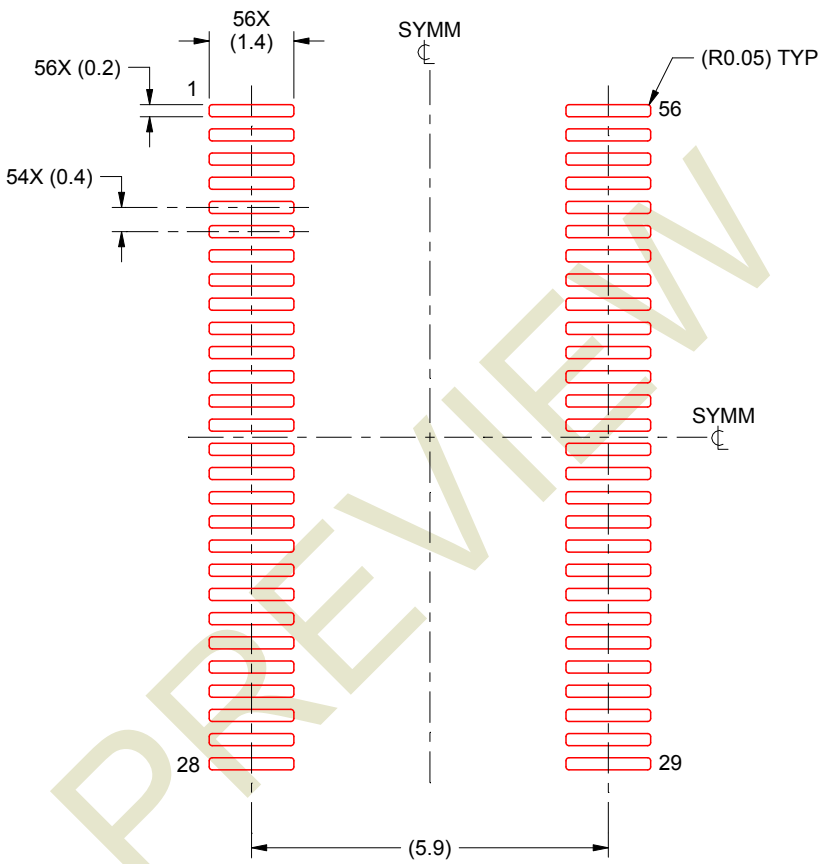


SOLDER MASK DETAILS

4220240/A 02/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2171729	2018	A. TORMA / K. SINCERBOX