


DATA BOOK PACKAGE OUTLINE

PREVIEW

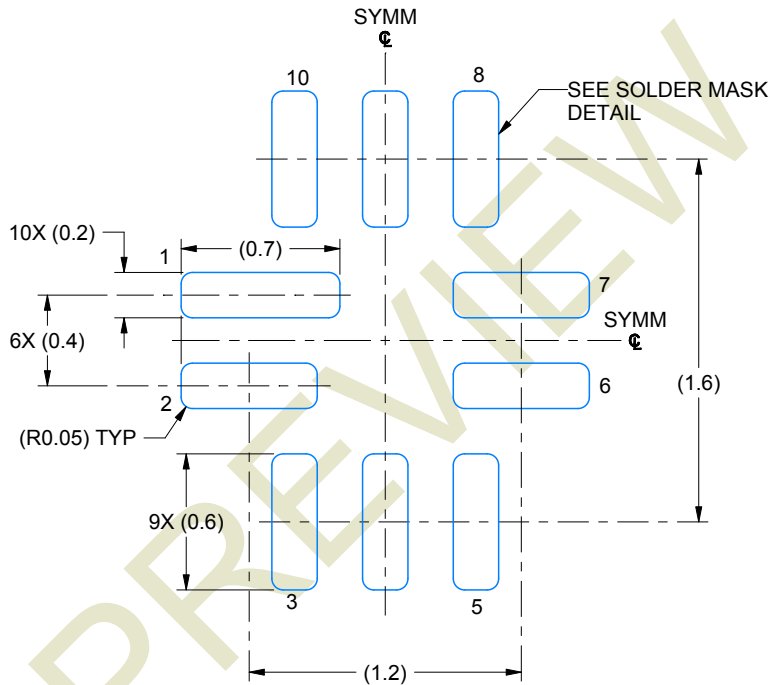
DRAFTER: K. SINCERBOX	DATE: 2019			DIMENSIONS IN MILLIMETERS		
DESIGNER:	DATE:	 TEXAS INSTRUMENTS <small>SEMICONDUCTOR OPERATIONS</small>		<small>CODE IDENTITY NUMBER</small> 01295		
CHECKER: K. SINCERBOX	DATE: 2019	ePOD, RSW0010A / UQFN, 10 PIN, 0.4 MM PITCH				
ENGINEER: A. TORMA	DATE: 2019					
APPROVED: D. CHIN & D. MILO	DATE: 2019					
RELEASED: K. SINCERBOX	DATE: 2019					
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016	<small>SCALE</small> NTS	<small>SIZE</small> A	4224897	<small>REV</small> A	<small>PAGE</small> 1 OF 5

EXAMPLE BOARD LAYOUT

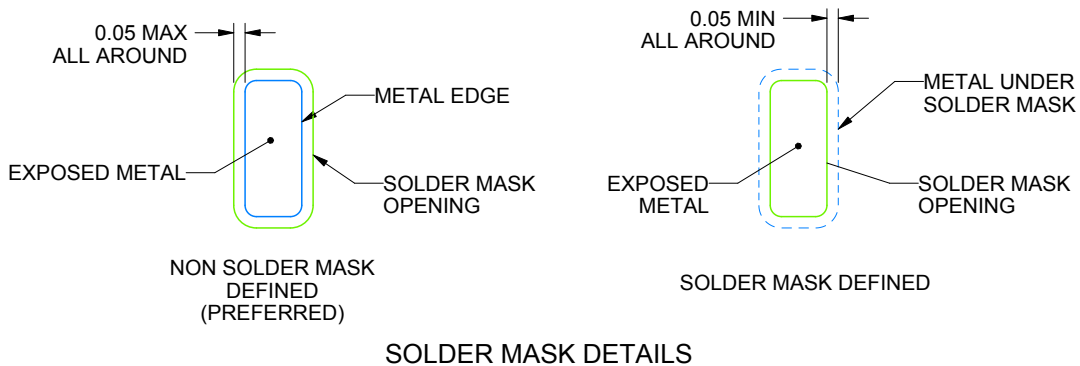
RSW0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4224897/A 03/2019

NOTES: (continued)

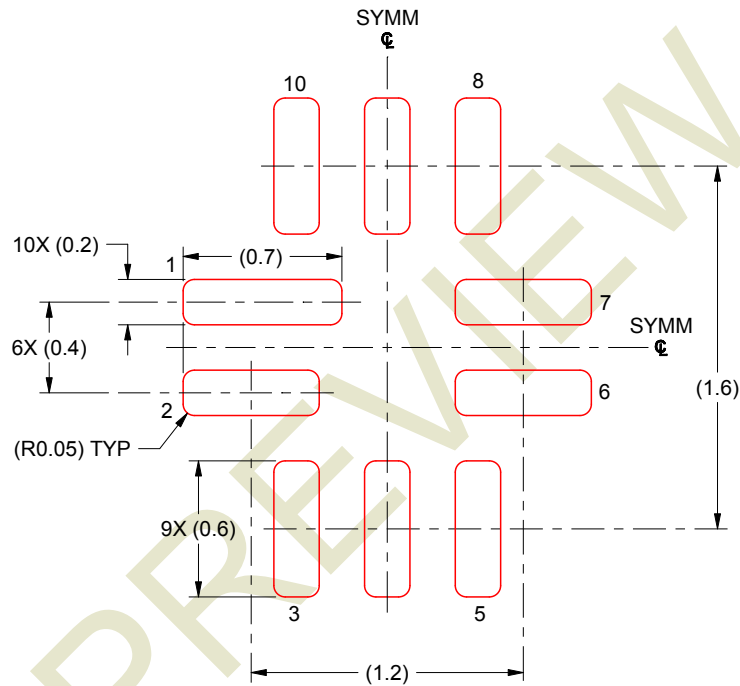
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSW0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2180189	2019	A. TORMA / K. SINCERBOX

PREVIEW