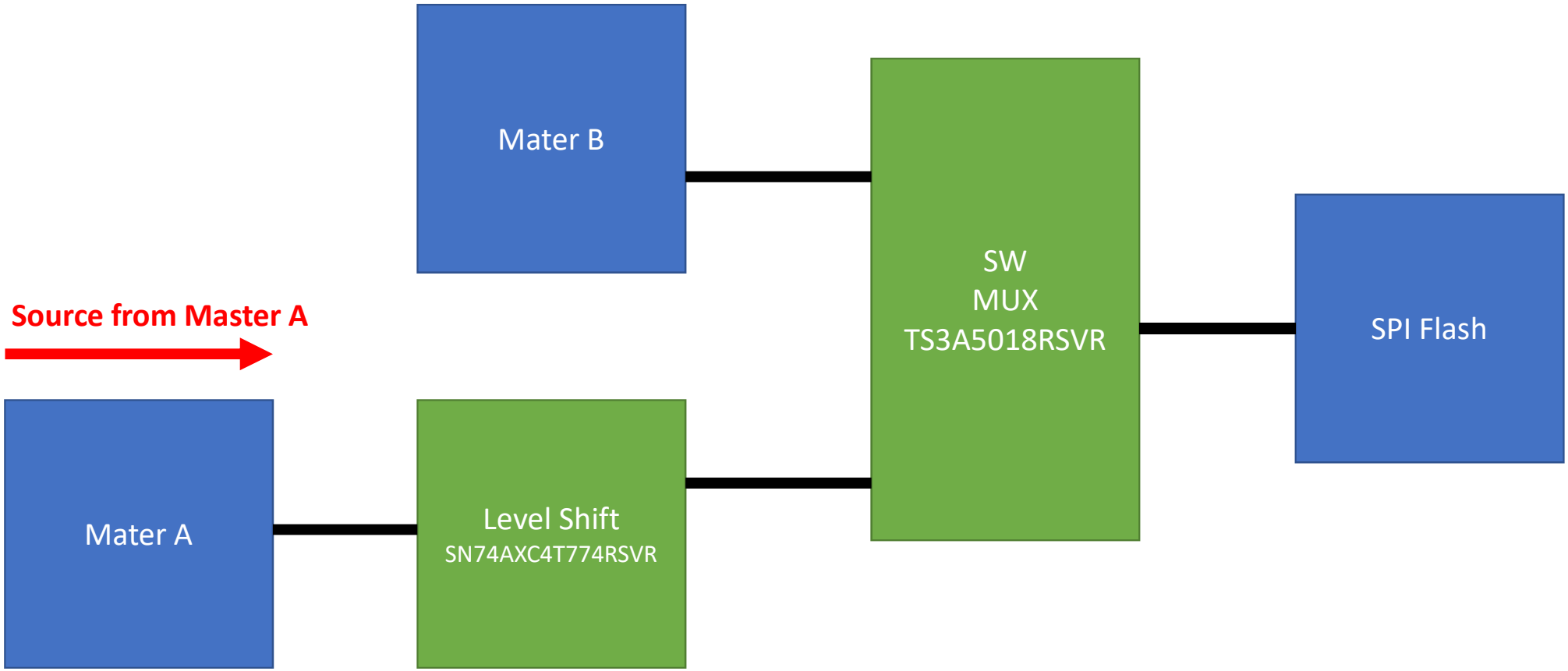
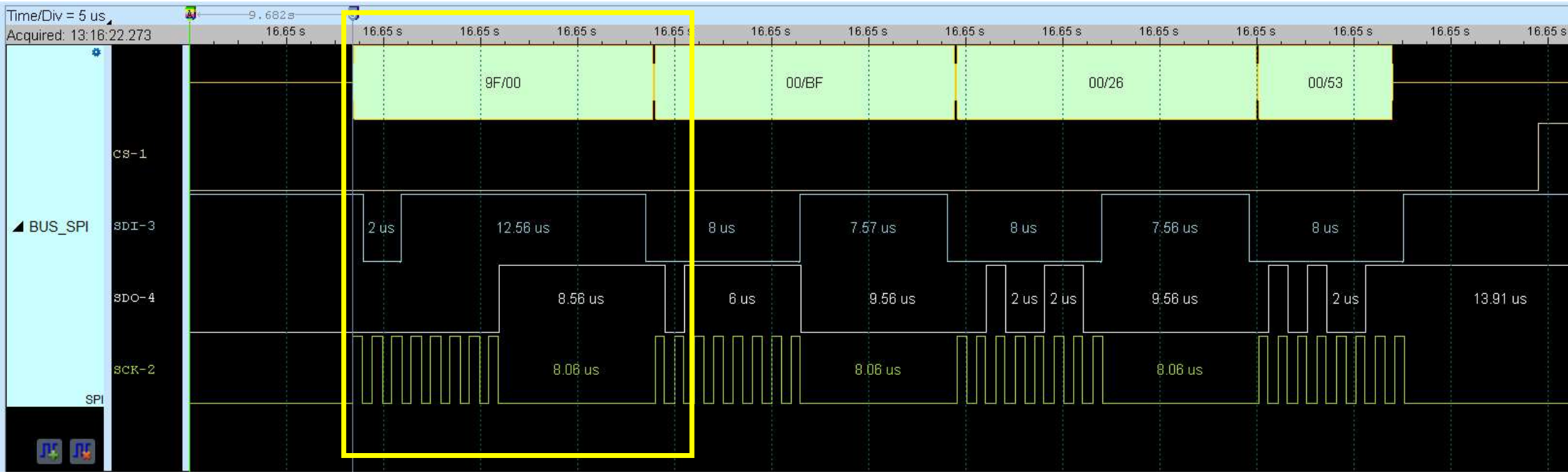
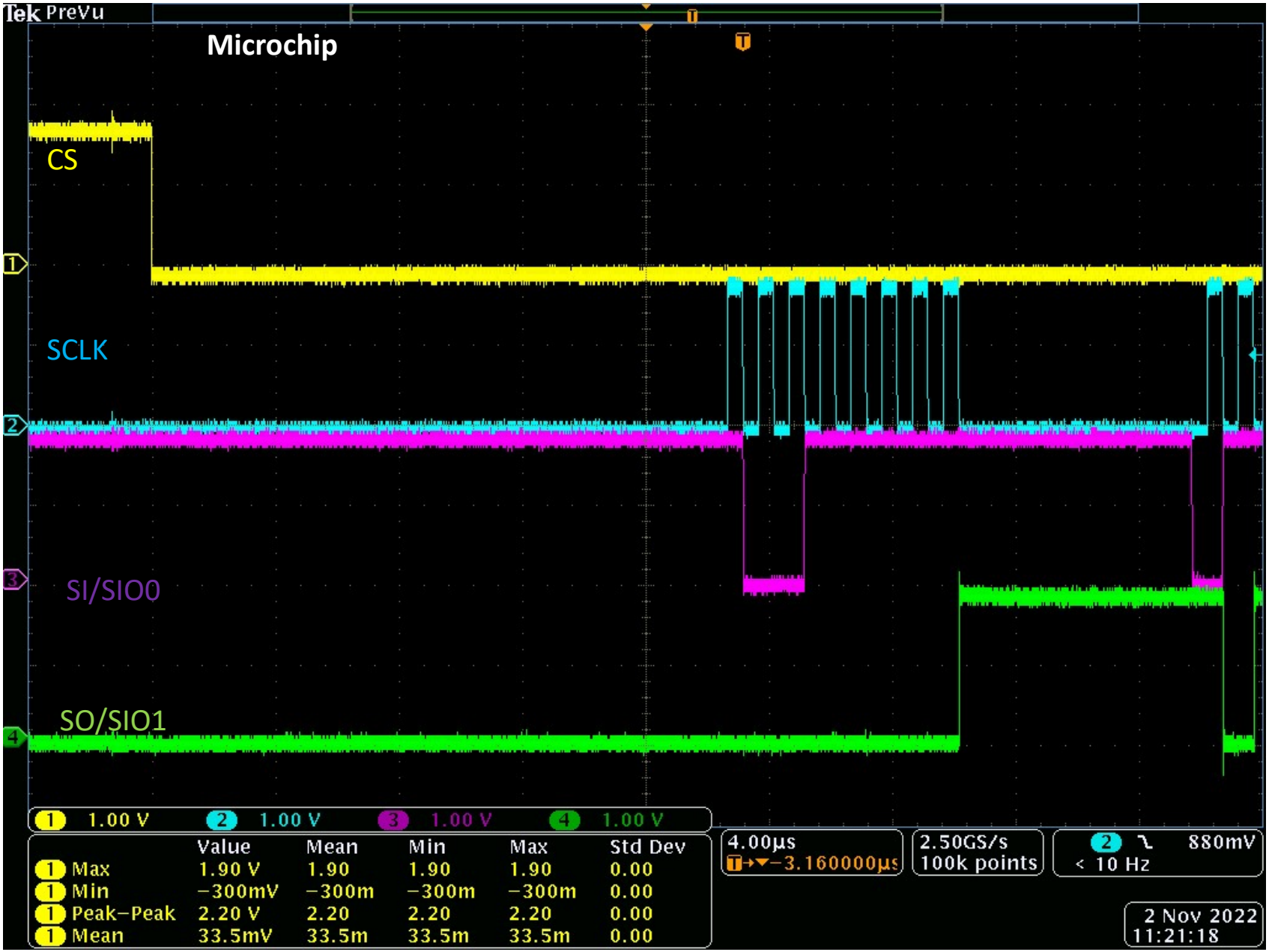
1MUX vs 2 MUX cascaded in SPI application

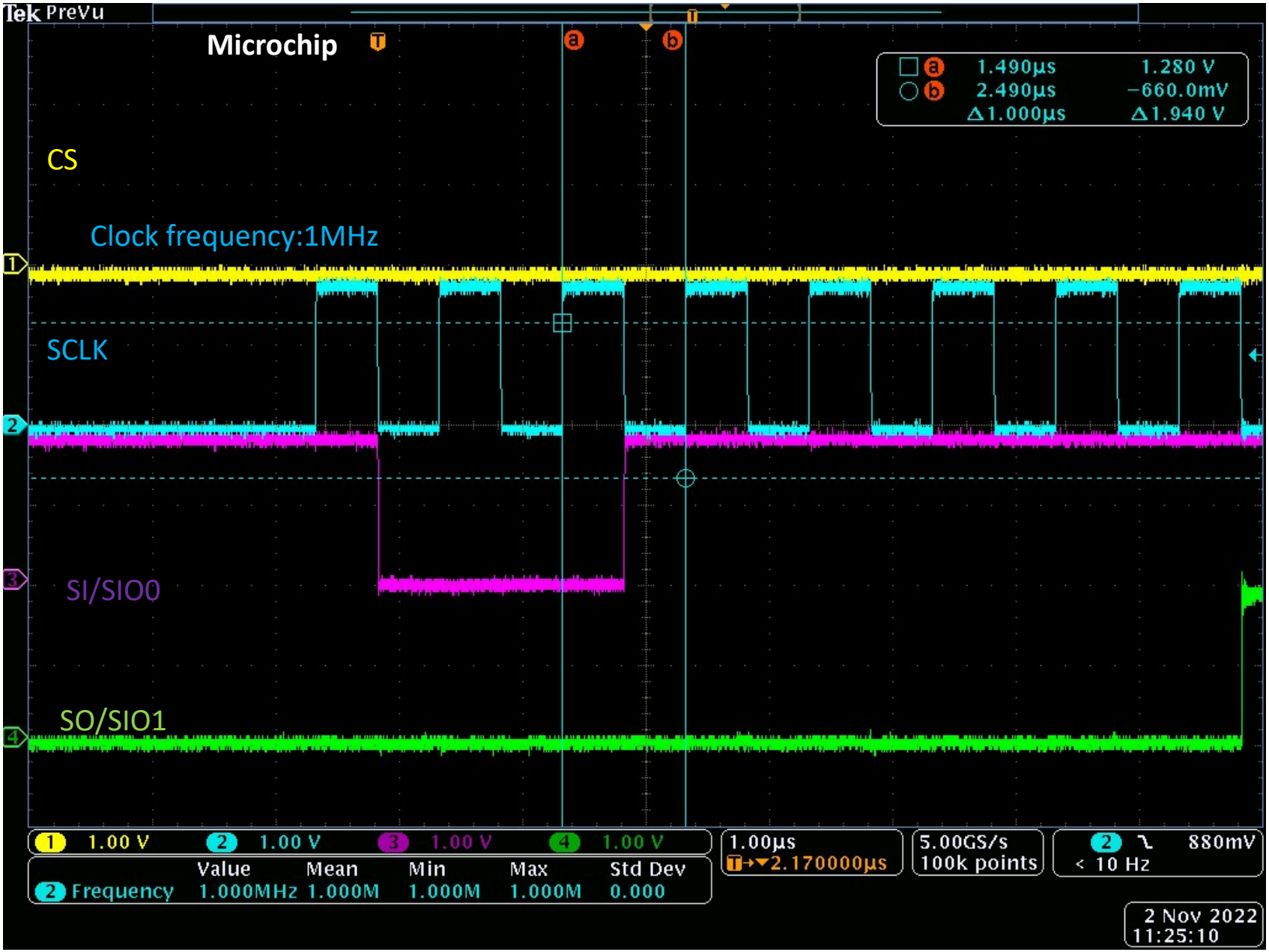
Structure of 1MUX in SPI application

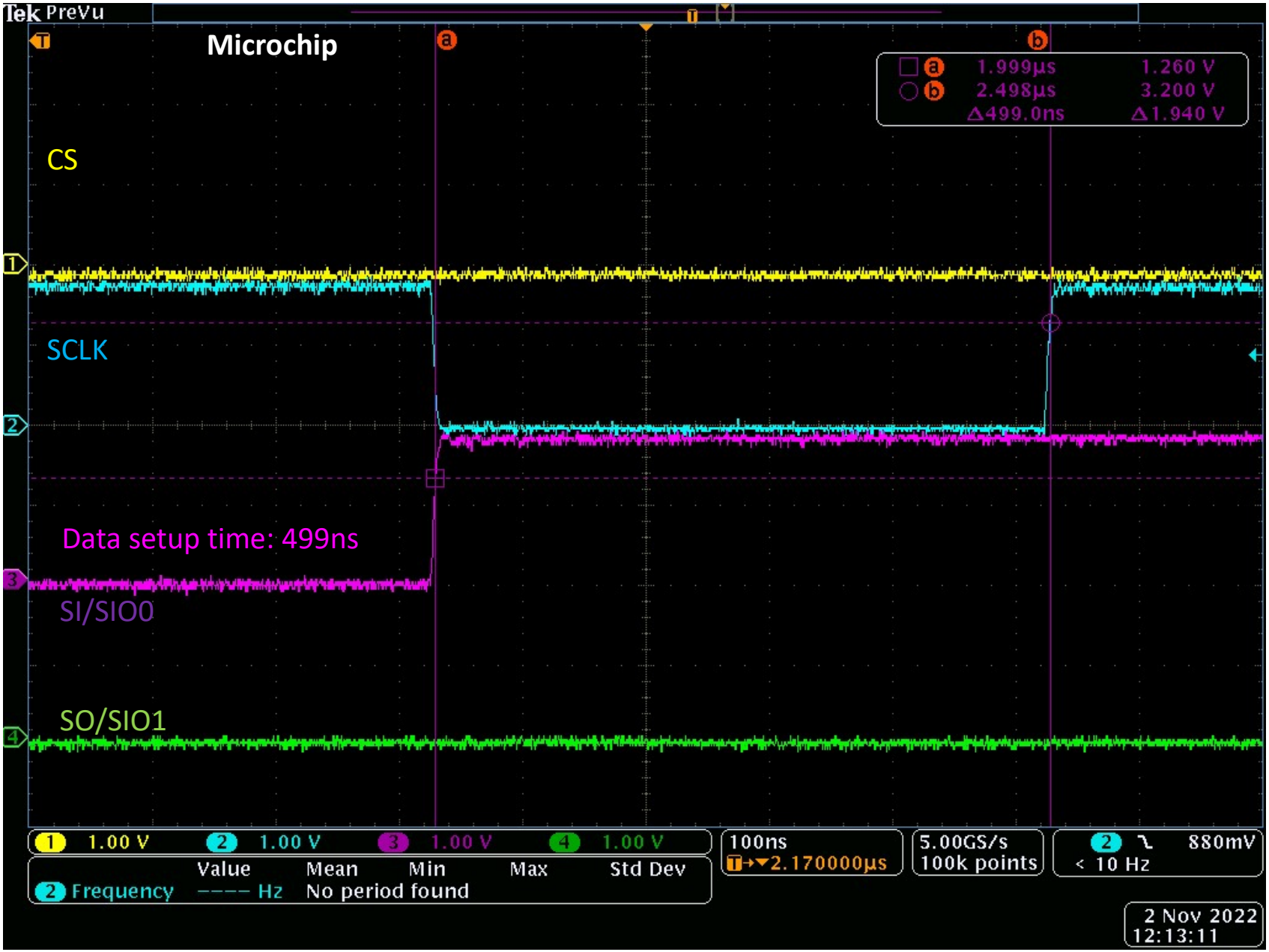


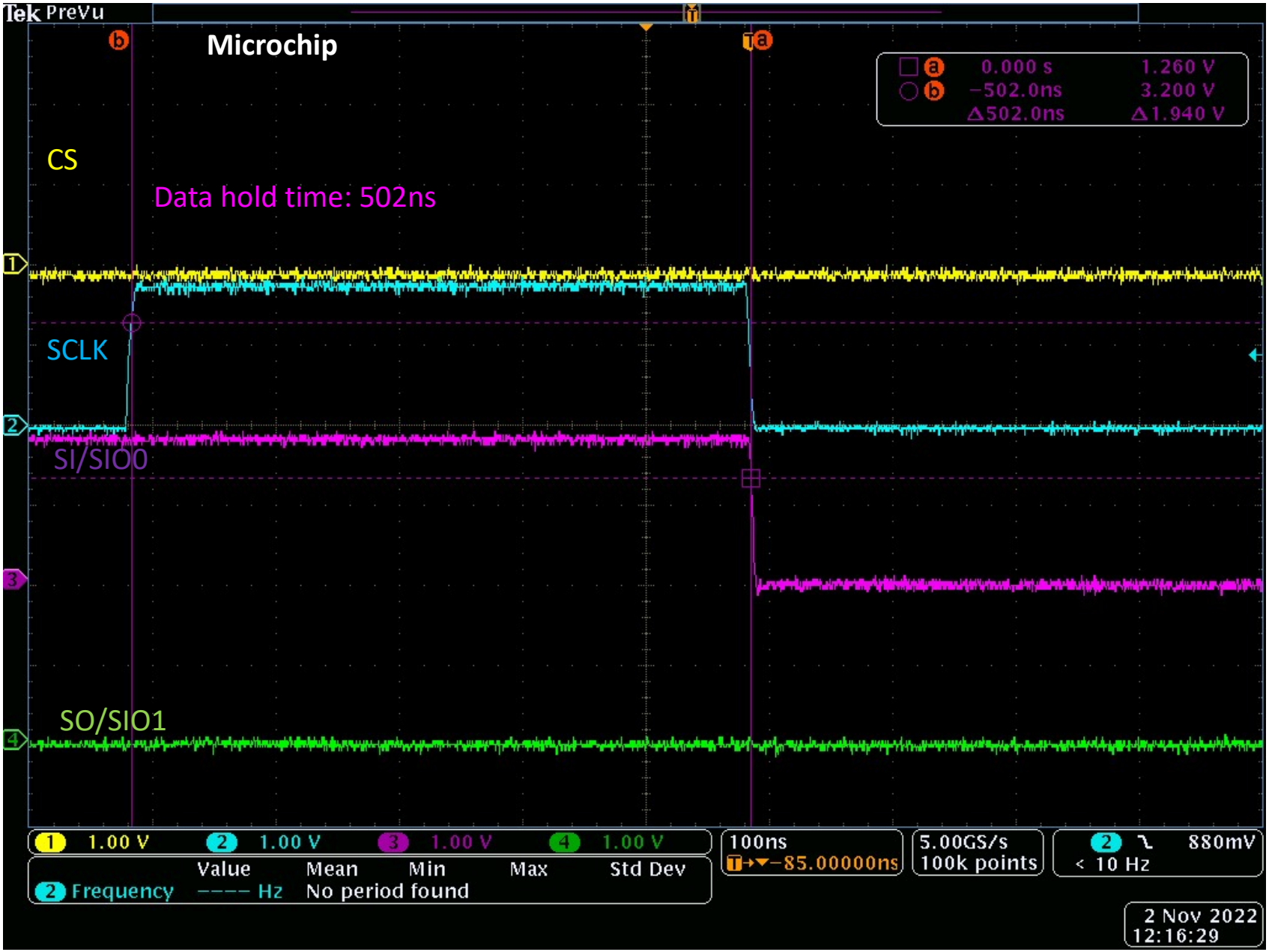
Logic Analyzer

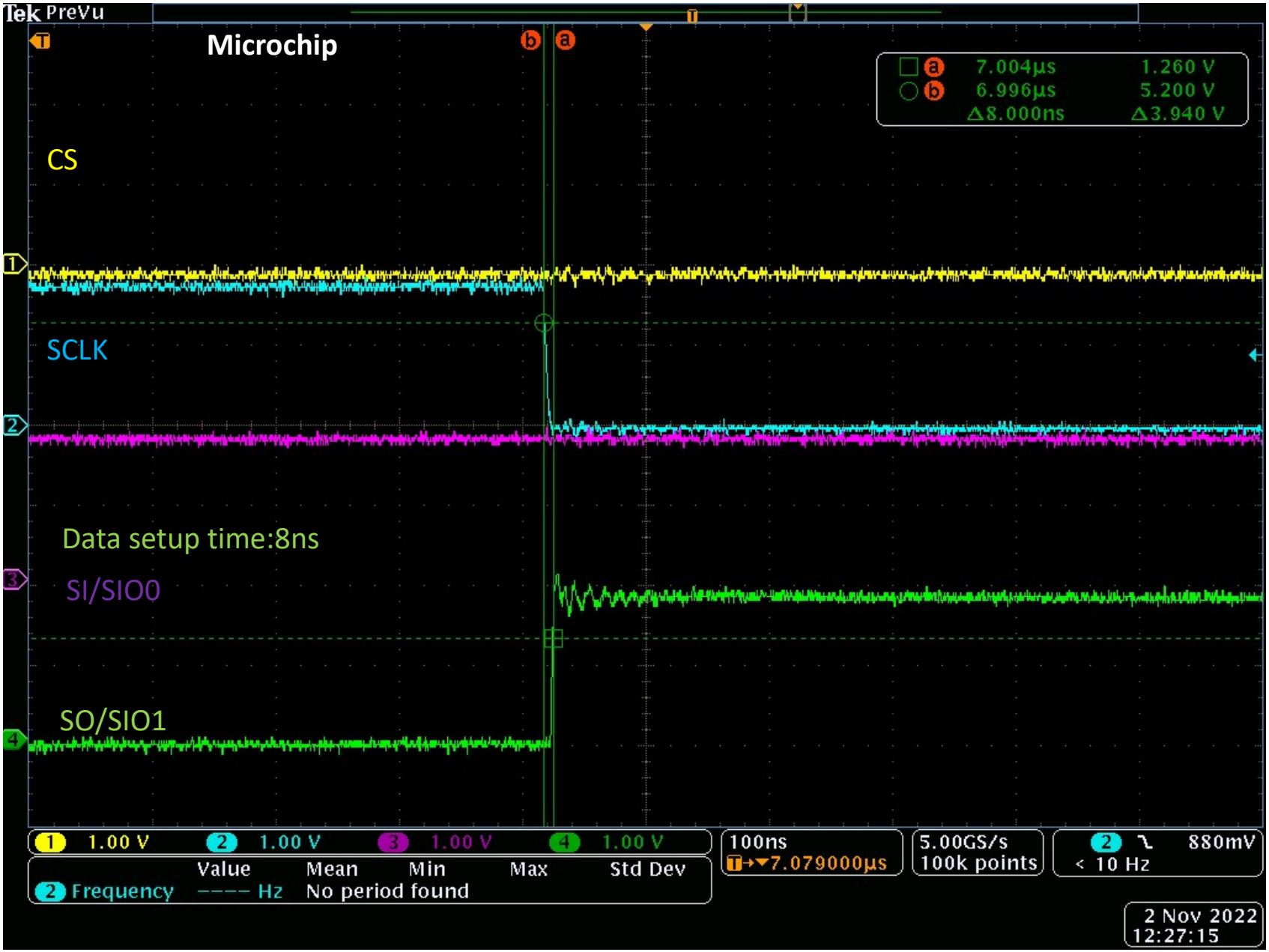


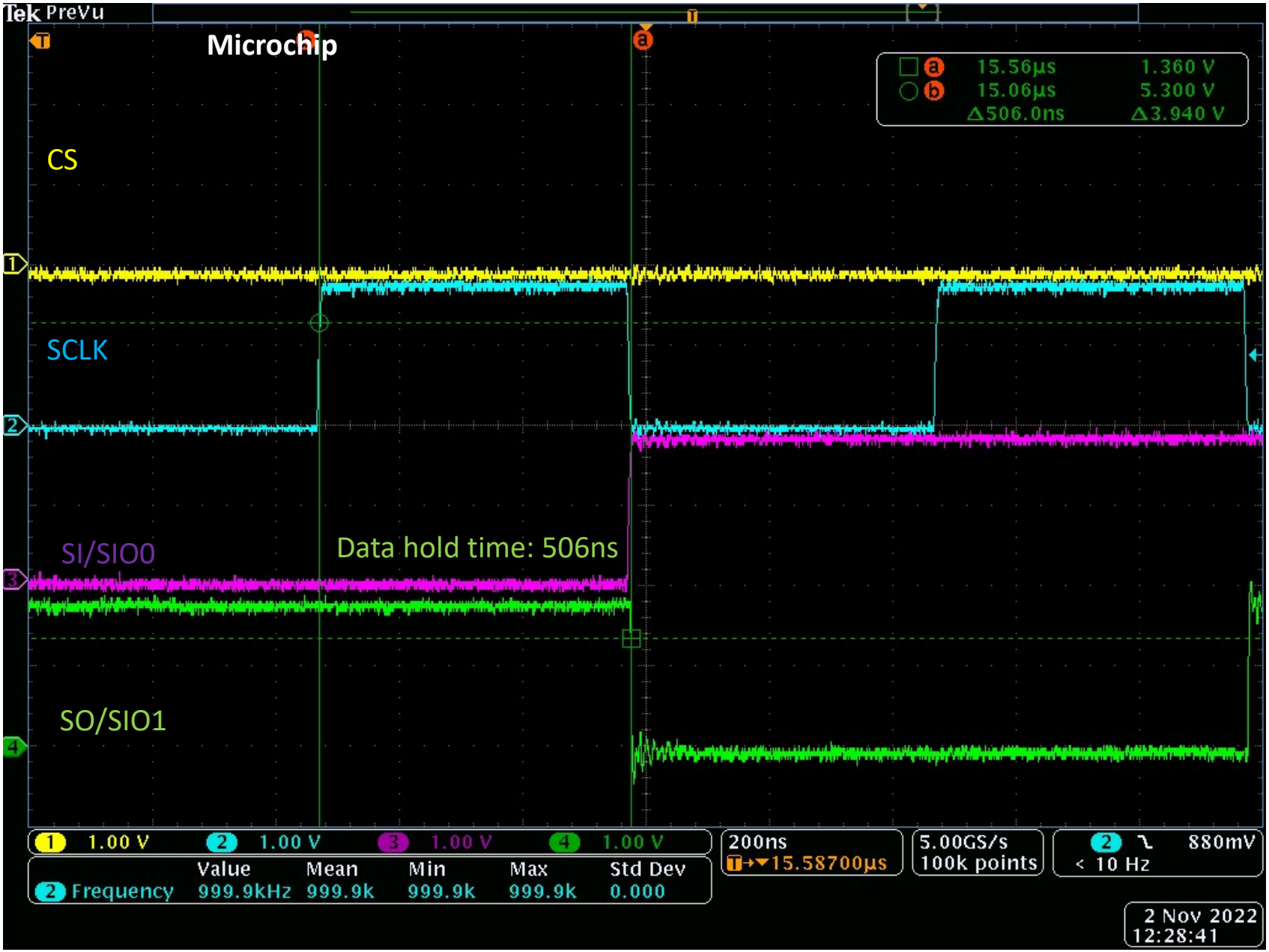

Tek PreVu
Microchip
CS
SCLK
SI/SIO0
SO/SIO1
1 1.00 V
2 1.00 V
3 1.00 V
4 1.00 V
Value Mean Min Max Std Dev
1 Max 1.90 V 1.90 1.90 1.90 0.00
1 Min −300mV −300m −300m −300m 0.00
1 Peak−Peak 2.20 V 2.20 2.20 2.20 0.00
1 Mean 33.5mV 33.5m 33.5m 33.5m 0.00
4.00µs
T→▼−3.160000µs
2.50GS/s
100k points
2 880mV
< 10 Hz
2 Nov 2022
11:21:18


Tek PreVu
Microchip
a 1.490µs 1.280 V
b 2.490µs −660.0mV
Δ1.000µs Δ1.940 V
CS
Clock frequency:1MHz
SCLK
SI/SIO0
SO/SIO1
1 1.00 V
2 1.00 V
3 1.00 V
4 1.00 V
1.00µs
T→▼2.170000µs
5.00GS/s
100k points
2 880mV
< 10 Hz
Value Mean Min Max Std Dev
2 Frequency 1.000MHz 1.000M 1.000M 1.000M 0.000
2 Nov 2022
11:25:10

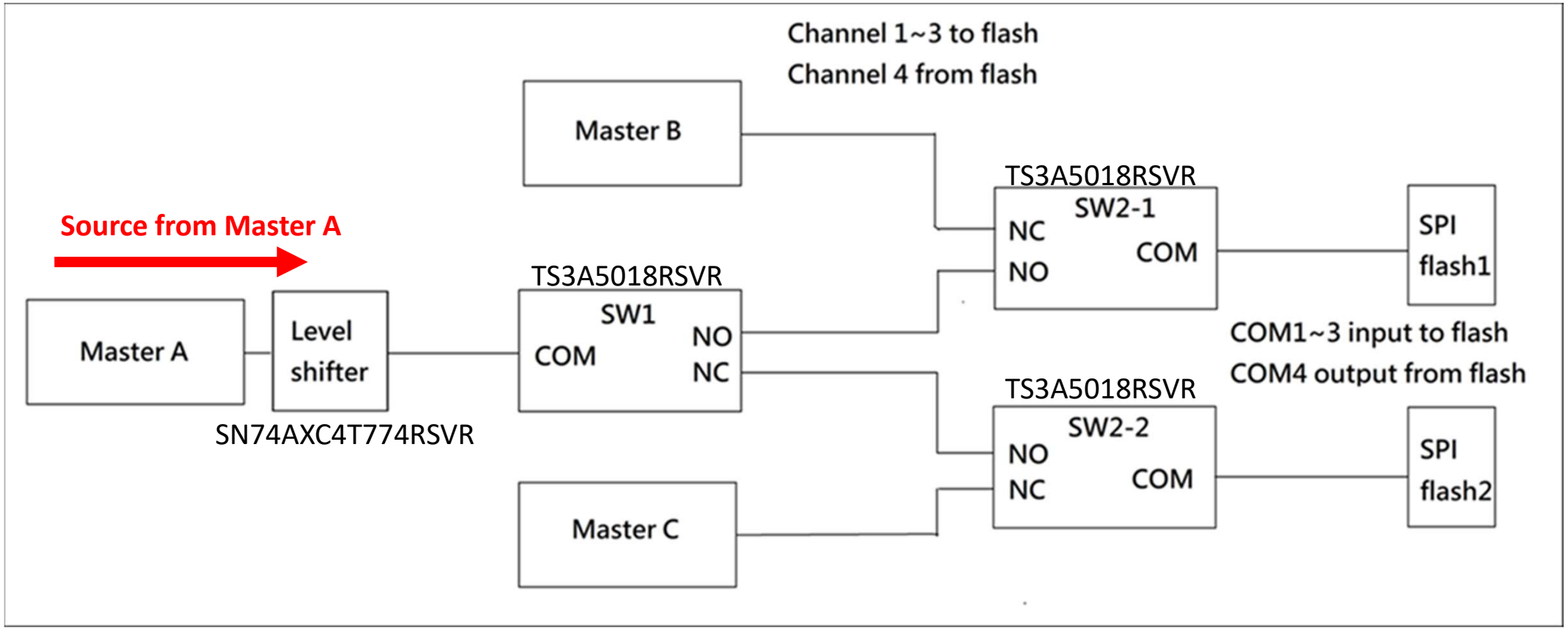

Tek PreVu
Microchip
a 1.999µs 1.260 V
b 2.498µs 3.200 V
Δ499.0ns Δ1.940 V
CS
SCLK
Data setup time: 499ns
SI/SIO0
SO/SIO1
1 1.00 V
2 1.00 V
3 1.00 V
4 1.00 V
100ns
T→▼2.170000µs
5.00GS/s
100k points
2 880mV
< 10 Hz
Value Mean Min Max Std Dev
2 Frequency ---- Hz No period found
2 Nov 2022
12:13:11

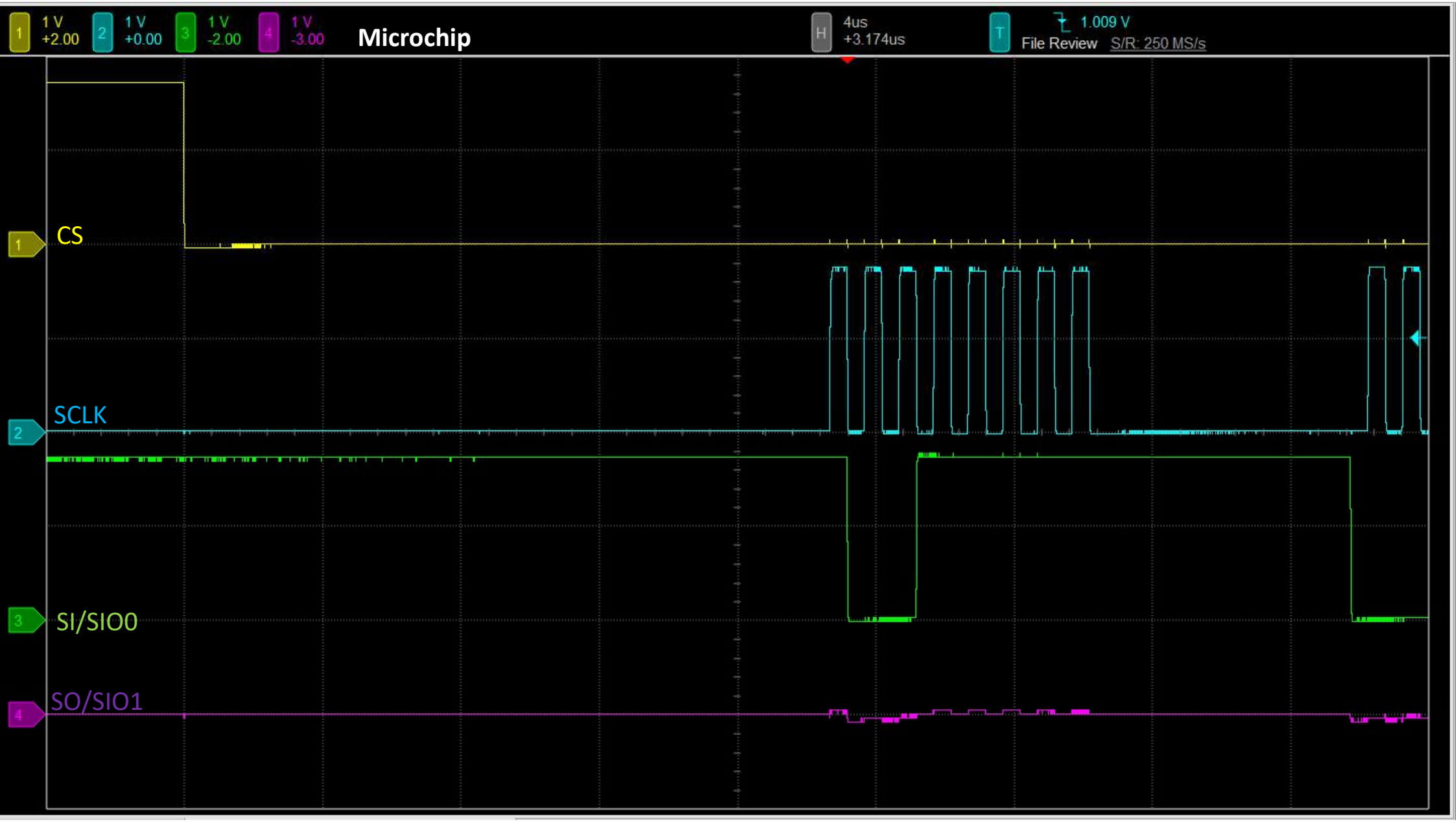

Tek PreVu
Microchip
a 0.000 s 1.260 V
b −502.0ns 3.200 V
Δ502.0ns Δ1.940 V
CS
Data hold time: 502ns
SCLK
SI/SIO0
SO/SIO1
1 1.00 V
2 1.00 V
3 1.00 V
4 1.00 V
Value Mean Min Max Std Dev
2 Frequency ---- Hz No period found
100ns
T→▼−85.00000ns
5.00GS/s
100k points
2 880mV
< 10 Hz
2 Nov 2022
12:16:29

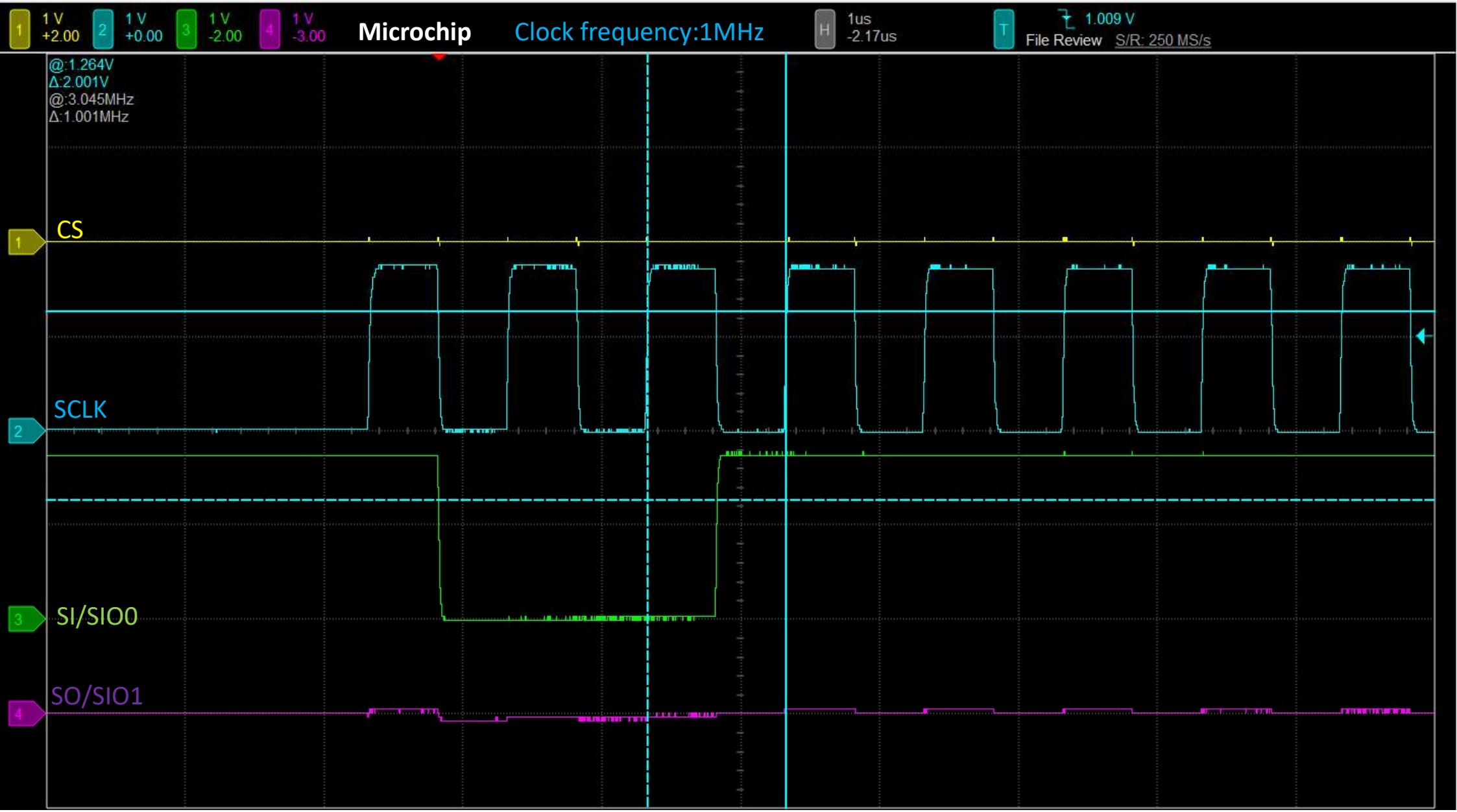

Tek PreVu
Microchip
a 7.004µs 1.260 V
b 6.996µs 5.200 V
Δ8.000ns Δ3.940 V
CS
SCLK
Data setup time:8ns
SI/SIO0
SO/SIO1
1 1.00 V
2 1.00 V
3 1.00 V
4 1.00 V
Value Mean Min Max Std Dev
2 Frequency ---- Hz No period found
100ns
T→▼7.079000µs
5.00GS/s
100k points
2 880mV
< 10 Hz
2 Nov 2022
12:27:15

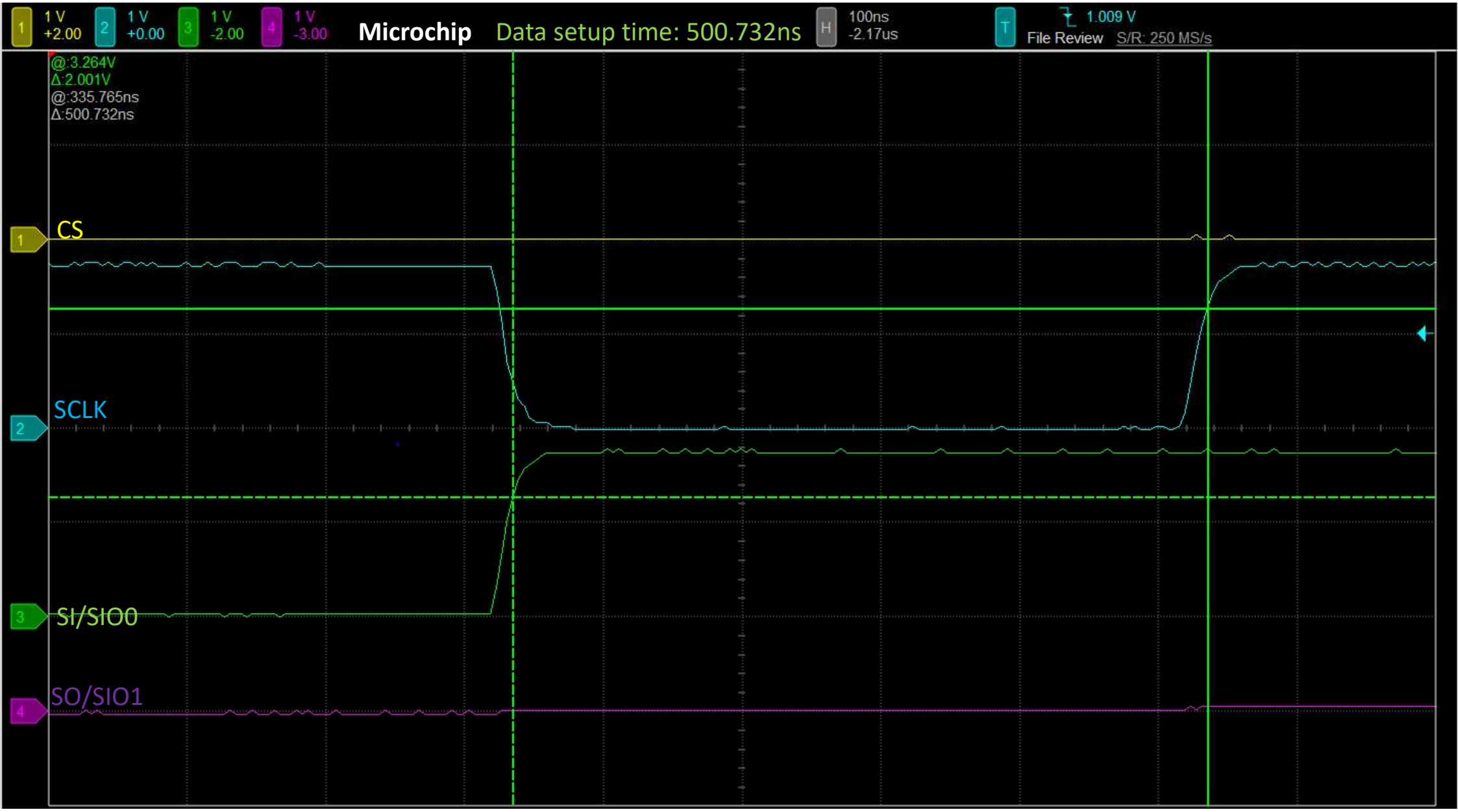

Tek PreVu
Microchip
a 15.56µs 1.360 V
b 15.06µs 5.300 V
Δ506.0ns Δ3.940 V
CS
SCLK
SI/SIO0
Data hold time: 506ns
SO/SIO1
1 1.00 V
2 1.00 V
3 1.00 V
4 1.00 V
200ns
T→▼15.58700µs
5.00GS/s
100k points
2 880mV
< 10 Hz
Value Mean Min Max Std Dev
2 Frequency 999.9kHz 999.9k 999.9k 999.9k 0.000
2 Nov 2022
12:28:41

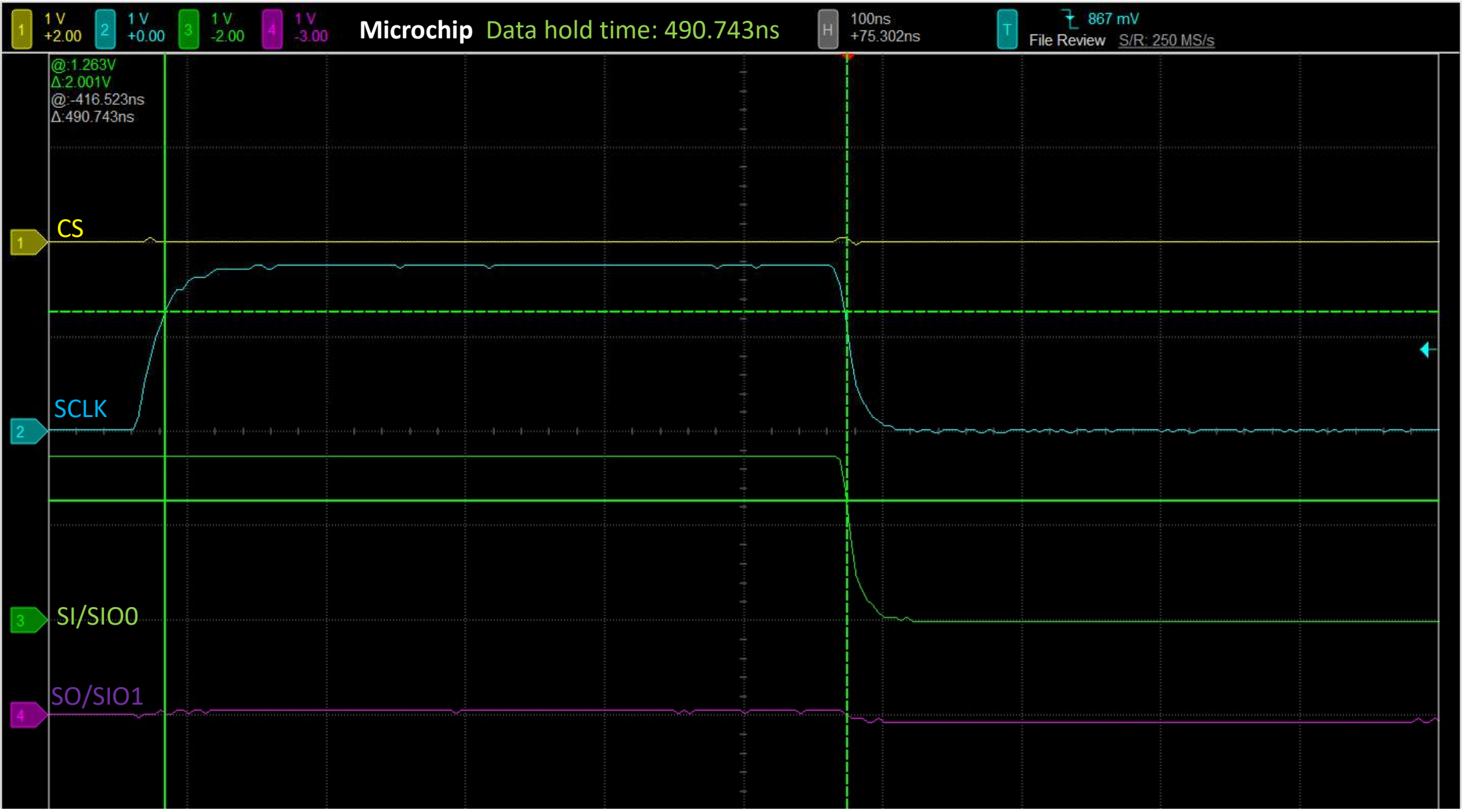
Structure of 2MUX cascaded in SPI application

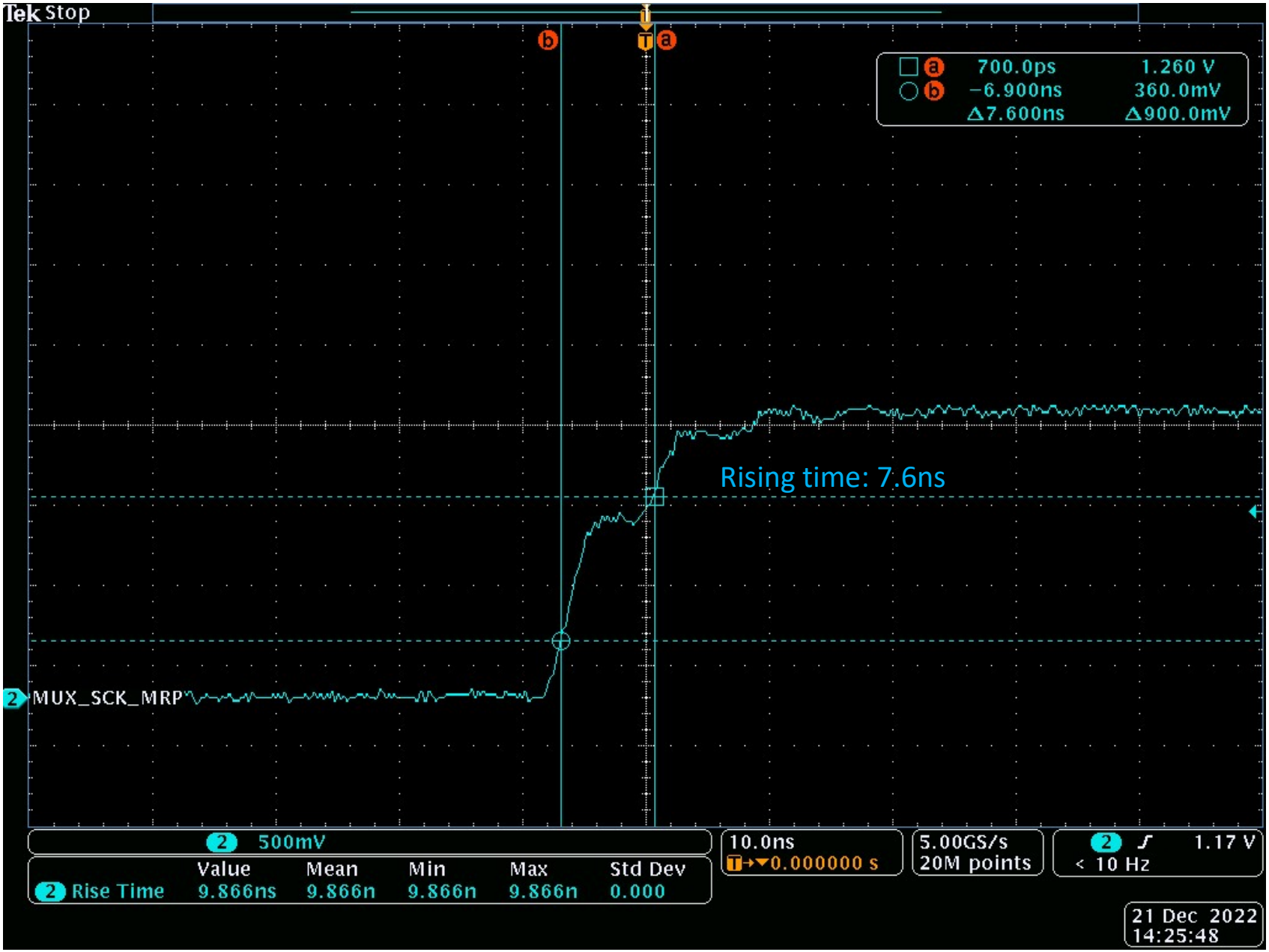



1 V
+2.00
1 V
+0.00
1 V
-2.00
1 V
-3.00
Microchip
4us
+3.174us
1.009 V
File Review
S/R: 250 MS/s
CS
SCLK
SI/SIO0
SO/SIO1

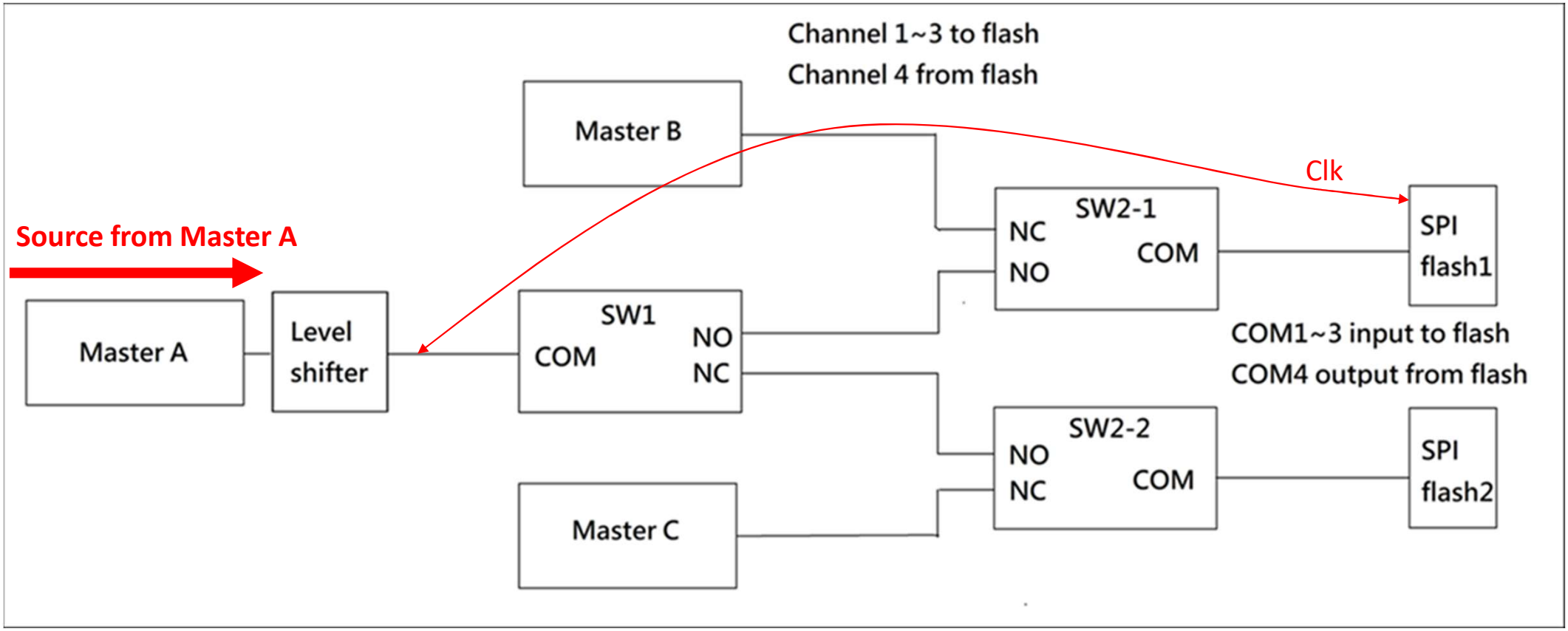

1 V
+2.00
1 V
+0.00
1 V
-2.00
1 V
-3.00
Microchip
Clock frequency:1MHz
1us
-2.17us
1.009 V
File Review
S/R: 250 MS/s
@:1.264V
Δ:2.001V
@:3.045MHz
Δ:1.001MHz
CS
SCLK
SI/SIO0
SO/SIO1


1 V
+2.00
1 V
+0.00
1 V
-2.00
1 V
-3.00
Microchip
Data setup time: 500.732ns
100ns
-2.17us
1.009 V
File Review
S/R: 250 MS/s
@:3.264V
Δ:2.001V
@:335.765ns
Δ:500.732ns
CS
SCLK
SI/SIO0
SO/SIO1


1 V
+2.00
1 V
+0.00
1 V
-2.00
1 V
-3.00
Microchip Data hold time: 490.743ns
100ns
+75.302ns
867 mV
File Review
S/R: 250 MS/s
@:1.263V
Δ:2.001V
@:-416.523ns
Δ:490.743ns
CS
SCLK
SI/SIO0
SO/SIO1


Tek Stop
a 700.0ps 1.260 V
b −6.900ns 360.0mV
Δ7.600ns Δ900.0mV
Rising time: 7.6ns
2 MUX_SCK_MRP
2 500mV
10.0ns
T→0.000000 s
5.00GS/s
20M points
2 1.17 V
< 10 Hz
Value Mean Min Max Std Dev
2 Rise Time 9.866ns 9.866n 9.866n 9.866n 0.000
21 Dec 2022
14:25:48

If jump the clk and by pass 2 MUX



Keysight Infiniium : Monday, January 09, 2023 02:59:01 PM