<Questions>

OutputX which is relation to PLL2 doesn't output in case of following conditions.

-PLL's setting -> please refer to the file "20200213_LMK03328_A.tcs".

PLL1 -> Output4, PLL2 -> Output1, 2, 3, 5, 6 and 7

(Other notes : PLLSTRTMODE = Parallel Cal)

(※ We measured with Output1 and Output6, the result was the same.)

-Connection to EVM -> please refer to the next page.

-Procedure

1. PRIREF : no input, SECREF : 50MHz input from crystal on EVM.
2. Operation of calibration(RESETN_SW toggles on GUI)
3. We measured the Output6 and Output4 using the Oscilloscope.

->In this case, Output6 doesn't output in spite of PLL2 lock condition.

As our assumption, in spite of PLL1 condition(no PRIREF),

Output6 should output.

Why does this phenomenon occur?

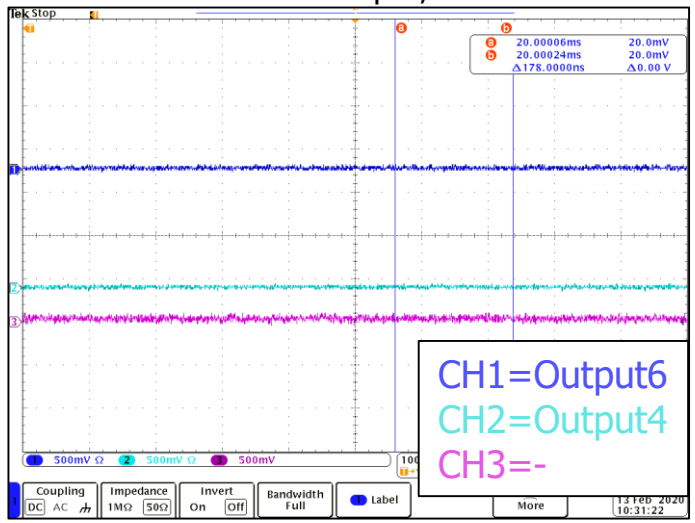
Is it possible to resolute using register setting?

And then, after PRIREF was inputted, OUTPUT6 outputted.

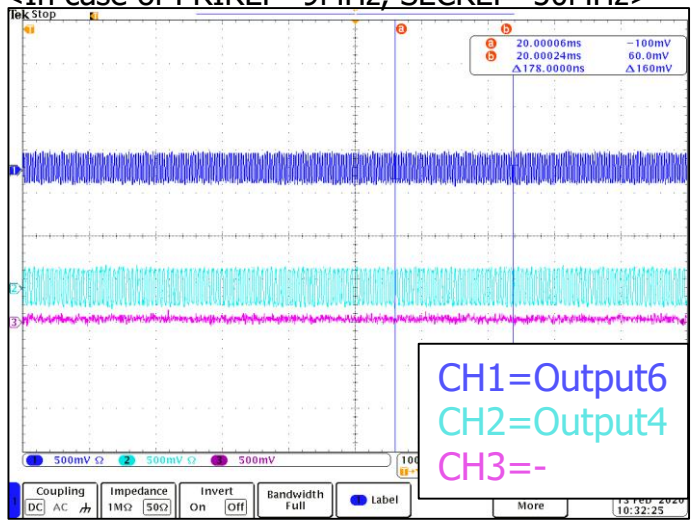
Therefore, does PRIREF have to be inputted first?

Could you confirm this phenomenon using your LMK03328 EVM?

<In case of PRIREF=no input, SECREF=50MHz>

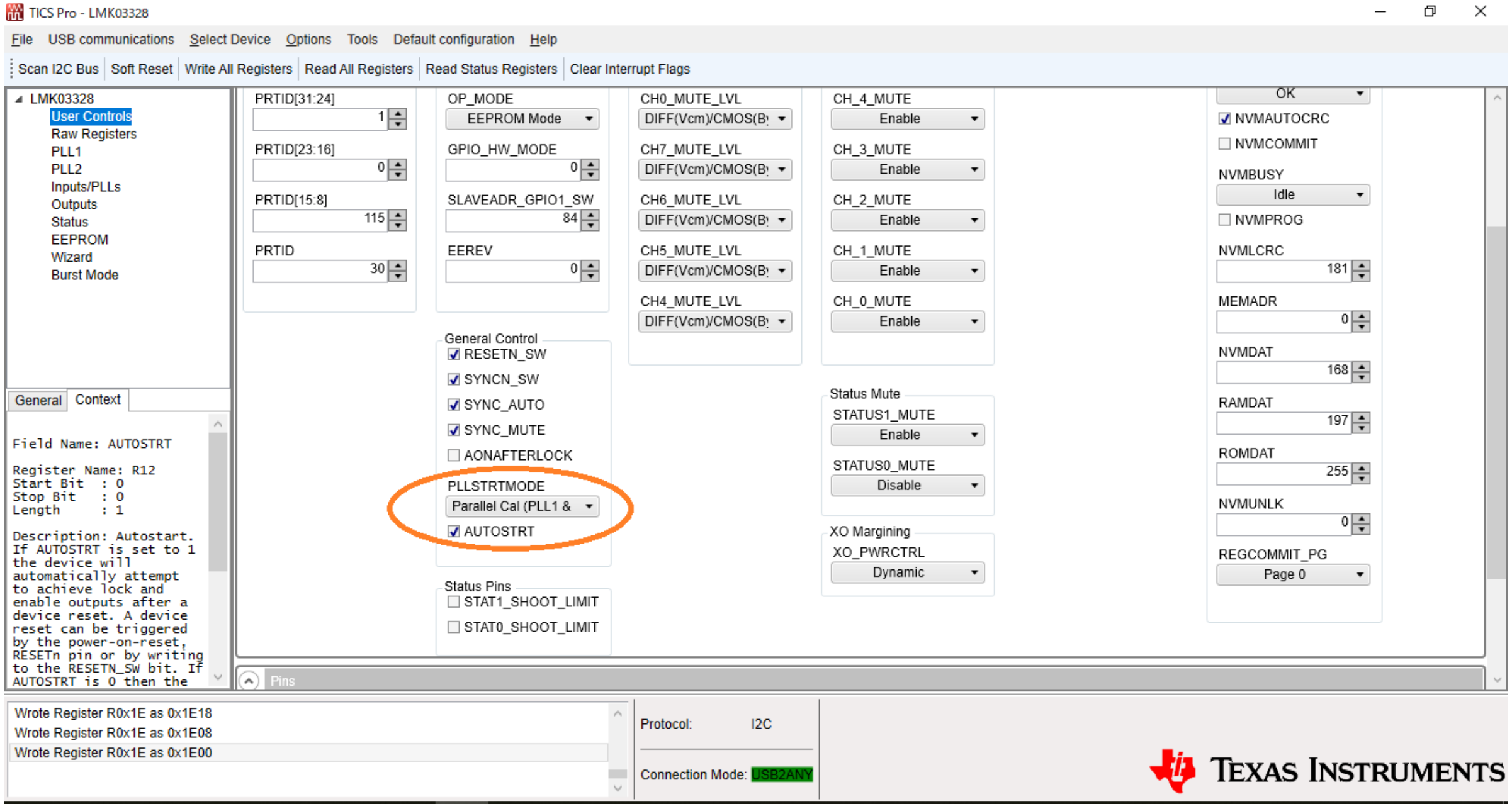


<In case of PRIREF=9MHz, SECREF=50MHz>

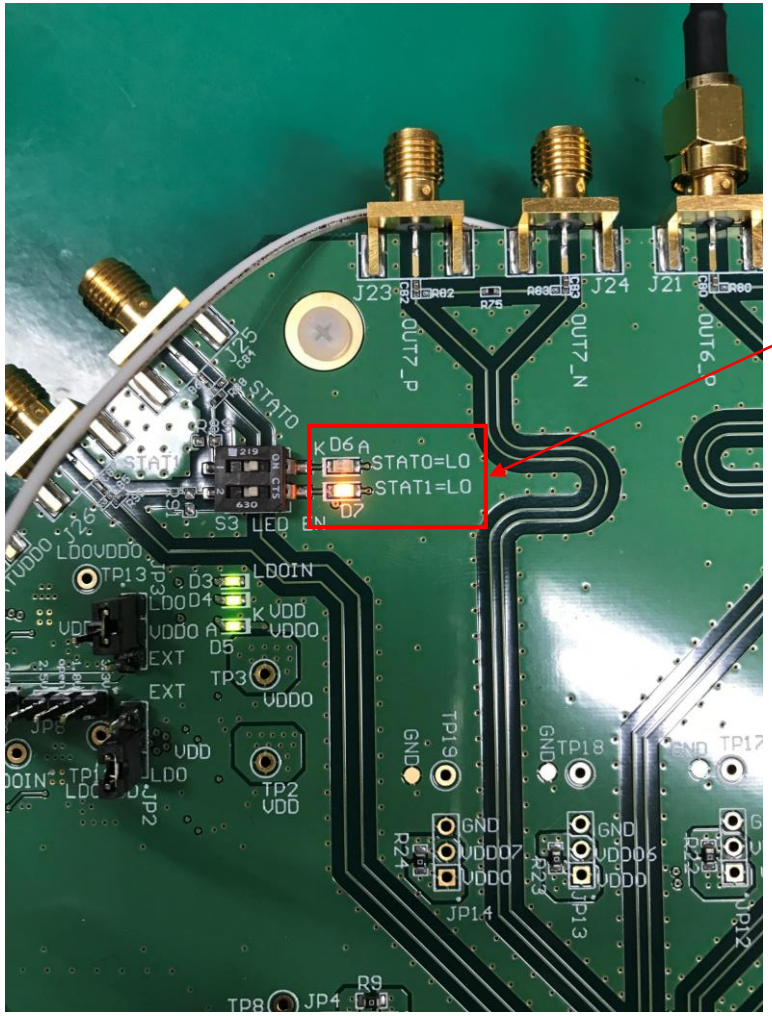


<EVM's connection>

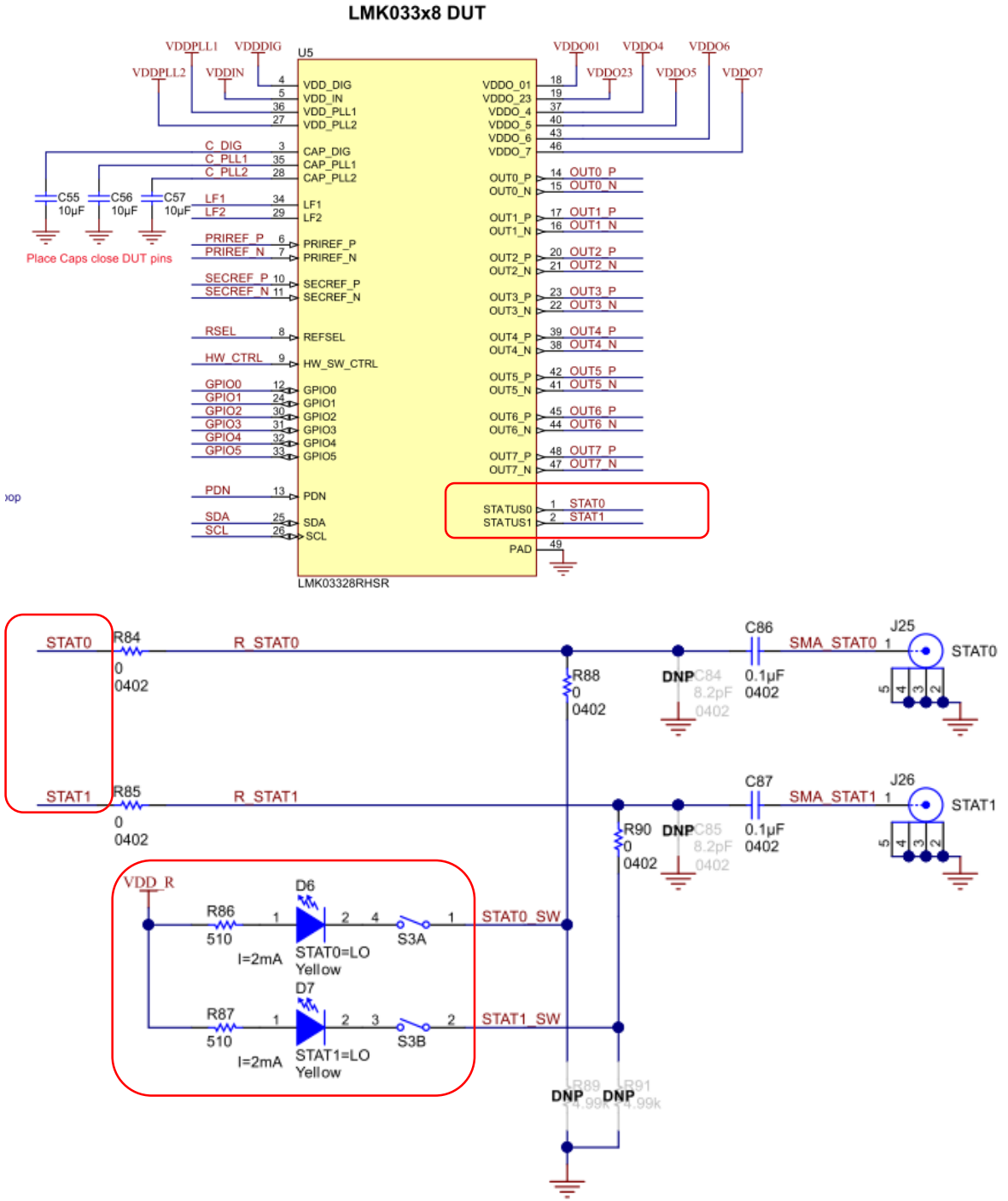
<PLLSTRTMODE setting>

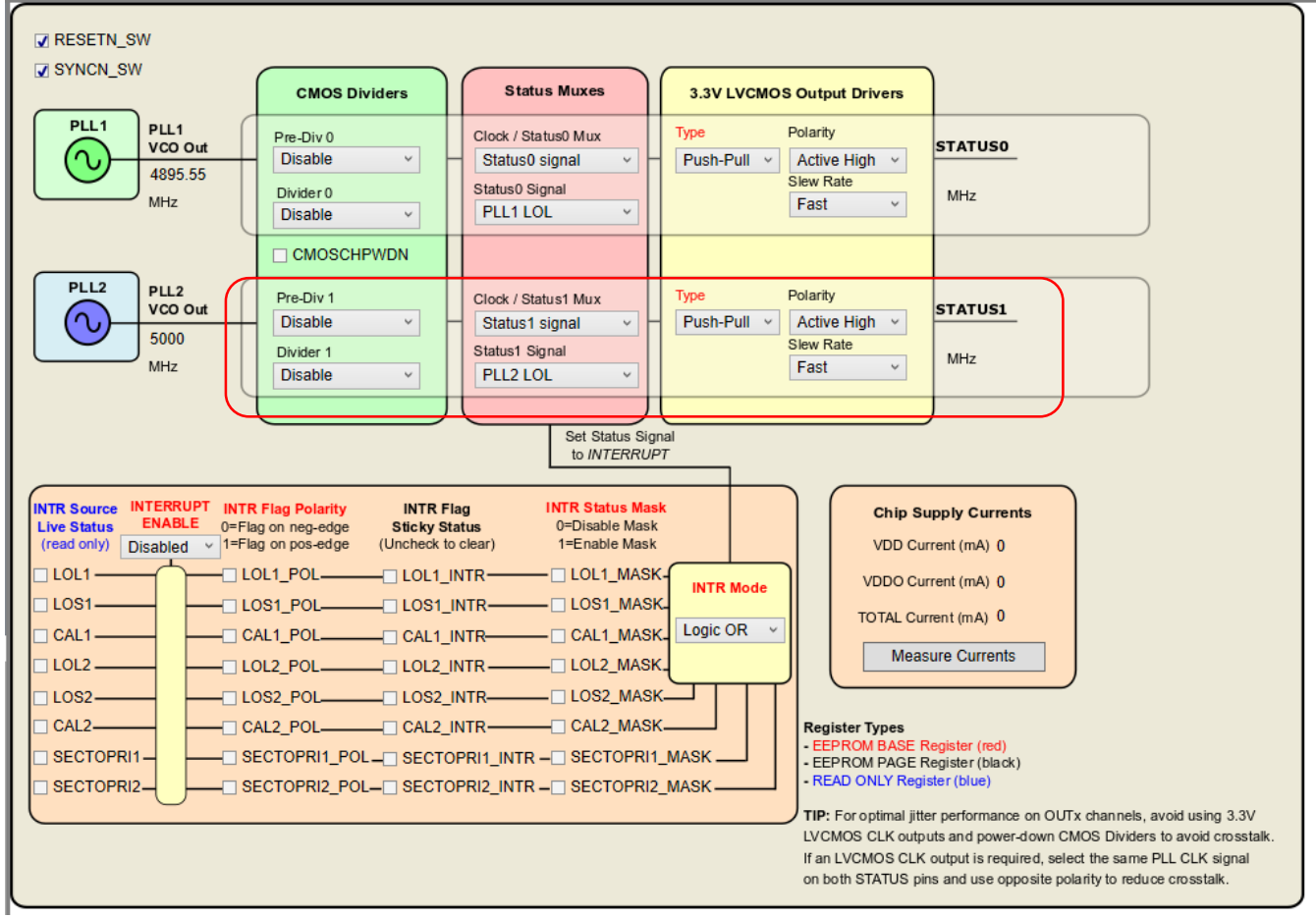


<PLL2 Lock condition In case of PRIREF=no input, SECREF=50MHz>



STAT0 : PLL1 no lock -> no matter
STAT1 : PLL2 shows “locked status.”
(Please to the next page.)





STAT1(Status1 setting)
-Type : Push pull
-Polarity : Active high
(it means the STAT1 output high in case of PLL=loss of lock.)
-Status1 Signal : PLL2 LOL(it means loss of lock at PLL2)
->Therefore,
in case of Lock status : STAT1 outputs low -> STAT1 turns on
in case of no Lock status : STAT1 outputs high -> STAT1 turns off