10M（TEST 1）-------------->CDCM6208(40M out)--------------->ad9361------------------>TEST2

# TEST1

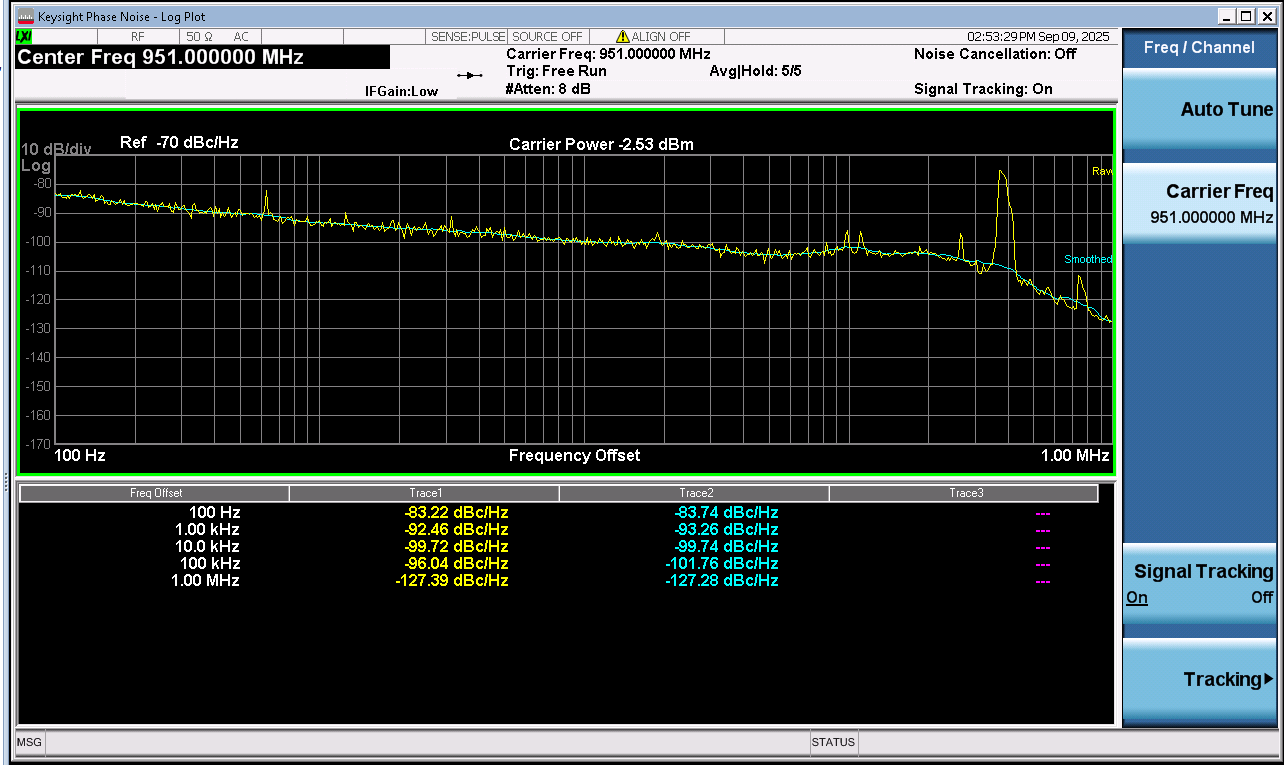
"The two clock sources (internal crystal oscillator and external input) show no obvious difference at the input side. However, the external clock source passes through some level-shifting circuits after entering the board, and we cannot rule out the possibility that these circuits introduce some noise. Since we are currently unable to test this inside the board, the issue cannot be fully confirmed."两种两种时钟源(内部晶振和外部输入)从输入端看不出明显差别，但是外部时钟源进入单板后经过了一些电平转换电路，不排除这部分电路引入了一些噪声。但是由于在单板内部我们当前没办法测试



# 2,TEST2

However, after switching the clock, the resulting IF signal shows a significant difference. On another board where we use the SI5345 PLL, this issue does not occur. After repeated comparisons, we found that the SI5345’s PLL bandwidth is around 100 Hz. Therefore, we would like to try reducing the bandwidth of the CDCM6208 to see if this improves the situation.

但是切换时钟后最终呈现的中频信号信号存在明显差异。我们另外一块单板采用的SI5345锁相环不会存在这种情况，我们反复对比差异后发现SI5345的锁相环带宽在100HZ左右。所以我们想尝试将CDCM6208的带宽改小一点，看下是否有改善.





# 3

We would appreciate it if you could provide us with a CDCM6208 configuration that reduces the loop bandwidth, so that we can test whether this improves the result.Our current configuration is shown below

所以我们想让你们帮看下，能不能出一份CDCM6208的配置，把带宽改小一些。以下是我们当前配置

