



12500 TI Boulevard, MS 8640, Dallas, Texas 75243

PCN# 20260211000.2

**Qualification of RFAB using qualified Process Technology, Datasheet, Die revision,
additional Assembly site, Test, and BOM options for select devices
Change Notification / Sample Request**

Date: February 12, 2026

To: SCHLUMBERGER PCN

Dear Customer:

This is an announcement of a change to a device that is currently offered by Texas Instruments (TI). The details of this change are on the following pages, and are in alignment with our standard product change notification (PCN) [process](#).

TI requires acknowledgement of receipt of this notification within 60 days of the date of this notice. Lack of acknowledgement of this notice within 60 days constitutes acceptance and approval of this change. If samples or additional data are required, requests must be received within 60 days of this notification, given that samples are not built ahead of the change.

The Proposed First Ship date in this PCN letter is the earliest possible date that customers could receive the changed material. It is our commitment that the changed device will not ship before that date. If samples are requested within the 60 day sample request window, customers will still have 30-days to complete their evaluation regardless of the proposed 1st ship date.

As referenced in the "reason for change" below, this particular PCN relates to TI's multiyear transition, announced in 2020, to close our 150mm production and move more capacity into 300mm. We are entering the final phases of this transition, and the final 150mm wafers started in October 2025. **Thus, it's critical that you take the appropriate actions, noted in this PCN, to prepare for applicable product changes.**

For questions regarding this notice or to provide acknowledgement of this PCN, you may contact your local Field Sales Representative or the Change Management team. For sample requests or sample related questions, contact your local Field Sales Representative. As always, we thank you for your continued business.

Change Management Team
SC Business Services

20260211000.2
Attachment: 1

Products Affected:

The devices listed on this page are a subset of the complete list of affected devices. According to our records, you have recently purchased these devices. The corresponding customer part number is also listed, if available.

DEVICE	CUSTOMER PART NUMBER
TLC555QDRQ1	NULL

Technical details of this Product Change follow on the next page(s).

PCN Number:	20260211000.2	PCN Date:	February 12, 2026																		
Title:	Qualification of RFAB using qualified Process Technology, Datasheet, Die revision, additional Assembly site, Test, and BOM options for select devices																				
Customer Contact:	Change Management Team	Dept:	Quality Services																		
Proposed 1st Ship Date:	August 11, 2026	Sample requests accepted until:	April 13, 2026*																		
*Sample requests received after April 13, 2026 will not be supported.																					
Change Type:																					
☒ Assembly Site	☒ Design	☐ Wafer Bump Material																			
☒ Assembly Process	☒ Data Sheet	☐ Wafer Bump Process																			
☒ Assembly Materials	☐ Part number change	☒ Wafer Fab Site																			
☐ Mechanical Specification	☒ Test Site	☒ Wafer Fab Material																			
☒ Packing/Shipping/Labeling	☐ Test Process	☒ Wafer Fab Process																			
PCN Details																					
Description of Change:																					
Texas Instruments is pleased to announce the addition of RFAB using the HPA9 qualified process technology technology and additional Assembly site and BOM options for the devices product affected section below.																					
<table border="1"> <thead> <tr> <th colspan="3">Current Fab Site</th> <th colspan="3">Additional Fab Site</th> </tr> <tr> <th>Current Fab Site</th> <th>Process</th> <th>Wafer Diameter</th> <th>Additional Fab Site</th> <th>Process</th> <th>Wafer Diameter</th> </tr> </thead> <tbody> <tr> <td>DL-LIN</td> <td>LINCMOS</td> <td>150 mm</td> <td>RFAB</td> <td>HPA9</td> <td>300 mm</td> </tr> </tbody> </table>			Current Fab Site			Additional Fab Site			Current Fab Site	Process	Wafer Diameter	Additional Fab Site	Process	Wafer Diameter	DL-LIN	LINCMOS	150 mm	RFAB	HPA9	300 mm	
Current Fab Site			Additional Fab Site																		
Current Fab Site	Process	Wafer Diameter	Additional Fab Site	Process	Wafer Diameter																
DL-LIN	LINCMOS	150 mm	RFAB	HPA9	300 mm																
The die was also changed as a result of the process change.																					
<table border="1"> <thead> <tr> <th></th> <th>Current</th> <th>Proposed</th> </tr> <tr> <th>Probe Test</th> <th>With Probe</th> <th>Without Probe</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td></td> </tr> </tbody> </table>			Current	Proposed	Probe Test	With Probe	Without Probe														
	Current	Proposed																			
Probe Test	With Probe	Without Probe																			
Construction differences are as follows:																					
Group 1: Additional Assembly site + BOM options + Laser Saw + Additional Test Site																					
	Current	New BOM	Additional Site																		
Assembly Site	MLA	MLA	FMX																		
Mold compound	EME-G700FGT	EME-G633C	EME-G633C																		
Mount compound	FS849-TI	QMI 505MT	QMI 505MT																		
Bond wire diam, material	0.96 mil Au	0.80 mil Cu	0.80 mil Cu																		
Die Scribe	Mechanical	Laser	Laser																		
	Current	Additional																			
Test Site	FMX	MLA																			
Group 2: Additional Test Site + Bond Wire + Laser Saw																					
	Current	New																			
Bond wire diam, material	0.96 mil Au	0.80 mil Cu																			
Die Scribe	Mechanical	Laser																			
	Current	Additional																			
Test Site	FMX	MLA																			

Groups 1 and 2:

The die design and layout has been updated as a consequence of being moved onto a more advanced process technology.

In conjunction with this notice, the probe test step will be removed from the process flow. Test coverage for all datasheet parameters will remain.

The datasheet will be changing as a result of the design change.



TLC555-Q1
SLFS078D – OCTOBER 2006 – REVISED JANUARY 2026

Changes from Revision C (March 2023) to Revision D (January 2026)	Page
• Removed LinCMOS™ terminology from data sheet.....	0
• Increased the Human-body model (HBM) ESD rating from 1kV to 2kV.....	3
• Removed the reset current (I_{RESET}) typical specification with test condition $V_{\text{RESET}} = 0\text{V}$ in <i>Electrical Characteristics: $V_{\text{DD}} = 5\text{V}$</i>	4
• Removed the test condition $V_{\text{RESET}} = V_{\text{DD}}$ from reset current (I_{RESET}) in <i>Electrical Characteristics: $V_{\text{DD}} = 5\text{V}$</i>	4
• Changed the typical value of discharge switch off-stage current at 25°C from 0.1nA to 0.3nA in <i>Electrical Characteristics: $V_{\text{DD}} = 5\text{V}$</i>	4
• Changed the typical value of discharge switch off-stage current at max temperature range from 120nA to 275nA in <i>Electrical Characteristics: $V_{\text{DD}} = 5\text{V}$</i>	4
• Changed the typical value of discharge switch on-stage voltage at 25°C from 0.14V to 0.06V in <i>Electrical Characteristics: $V_{\text{DD}} = 5\text{V}$</i>	4
• Removed the reset current (I_{RESET}) typical specification with test condition $V_{\text{RESET}} = 0\text{V}$ in <i>Electrical Characteristics: $V_{\text{DD}} = 15\text{V}$</i>	5
• Removed the test condition $V_{\text{RESET}} = V_{\text{DD}}$ from reset current (I_{RESET}) in <i>Electrical Characteristics: $V_{\text{DD}} = 15\text{V}$</i>	5
• Changed the typical value of discharge switch off-stage current at 25°C from 0.1nA to 0.75nA in <i>Electrical Characteristics: $V_{\text{DD}} = 15\text{V}$</i>	5
• Changed the typical value of discharge switch off-stage current at max temperature range from 120nA to 280nA in <i>Electrical Characteristics: $V_{\text{DD}} = 15\text{V}$</i>	5
• Changed the typical value of supply current at 25°C from 360µA to 235µA in <i>Electrical Characteristics: $V_{\text{DD}} = 15\text{V}$</i>	5
• Updated all charts in the Typical Characteristics section.....	6

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
TLC555-Q1	SLFS078C	SLFS078D	http://www.ti.com/product/TLC555-Q1

Qual details are provided in the Qual Data Section.

Reason for Change:

These changes are part of our multiyear plan to transition products from our 150 and 200-millimeter factories to newer, more efficient manufacturing processes and technologies, underscoring our commitment to product longevity and supply continuity.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Changes to product identification resulting from this PCN:

Wafer Fab Site Information:

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
DFAB	DL-LIN	DLN	USA
RFAB	RFB	USA	Richardson

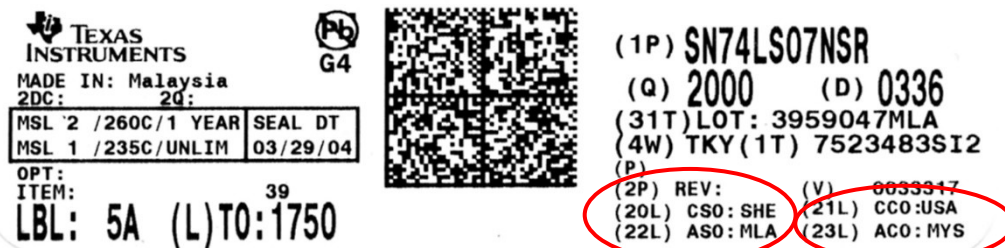
Die Rev:**Current****New**

Die Rev [2P]	Die Rev [2P]
F	B

Assembly Site Information:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
MLA	MLA	MYS	KUALA LUMPUR
FMX	MEX	MEX	Aguascalientes

Sample product shipping label (not actual product label):

**Product Affected- Group 1_Wafer Fab, Assembly site, Die rev, BOM and Test site changes :**

TLC555ZQDRQ1

Product Affected- Group 2_Wafer Fab, Die Rev, Test Site change only:

TLC555QDRQ1

For alternate parts with similar or improved performance, please visit the product page on [TI.com](https://www.ti.com)

Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

TLC555-Q1
FMX Assembly
Approve Date 19-December-2025

Product Attributes

Attributes	Qual Device: TLC555QDRQ1	QBS Process Reference: INA229AQDGSRQ1	QBS Package, Process, Product Reference: TLC555QDRQ1	QBS Package, Process, Product Reference: TLC555QDRQ1	QBS Package Reference: SN74LVC11ADRQ1	QBS Package Reference: SN74LVC132ADRQ1	QBS Package Reference: SN74LVC74ADRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Logic	Logic	Logic
Wafer Fab Supplier	RFAB	RFAB	RFAB	RFAB	RFAB	RFAB	RFAB
Assembly Site	FMX	ASESHAT	FMX	FMX	FMX	FMX	FMX
Package Group	SOIC	VSSOP	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	D	DGS	D	D	D	D	D
Pin Count	8	10	8	8	14	14	14

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device TLC555QDRQ1 is qualified at MSL1 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: TLC555QDRQ1	QBS Process Reference: INA229AQDGSRQ1	QBS Package, Process, Product Reference: TLC555QDRQ1	QBS Package, Process, Product Reference: TLC3555QDRQ1	QBS Package Reference: SN74LVC11ADRO1	QBS Package Reference: SN74LVC132ADRO1	QBS Package Reference: SN74LVC74ADRO1
Test Group A - Accelerated Environment Stress Tests														
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	-	1/Pass	1/Pass	1/Pass	1/Pass	1/Pass
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	1/77/0	1/77/0	1/77/0	1/77/0	1/77/0
ACUHA	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	-	-	1/77/0	1/77/0	1/77/0
ACUHA	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-	-	1/77/0	1/77/0	-	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	-	1/77/0	1/77/0	1/77/0	1/77/0	1/77/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	1/45/0	1/45/0	-	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	-	-	1/45/0	1/45/0	1/45/0
Test Group B - Accelerated Lifetime Simulation Tests														
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	3/231/0	2/154/0	1/77/0	-	-	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-	-	-	-
Test Group C - Package Assembly Integrity Tests														
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	-	-	-
Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: TLC555QDRQ1	QBS Process Reference: INA229AQDGSRQ1	QBS Package, Process, Product Reference: TLC555QDRQ1	QBS Package, Process, Product Reference: TLC3555QDRQ1	QBS Package Reference: SN74LVC11ADRO1	QBS Package Reference: SN74LVC132ADRO1	QBS Package Reference: SN74LVC74ADRO1
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/15/0	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0	-	-	1/10/0	1/10/0	1/10/0	1/10/0
Test Group D - Die Fabrication Reliability Tests														
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDOB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests														
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	-	1/3/0	1/3/0	-	-	-
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	-	1/3/0	1/3/0	-	-	-
ESD	E3	AEC Q100-011	1	3	ESD CDM	Corner pins	750 Volts	1/3/0	-	-	-	-	-	-
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	1/3/0	-	1/6/0	1/3/0	-	-	-
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	-	1/30/0	3/90/0	-	-	-

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Orderable Part Numbers

The following table contains a list of all TI Orderable Part Numbers (OPNs) released by this qualification per Product Qualification Family definition (AEC Q100 Appendix 1). Group E results shown above cover all part numbers listed here.

TLC555QDRQ1	TLC555QDRQ1.A
TLC555ZQDRQ1	TLC555ZQDRQ1.A

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or J) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/HAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2508-038

Automotive Qualification Summary (As per AEC and JEDEC Guidelines)

Q006 SOIC at FMX
Approve Date 16-DECEMBER -2024

Attributes	Qual Device:	Qual Device:	Qual Device:
	<u>SN74LVC11ADRQ1</u>	<u>SN74LVC132ADRQ1</u>	<u>SN74LVC74ADRQ1</u>
Automotive Grade Level	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125
Product Function	Logic	Logic	Logic
Wafer Fab Supplier	RFAB	RFAB	RFAB
Assembly Site	FMX	FMX	FMX
Package Group	SOIC	SOIC	SOIC
Package Designator	D	D	D
Pin Count	14	14	14

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <u>SN74LVC11ADRQ1</u>	Qual Device: <u>SN74LVC132ADRQ1</u>	Qual Device: <u>SN74LVC74ADRQ1</u>
Test Group A - Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	1/0/0	1/0/0	1/0/0
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	1/22/0	1/22/0	1/22/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	1/22/0	1/22/0	1/22/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	1/77/0	1/77/0	1/77/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	1/77/0	1/77/0	1/77/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST, 2X	Review for delamination	Completed	1/22/0	1/22/0	1/22/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	1/3/0	1/3/0	1/3/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <u>SN74LVC11ADRQ1</u>	Qual Device: <u>SN74LVC132ADRQ1</u>	Qual Device: <u>SN74LVC74ADRQ1</u>
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	1/77/0	1/77/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC, 1X	Review for delamination	Completed	1/22/0	1/22/0	1/22/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	1/77/0	1/77/0	1/77/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	1/22/0	1/22/0	1/22/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	1/3/0	1/3/0	1/3/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC11ADRQ1	Qual Device: SN74LVC132ADRQ1	Qual Device: SN74LVC74ADRQ1
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	-	-	-
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	175C	500 Hours	1/45/0	1/45/0	1/45/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	-	-	-
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	175C	1000 Hours	1/45/0	1/45/0	1/45/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
Test Group C - Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device SN74LVC11ADRQ1 is qualified at MSL1 260C
- Qual Device SN74LVC132ADRQ1 is qualified at MSL1 260C
- Qual Device SN74LVC74ADRQ1 is qualified at MSL1 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-NPD-2307-083

Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

TLC555-Q1
MLA Assembly
Approve Date 19-December-2025

Product Attributes

Attributes	Qual Device: TLC555QDRQ1	QBS Package Reference: TLV902QDRQ1	QBS Process Reference: INA229AQDGSRQ1	QBS Package, Product Reference: TLC555QDRQ1	QBS Package Reference: OPA2991QDRQ1	QBS Package Reference: TLV3702QDRQ1	QBS Process, Product Reference: TLC555QDRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain
Wafer Fab Supplier	RFAB	RFAB	RFAB	RFAB	RFAB	RFAB	RFAB
Assembly Site	MLA	MLA	ASESHAT	MLA	MLA	MLA	FMX
Package Group	SOIC	SOIC	VSSOP	SOIC	SOIC	SOIC	SOIC
Package Designator	D	D	DGS	D	D	D	D
Pin Count	8	8	10	8	8	8	8

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device TLC555QDRQ1 is qualified at MSL1 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: TLC555QDRQ1	QBS Package Reference: TLV9022QDRQ1	QBS Process Reference: INA229AQDGSRQ1	QBS Package, Product Reference: TLC555QDRQ1	QBS Package Reference: OPA2981QDRQ1	QBS Package Reference: TLV3702QDRQ1	QBS Process, Product Reference: TLC555QDRQ1
Test Group A - Accelerated Environment Stress Tests														
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	3/0/0	-	1/132/0	3/924/0	1/0/0	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	3/231/0	-	1/77/0	3/231/0	1/77/0	-
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-	3/231/0	-	1/77/0	3/231/0	1/77/0	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	3/231/0	-	1/109/0	3/231/0	1/77/0	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	-	-	-	-	1/5/0	1/5/0	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	3/135/0	-	1/50/0	3/135/0	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	-	-	-	1/77/0	-
Test Group B - Accelerated Lifetime Simulation Tests														
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	3/231/0	1/77/0	-	-	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	-	-	-	-
Test Group C - Package Assembly Integrity Tests														
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	3/90/0	-	1/30/0	3/90/0	1/30/0	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	3/90/0	-	1/30/0	3/90/0	1/30/0	-
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	1/15/0	-	1/15/0	-	1/15/0	-

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: TLC555QDRQ1	QBS Package Reference: TLV9022QDRQ1	QBS Process Reference: INA229AQDGSRQ1	QBS Package, Product Reference: TLC555QDRQ1	QBS Package Reference: OPA2981QDRQ1	QBS Package Reference: TLV3702QDRQ1	QBS Process, Product Reference: TLC555QDRQ1
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	1/15/0	-	1/15/0	-	1/15/0	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0	3/30/0	-	1/10/0	3/30/0	1/10/0	-

Test Group D - Die Fabrication Reliability Tests														
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDb	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements

Test Group E - Electrical Verification Tests														
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	-	-	-	1/3/0	-	-	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	-	-	-	1/3/0	-	-	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	Corner pins	750 Volts	-	-	-	-	-	-	1/3/0
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	-	-	-	1/6/0	-	-	1/3/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	-	-	3/90/0	-	-	1/30/0

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Orderable Part Numbers

The following table contains a list of all TI Orderable Part Numbers (OPNs) released by this qualification per Product Qualification Family definition (AEC Q100 Appendix 1). Group E results shown above cover all part numbers listed here.

TLC555QDRQ1	TLC555QDRQ1A
TLC555ZQDRQ1	TLC555ZQDRQ1A

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : ACuHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2508-039

Automotive Qualification Summary (As per AEC and JEDEC Guidelines)

Q006 SOIC at MLA
Approve Date 19-MAY -2022

Attributes	Qual Device: <u>OPA2991QDRQ1</u>
Automotive Grade Level	Grade 1
Operating Temp Range (C)	-40 to 125
Product Function	Signal Chain
Wafer Fab Supplier	RFAB
Assembly Site	MLA
Package Group	SOIC
Package Designator	D
Pin Count	8

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: OPA2991QDRQ1
Test Group A - Accelerated Environment Stress Tests								
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/924/0
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	3/3/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	3/9/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	3/9/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	3/9/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	3/231/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	3/9/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	3/3/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: OPA2991QDRQ1
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	3/9/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	3/9/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	3/9/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/231/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	3/3/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	3/135/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0
Test Group C - Package Assembly Integrity Tests								
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device OPA2991QDRQ1 is qualified at MSL1 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
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Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-BKF-2205-008

ZVEI ID: SEM-PA-19, SEM-PA-07, SEM-PA-11, SEM-DE-01, SEM-DE-02, SEM-TF-01, SEM-DS-01, SEM-PW-13, SEM-PW-02, SEM-PS-04, SEM-QG-01

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